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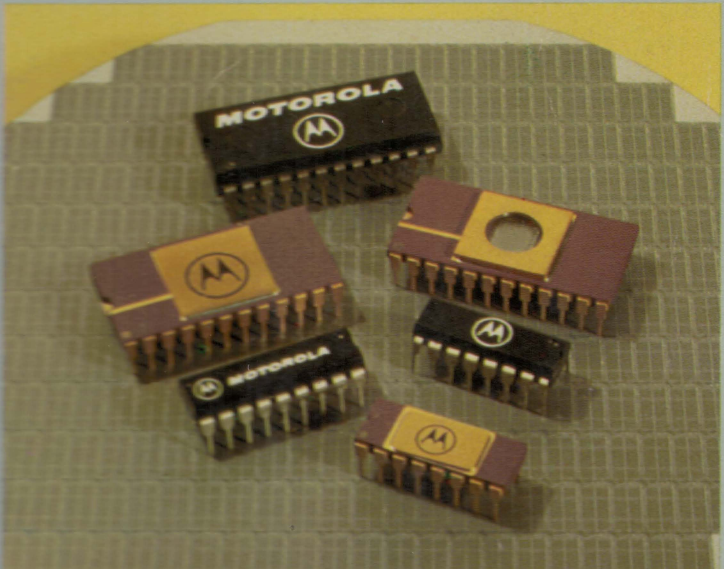
MOTOROLA
MEMORY
DATA MANUAL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- QUALITY
- RELIABILITY
- TECHNOLOGY

MOTOROLA MEMORY DATA MANUAL

Selector Guides	Selector
MOS Dynamic RAM	DRAM
MOS Static RAM	SRAM
MOS EPROM	EPROM
MOS EEPROM	EEPROM
MOS ROM	ROM
TTL RAM	TTL RAM
TTL PROM	TTL PROM
MECL Memory General Information	MECL
MECL RAM	MECL RAM
MECL PROM	MECL PROM
Mechanical Data	Mechanical

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MEMORIES

Prepared by
Technical Information Center

Motorola has developed a very broad range of reliable MOS and bipolar memories for virtually any digital data processing system application. Complete specifications for the individual circuits are provided in the form of data sheets. In addition, selector guides are included to simplify the task of choosing the best combination of circuits for optimum system architecture.

New Motorola memories are being introduced continually. For the latest releases, and additional technical information or pricing, contact your nearest authorized Motorola distributor or Motorola sales office.

The information in this book has been carefully checked; no responsibility, however, is assumed for inaccuracies. Furthermore, this information does not convey to the purchaser of microelectronic devices any license under the patent rights of the manufacturer.

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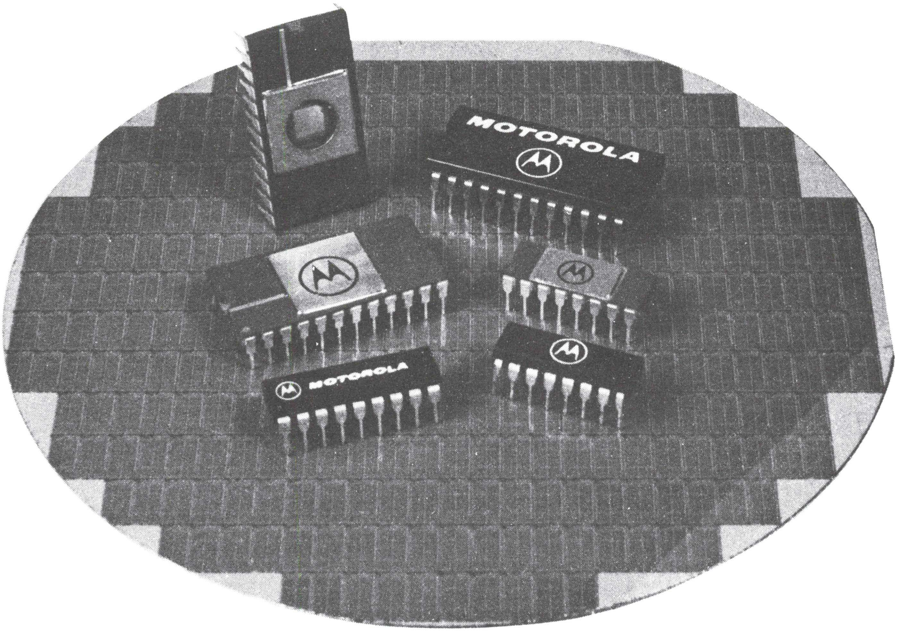
Selector Guides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NOTES

Not all package options are listed.

Operating temperature ranges:
MOS — 0°C to 70°C
ECL — Consult individual data sheets
TTL — Military −55°C to +125°C, Commercial 0°C to 70°C

FOOTNOTES

[1] Motorola's innovative pin #1 refresh

[2] All MOS memory outputs are three-state except the open collector MCM2115A series.

[3] Character generators include shifted and unshifted characters, ASCII, alphanumeric control, math, Japanese, British, German, European and French symbols.

[4] Standard Patterns for MOS ROMs:
MCM68A308P7 — MC6800 MIKbug/MINIbug ROM
MCM68A316EP91 — Universal Code Converter and Character Generator
MCM68A332P2 — Sine/Cosine Look-Up Table
MCM68364P35-3 — Log/Antilog Look-Up Table
MCM65516P43M — MC146805 Monitor Program

*To be introduced.
(Not all speed selections shown)

RAMs

MOS DYNAMIC RAMs

Organization	Part Number	Access Time (ns max)	Power Supplies	No. of Pins
4096 × 1	MCM4027AC-2	150	+ 12, ± 5 V	16
4096 × 1	MCM4027AC-3	200	+ 12, ± 5 V	16
4096 × 1	MCM4027AC-4	250	+ 12, ± 5 V	16
16384 × 1	MCM4116BP15	150	+ 12, ± 5 V	16
16384 × 1	MCM4116BP20	200	+ 12, ± 5 V	16
16384 × 1	MCM4116BP25	250	+ 12, ± 5 V	16
16384 × 1	MCM4517P10	100	+ 5 V	16
16384 × 1	MCM4517P12	120	+ 5 V	16
16384 × 1	MCM4517P15	150	+ 5 V	16
16384 × 1	MCM4517P20	200	+ 5 V	16
32768 × 1	MCM6632AP15[1]	150	+ 5 V	16
32768 × 1	MCM6632AP20[1]	200	+ 5 V	16
32768 × 1	MCM6633AP15	150	+ 5 V	16
32768 × 1	MCM6633AP20	200	+ 5 V	16
65536 × 1	MCM6664AP12[1]	120	+ 5 V	16
65536 × 1	MCM6664AP15[1]	150	+ 5 V	16
65536 × 1	MCM6664AP20[1]	200	+ 5 V	16
65536 × 1	MCM6665AP12	120	+ 5 V	16
65536 × 1	MCM6665AP15	150	+ 5 V	16
65336 × 1	MCM6665AP20	200	+ 5 V	16

TTL BIPOLAR RAMs

Organization	Part Number	Access Time (ns max)	Output	No. of Pins
256 × 4	MCM93412	45	Open Collector	22
256 × 4	MCM93422*	45	3-State	22
256 × 4	MCM93L422*	60	3-State	22
1024 × 1	MCM93415	45	Open Collector	16
1024 × 1	MCM93425	45	3-State	16

See Notes on Page 1-2

MOS STATIC RAMs (+5 Volts)

Organization	Part Number	Access Time (ns max)	No. of Pins
128 × 8	MCM6810	450	24
128 × 8	MCM68A10	360	24
128 × 8	MCM68B10	250	24
1024 × 4	MCM2114P20	200	18
1024 × 4	MCM2114P25	250	18
1024 × 4	MCM2114P30	300	18
1024 × 4	MCM2114P45	450	18
1024 × 4	MCM21L14P20	200	18
1024 × 4	MCM21L14P25	250	18
1024 × 4	MCM21L14P30	300	18
1024 × 4	MCM21L14P45	450	18
1024 × 1	MCM2115AC45[2]	45	16
1024 × 1	MCM2115AC55[2]	55	16
1024 × 1	MCM2115AC70[2]	70	16
1024 × 1	MCM21L15AC45[2]	45	16
1024 × 1	MCM21L15AC70[2]	70	16
1024 × 1	MCM2125AC45	45	16
1024 × 1	MCM2125AC55	55	16
1024 × 1	MCM2125AC70	70	16
1024 × 1	MCM21L25AC45	45	16
1024 × 1	MCM21L25AC70	70	16
4096 × 1	MCM6641P20	200	18
4096 × 1	MCM6641P25	250	18
4096 × 1	MCM6641P30	300	18
4096 × 1	MCM6641P45	450	18
4096 × 1	MCM66L41P20	200	18
4096 × 1	MCM66L41P25	250	18
4096 × 1	MCM66L41P30	300	18
4096 × 1	MCM66L41P45	450	18
4096 × 1	MCM2147C55	55	18
4096 × 1	MCM2147C70	70	18
4096 × 1	MCM2147C85	85	18

CMOS STATIC RAMs (+5 Volts)

Organization	Part Number	Access Time (ns max)	No. of Pins
256 × 4	MCM5101P65	650	22
256 × 4	MCM5101P80	800	22
256 × 4	MCM51L01P45	450	22
256 × 4	MCM51L01P65	650	22
2048 × 8	MCM65116P15*	150	24
4096 × 1	MCM65147P55	55	18
4096 × 1	MCM65147P70	70	18

See Notes on Page 1-2

ECL BIPOLAR RAMs

Organization	Part Number	Access Time (ns max)	No. of Pins
8 × 2	MCM10143	15	24
256 × 1	MCM10144	26	16
16 × 4	MCM10145	15	16
1024 × 1	MCM10146	29	16
1024 × 1	MCM10146A*	15	16
128 × 1	MCM10147	15	16
64 × 1	MCM10148	15	16
256 × 1	MCM10152	15	16
4096 × 1	MCM10470	35	18
4096 × 1	MCM10470A*	20	18
1024 × 4	MCM10474*	25	24

EPROMs

MOS EPROMs

Organization	Part Number	Access Time (ns max)	Power Supplies	No. of Pins
1024 × 8	MCM2708C	450	+12, ±5 V	24
1024 × 8	MCM27A08C	300	+12, ±5 V	24
2048 × 8	TMS2716C	450	+12, ±5 V	24
2048 × 8	MCM2716C	450	+5 V	24
4096 × 8	MCM2532C	450	+5 V	24
8192 × 8	MCM68764C	450	+5 V	24
8192 × 8	MCM68766C	450	+5 V	24
8192 × 8	MCM68766C35	350	+5 V	24

EEPROMs

MOS EEPROM

Organization	Part Number	Access Time (ns max)	Power Supplies	No. of Pins
16 × 16	MCM2801P	10 μs	+5 V	14
32 × 32	MCM2802P*	15 μs	+5 V	14
2048 × 8	MCM2816P*	450 ns	+5 V	24
2048 × 8	MCM2817P*	150 ns	+5 V	28
4096 × 8	MCM2832P*	150 ns	+5 V	28

See Notes on Page 1-2

ROMs

MOS STATIC ROMs (+5 Volts)

Character Generators[3]

Organization	Part Number	Access Time (ns max)	No. of Pins
128 × (7 × 5)	MCM6670P	350	18
128 × (7 × 5)	MCM6674P	350	18
128 × (9 × 7)	MCM66700P	350	24
128 × (9 × 7)	MCM66710P	350	24
128 × (9 × 7)	MCM66714P	350	24
128 × (9 × 7)	MCM66720P	350	24
128 × (9 × 7)	MCM66730P	350	24
128 × (9 × 7)	MCM66734P	350	24
128 × (9 × 7)	MCM66740P	350	24
128 × (9 × 7)	MCM66750P	350	24
128 × (9 × 7)	MCM66760P	350	24
128 × (9 × 7)	MCM66770P	350	24
128 × (9 × 7)	MCM66780P	350	24
128 × (9 × 7)	MCM66790P	350	24

Binary ROMs (+5 Volts)

Organization	Part Number	Access Time (ns max)	No. of Pins
1024 × 8	MCM68A308P	350	24
1024 × 8	MCM68A308P7[4]	350	24
1024 × 8	MCM68B308P	250	24
2048 × 8	MCM68A316EP	350	24
2048 × 8	MCM68A316EP91[4]	350	24
4096 × 8	MCM68A332P	350	24
4096 × 8	MCM68A332P2[4]	350	24
8192 × 8	MCM68364P35	350	24
8192 × 8	MCM68364P35-3[4]	350	24
8192 × 8	MCM68364P20	250	24
8192 × 8	MCM68364P25	200	24
8192 × 8	MCM68365P25	250	24
8192 × 8	MCM68365P35	350	24
8192 × 8	MCM68366P25	250	24
8192 × 8	MCM68366P35	350	24

CMOS ROMs (+5 Volts)

Organization	Part Number	Access Time (ns max)	No. of Pins
256 × 4	MCM14524	1200	16
2048 × 8	MCM65516P43	430	18
2048 × 8	MCM65516P43M[4]	430	18
2048 × 8	MCM65516P55	550	18

See Notes on Page 1-2

PROMs

ECL PROMs

Organization	Part Number	Access Time (ns max)	No. of Pins
32 × 8	MCM10139	20	16
256 × 4	MCM10149	25	16

TTL PROMs

Organization	Part Number	Access Time (ns max)	Output	No. of Pins
512 × 4	MCM7621*	70	3-State	16
512 × 8	MCM7641*	70	3-State	24
1024 × 4	MCM7643	70	3-State	18
1024 × 8	MCM7681	70	3-State	24
2048 × 4	MCM7685	70	3-State	18
2048 × 8	MCM76161*	70	3-State	24

See Notes on Page 1-2

STANDARD MEMORY SYSTEMS

Motorola Memory Systems offers a variety of standard add-in memory modules to support LSI, PDP, VAX, UNIBUS, and MULTIBUS architectures. Many of these systems offer parity options and depopulated configurations. Some systems have EDAC for detecting and correcting erroneous data. Fast read access times are featured in all systems for compatibility with the most popular and latest computer systems.

Board Selector Guide

Host Computer	Motorola Device	Organization*	Access Time Typ (ns)	Parity
LS-11/23, PDP-11/03	MMS1132N3128 MMS1132P3128 MMS1142N0016	128K × 16 128K × 18 16K × 16 CMOS RAMs	300 300 150	No Yes No
PDP-11/04 through PDP-11/60 (Uses HEX SPC Slot)	MMS1117-38PC MMS1117-48PC	64K × 18 64K × 18	300 350	Yes Yes
PDP-11/04, PDP-11/34 (Modified UNIBUS Compatible)	MMS1128P3064 MMS1128P3096	64K × 18 96K × 18	300 300	Yes Yes
PDP-11/04, PDP-11/24 PDP-11/34 (Modified and Extended UNIBUS Compatible)	MMS1119P3128 MMS1119P4128	128K × 18 128K × 18	300 350	Yes Yes
PDP-11/44	MMS1129E4512	1 Mbyte with EDAC (Error Detection and Correction)	350	No
PDP-11/70	MMS1170E1064	256 Kbyte***	**	No
VAX-11/750	MMS750AE1064 MMS750BE1256	256 Kbyte*** 1 Mbyte***	** **	No No
VAX-11/780	MMS780AE1032	256 Kbyte***	**	No
SBC 80/–, SBC 86/– (MULTIBUS Compatible)	MMS8512E MMS8256E	512 Kbyte (with EDAC) 256 Kbyte (with EDAC)	350 350	No No
EXORmacs, VERSAmodule	MMS68KE4512	512 Kbyte (with EDAC)	350	No

LSI, PDP, VAX, and UNIBUS are trademarks of Digital Equipment Corp.
MULTIBUS is a trademark of Intel.
*Only the most popular versions are listed. Depopulated models are also available in most series.
**Access Time is a function of DEC controller as well as listed array card.
***These cards support EDAC. Actual circuitry is on DEC controller board.

CUSTOM MEMORY SYSTEMS

Motorola Memory Systems has the engineering expertise necessary to support numerous applications, ranging from industrial machine control to geophysical exploration. Designs are made to customer specifications. User-defined evaluations are performed in addition to Memory Systems' standard testing procedures.

The design engineering group has over 100 man years of experience, including the thorough knowledge of semiconductor technology that is a must when designing complete systems. State-of-the-art techniques are implemented when a system is being constructed. Interleaving and block transferring are used to enhance overall system performance. Memory Systems designers are specialists at incorporating Error Detection and Correction (EDAC) to improve reliability and increase Mean Time Between Failure (MTBF). Sophisticated computer aided design equipment enhances layout of the printed circuit boards and dense memory arrays.

The circuit boards are partially assembled using automatic insertion equipment, lowering the burden on the assembly line.

Quality Assurance is intense at every stage of production. Every product is thoroughly tested and evaluated by computer-controlled test equipment, and must meet customer specifications or be rejected.

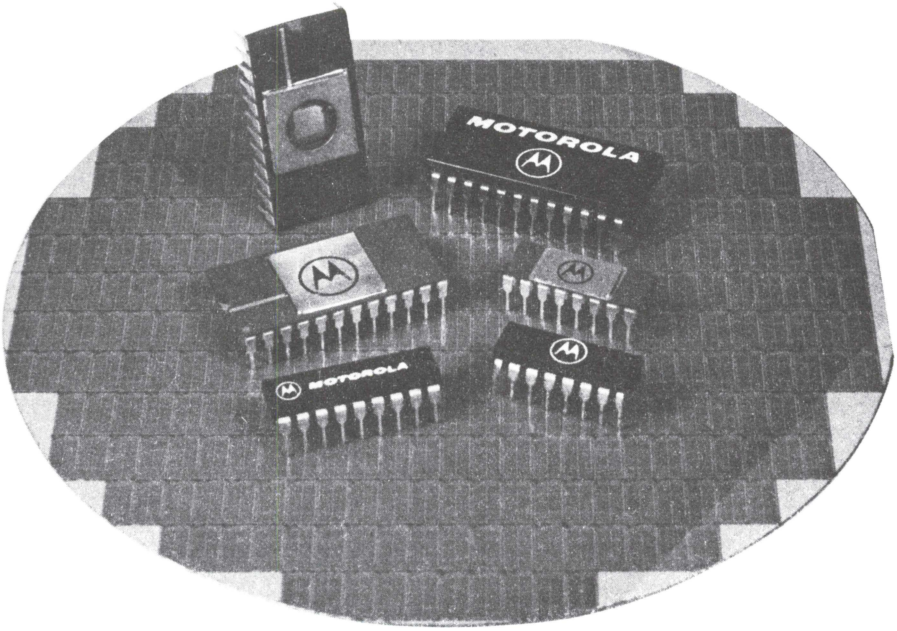
The customer's satisfaction is the number one priority of Motorola Memory Systems. On-time customer delivery is stressed. A computerized inventory control system provides constant data on product availability. Highly trained field service personnel and the product engineering staff are always available for customer assistance. Motorola Representatives and Systems Engineers are located nationwide to assist our customers.

For more information on custom memory systems...

CALL TOLL FREE
1-800-531-5118
(512-928-6776 in Texas)

OR WRITE
Motorola Memory Systems
Marketing Dept. V1230
3501 Ed Bluestein Blvd.
Austin, Texas 78721

MOS Dynamic RAM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MCM4027A

MOS

(N-CHANNEL, SILICON-GATE)

4096-BIT DYNAMIC RANDOM ACCESS MEMORY

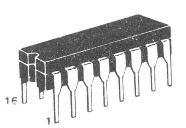
4096-BIT DYNAMIC RANDOM ACCESS MEMORY

The MCM4027A is a 4096 x 1 bit high-speed dynamic Random Access Memory. It has smaller die size than the MCM4027 providing improved speed selections. The MCM4027A is fabricated using Motorola's highly reliable N-channel silicon-gate technology.

By multiplexing row and column address inputs, the MCM4027A requires only six address lines and permits packaging in Motorola's standard 16-pin dual-in-line packages. Complete address decoding is done on chip with address latches incorporated.

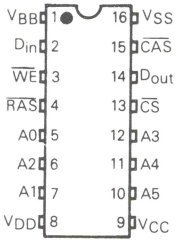
All inputs are TTL compatible, and the output is 3-state TTL compatible. The MCM4027A incorporates a one-transistor cell design and dynamic storage techniques, with each of the 64 row addresses requiring a refresh cycle every 2.0 milliseconds.

- Maximum Access Time = 120 ns – MCM4027AC1
  150 ns – MCM4027AC2
  200 ns – MCM4027AC3
  250 ns – MCM4027AC4
- Maximum Read and Write Cycle Time =
  320 ns – MCM4027AC1, C2
  375 ns – MCM4027AC3, C4
- Low Power Dissipation – 470 mW Max (Active)
  27 mW Max (Standby)
- 3-State Output for OR-Ties
- On-Chip Latches for Address, Chip Select, and Data In
- Power Supply Pins on Package Corners for Optimum Layout
- Industry Standard 16-Pin Package
- Page-Mode Capability
- Compatible with the Popular 2104/MK4096/MCM6604
- Second Source for MK4027



C SUFFIX
FRIT-SEAL CERAMIC PACKAGE
CASE 620

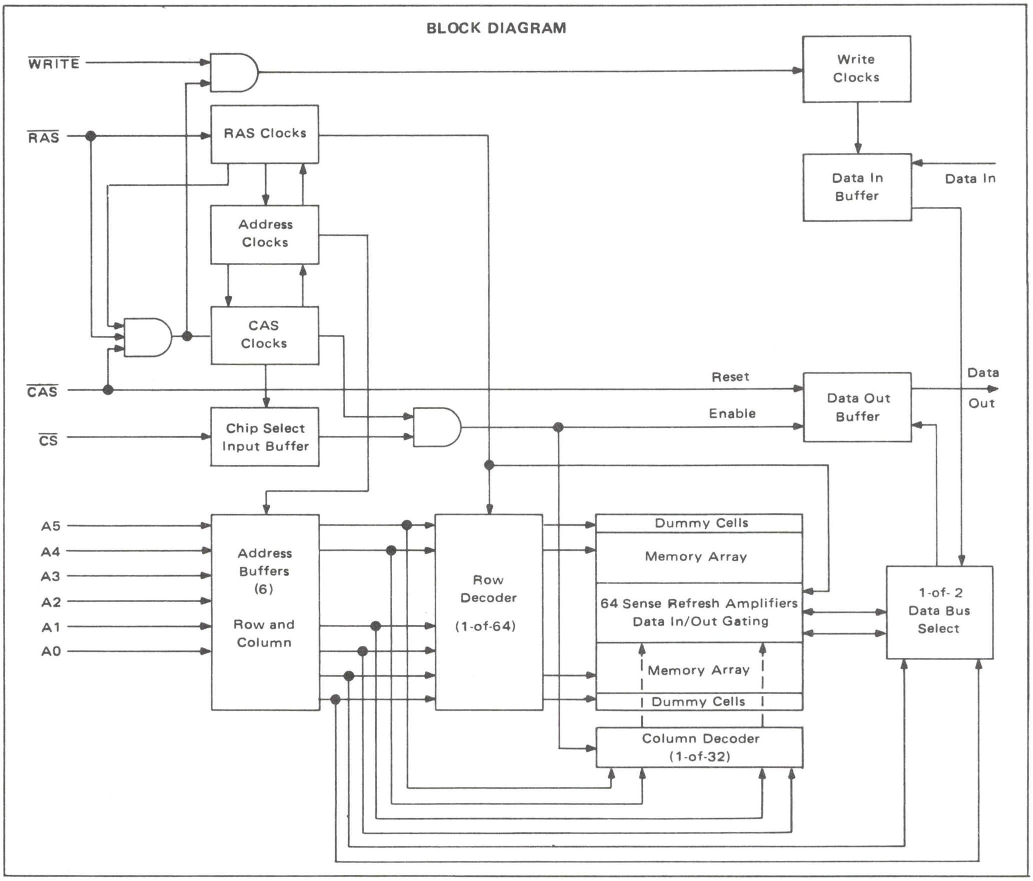
PIN ASSIGNMENT



TRUTH TABLE

Inputs				Data Out			Cycle Power	Ref	Function
$\overline{RAS}$	$\overline{CAS}$	$\overline{CS}$	$\overline{WE}$	Previous	Interim	Present			
L	L	L	L	Valid data	High Imp.	Input data	Full-operating	Yes	Write cycle
L	L	L	H	Valid data	High Imp.	Valid data (cell)	Full-operating	Yes	Read cycle
L	L	H	X	Valid data	High Imp.	High Imp.	Full-operating	Yes	Deselected-refresh
L	H	X	X	Valid data	Valid data	Valid data	Reduced operating	Yes	$\overline{RAS}$ only-refresh
H	L	X	X	Valid data	High Imp.	High Imp.	Standby	No	Standby-output disabled
H	H	X	X	Valid data	Valid data	Valid data	Standby	No	Standby-output valid

H = High, L = Low, X = Don't Care



BLOCK DIAGRAM

$\overline{\text{WRITE}}$
$\overline{\text{RAS}}$
$\overline{\text{CAS}}$
$\overline{\text{CS}}$
A5
A4
A3
A2
A1
A0
RAS Clocks
Address Clocks
CAS Clocks
Chip Select Input Buffer
Address Buffers (6) Row and Column
Row Decoder (1-of-64)
Write Clocks
Data In Buffer
Data In
Reset
Enable
Data Out Buffer
Data Out
Dummy Cells
Memory Array
64 Sense Refresh Amplifiers Data In/Out Gating
Memory Array
Dummy Cells
Column Decoder (1-of-32)
1-of-2 Data Bus Select

OPERATING CHARACTERISTICS

ADDRESSING

The MCM4027A has six address inputs (A0—A5) and two clock signals designated Row Address Strobe ($\overline{\text{RAS}}$) and Column Address Strobe ($\overline{\text{CAS}}$). At the beginning of a memory cycle, the six low order address bits A0 through A5 are strobed into the chip with $\overline{\text{RAS}}$ to select one of the 64 rows. The row address strobe also initiates the timing that will enable the 64 column sense amplifiers. After a specified hold time, the row address is removed and the six high order address bits (A6—A11) are placed on the address pins. This address is then strobed into the chip with $\overline{\text{CAS}}$. Two of the 64 column sense amplifiers are selected by A1 through A5. A one of two data bus select is accomplished by A0 to complete the data selection. The Chip Select ($\overline{\text{CS}}$) is latched into the port along with the column addresses.

DATA OUTPUT

In order to simplify the memory system designed and reduce the total package count, the MCM4027A contains an input data latch and a buffered output data latch. The state of the output latch and buffer at the end of a memory cycle will depend on the type of memory cycle performed and whether the chip is selected or unselected for that memory cycle.

A chip will be unselected during a memory cycle if:

(1) The chip receives both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ signals, but no $\overline{\text{Chip Select}}$ signal.

(2) The chip receives a $\overline{\text{CAS}}$ signal but no $\overline{\text{RAS}}$ signal. With this condition, the chip will be unselected regardless of the state of $\overline{\text{Chip Select}}$ input.

If, during a read, write, or read-modify-write cycle, the chip is unselected, the output buffer will be in the high impedance state at the end of the memory cycle. The output buffer will remain in the high impedance state until the chip is selected for a memory cycle.

For a chip to be selected during a memory cycle, it must receive the following signals: $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and $\overline{\text{Chip Select}}$. The state of the output latch and buffer of a selected chip during the following type of memory cycles would be:

(1) Read Cycle – On the negative edge of $\overline{\text{CAS}}$, the output buffer will unconditionally go to a high impedance state. It will remain in this state until access time. At this time, the output latch and buffer will assume the logic state of the data read from the selected cell. This output state will be maintained until the chip receives the next $\overline{\text{CAS}}$ signal.

(2) Write Cycle – If the $\overline{\text{WE}}$ input is switched to a logic 0 before the $\overline{\text{CAS}}$ transition, the output latch and buffer will be switched to the state of the data input at the end of the access time. This logic state will be maintained until the chip receives the next $\overline{\text{CAS}}$ signal.

(3) Read-Modify-Write – Same as read cycle.

DATA INPUT

Data to be written into a selected storage cell of the memory chip is first stored in the on-chip data latch. The gating of this latch is performed with a combination of the $\overline{\text{WE}}$ and $\overline{\text{CAS}}$ signals. The last of these signals to make a negative transition will strobe the data into the latch. If the $\overline{\text{WE}}$ input is switching to a logic 0 in the beginning of a write cycle, the falling edge of $\overline{\text{CAS}}$ strobes the data into the latch. The data setup and hold times are then referenced to the negative edge of $\overline{\text{CAS}}$.

If a read-modify-write cycle is being performed, the $\overline{\text{WE}}$ input would not make its negative transistion until after the $\overline{\text{CAS}}$ signal was enabled. Thus, the data would not be strobed into the latch until the negative transistion of $\overline{\text{WE}}$. The data setup and hold times would now be referenced to the negative edge of the $\overline{\text{WE}}$ signal. The only other timing constraints for a write-type-cycle is that both the $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ signals remain in the logic 0 state for a sufficient time to accomplish the permanent storage of the data into the selected cell.

INPUT/OUTPUT LEVELS

All of the inputs to the MCM4027A are TTL-compatible, featuring high impedance and low capacitance (5 to 7 pF). The three-state data output buffer is TTL-compatible and has sufficient current sink capability (3.2 mA) to drive two TTL loads. The output buffer also has a separate V_{CC} pin so that it can be powered from the same supply as the logic being employed.

REFRESH

In order to maintain valid data, each of the 64 internal rows of the MCM4027A must be refreshed once every 2 ms. Any cycle in which a $\overline{\text{RAS}}$ signal occurs accomplishes a refresh operation. Any read, write, or read-modify-write cycle will refresh an entire internally selected row. However, if a write or read-modify-write cycle is used to perform a refresh cycle the chip must be deselected to prevent writing data into the selected cell. The memory can also be refreshed by employing only the $\overline{\text{RAS}}$ cycle. This refresh mode will not shorten the refresh cycle time; however, the system standby power can be reduced by approximately 30%.

If the $\overline{\text{RAS}}$ only refresh cycles are employed for an extended length of time, the output buffer may eventually lose data and assume the high impedance state. Applying $\overline{\text{CAS}}$ to the chip will restore activity of the output buffer.

POWER DISSIPATION

Since the MCM4027A is a dynamic RAM, its power drain will be extremely small during the time the chip is unselected.

The power increases when the chip is selected and most of this increase is encountered on the address strobe edge. The circuitry of the MCM4027A is largely dynamic so power is not drawn during the whole time the strobe is active. Thus the dynamic power is a function of the operating frequency rather than the active duty cycle.

In a memory system, the $\overline{\text{CAS}}$ signal must be supplied to all the memory chips to ensure that the outputs of the unselected chips are switched to the high impedance state. Those chips that do not receive a $\overline{\text{RAS}}$ signal will not dissipate any power on the $\overline{\text{CAS}}$ edge except for that required to turn off the chip outputs. Thus, in order to ensure minimum system power, the $\overline{\text{RAS}}$ signal should be decoded so that only the chips to be selected receive a $\overline{\text{RAS}}$ signal. If the $\overline{\text{RAS}}$ signal is decoded, then the chip select input of all the chips can be set to a logic 0 state.

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DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS} = Ground.)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	V_{DD}	10.8	12.0	13.2	Vdc	2
	V_{CC}	V_{SS}	5.0	V_{DD}	Vdc	3
	V_{SS}	0	0	0	Vdc	2
	V_{BB}	-4.5	-5.0	-5.5	Vdc	2
Logic 1 Voltage, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WRITE}}$	V_{IHC}	2.4	5.0	7.0	Vdc	2, 4
Logic 1 Voltage, all inputs except $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WRITE}}$	V_{IH}	2.2	5.0	7.0	Vdc	2, 4
Logic 0 Voltage, all inputs	V_{IL}	-1.0	0	0.8	Vdc	2, 4

DC CHARACTERISTICS (V_{DD} = 12 V ± 10%, V_{CC} = 5.0 V ± 10%, V_{BB} = -5.0 V ± 10%, V_{SS} = 0 V, T_A = 0 to 70°C.) Notes 1, 5

Characteristic	Symbol	Min	Typ	Max	Units	Notes
Average V_{DD} Power Supply Current	I_{DD1}			35	mA	6
V_{CC} Power Supply Current	I_{CC}				mA	7
Average V_{BB} Power Supply Current	I_{BB}			250	µA	
Standby V_{DD} Power Supply Current	I_{DD2}			2	mA	9
Average V_{DD} Power Supply Current during "$\overline{\text{RAS}}$ only" cycles	I_{DD3}			25	mA	6
Input Leakage Current (any input)	$I_{I(L)}$			10	µA	8
Output Leakage Current	$I_{O(L)}$			10	µA	9, 10
Output Logic 1 Voltage @ I_{out} = -5 mA	V_{OH}	2.4			Vdc	
Output Logic 0 Voltage @ I_{out} = 3.2 mA	V_{OL}			0.4	Vdc	

NOTES 1 through 11:

1. T_A is specified for operation at frequencies to $t_{RC} \geqslant t_{RC}$(min). Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible provided that all ac parameters are met.

2. All voltages referenced to V_{SS}.

3. Output voltage will swing from V_{SS} to V_{CC} when enabled, with no output load. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH}(min) specification is not guaranteed in this mode.

4. Device speed is not guaranteed at input voltages greater than TTL levels (0 to 5 v).

5. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.

6. Current is proportional to cycle rate. I_{DD1}(max) is measured at the cycle rate specified by t_{RC}(min).

7. I_{CC} depends on output loading. During readout of high level data V_{CC} is connected through a low impedance (135 Ω typ) to Data Out. At all other times I_{CC} consists of leakage currents only.

8. All device pins at 0 volts except V_{BB} which is at −5 volts and the pin under test which is at +10 volts.

9. Output is disabled (high-impedance) and $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are both at a logic 1. Transient stabilization is required prior to measurement of this parameter.

10. $0\text{ V} \leqslant V_{Out} \leqslant +10\text{ V}$.

11. Effective capacitance is calculated from the equation:

$$C = \frac{\Delta Q}{\Delta V} \text{ with } \Delta V = 3 \text{ volts.}$$

EFFECTIVE CAPACITANCE (Full operating voltage and temperature range, periodically sampled rather than 100% tested) Note 11

Characteristic		Symbol	Max	Unit
Input Capacitance	(A0–A5), D_{in}, $\overline{\text{CS}}$	$C_{in(EFF)}$	5.0	pF
	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WRITE}}$		10.0	
Output Capacitance		$C_{out(EFF)}$	7.0	pF

ABSOLUTE MAXIMUM RATINGS (See Notes 1 and 2)

Rating	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{BB}*	V_{in}, V_{out}	-0.5 to +20	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Output Current (Short Circuit)	I_{out}	50	mAdc

* (V_{SS} - V_{BB} > 4.5 V)

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS ARE EXCEEDED. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability. V_{BB} must be applied prior to V_{CC} and V_{DD}. V_{BB} must also be the last power supply switched off.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

AC OPERATING CONDITIONS AND CHARACTERISTICS
(Read, Write, and Read-Modify-Write Cycles)

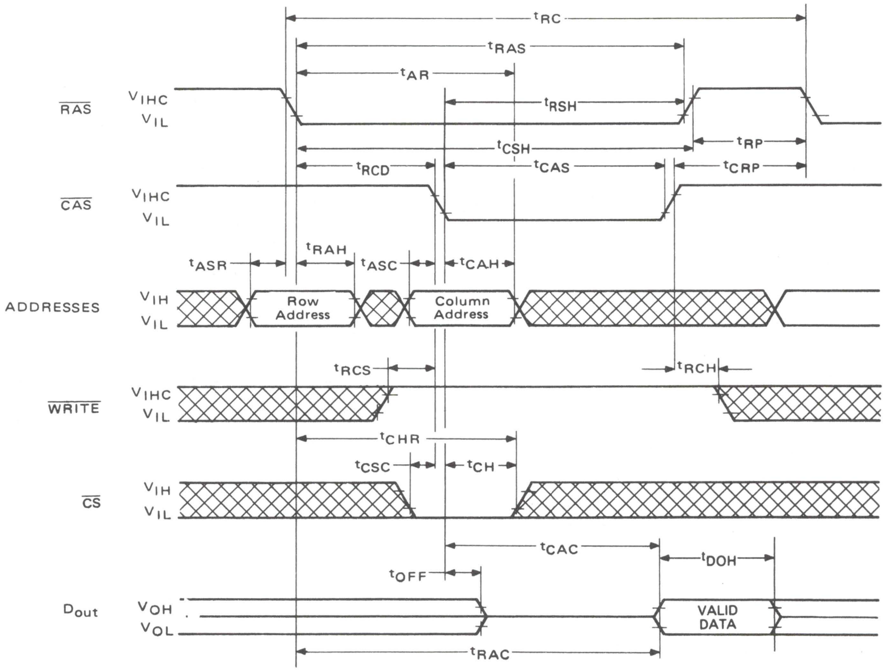
RECOMMENDED AC OPERATING CONDITIONS (V_{DD} = 12 V ± 10%, V_{CC} = 5.0 V ± 10%, V_{BB} = −5.0 V ± 10%, V_{SS} = 0 V, T_A = 0 to 70°C.) Notes 1, 5, 12, 18

Parameter	Symbol	MCM4027AC1		MCM4027AC2		MCM4027AC3		MCM4027AC4		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	320		320		375		375		ns	13
Read Write Cycle Time	t_{RWC}	320		320		375		375		ns	13
Page Mode Cycle Time	t_{PC}	160		170		225		285		ns	13
Access Time From Row Address Strobe	t_{RAC}		120		150		200		250	ns	14, 16
Access Time From Column Address Strobe	t_{CAC}		80		100		135		165	ns	15, 16
Output Buffer and Turn-Off Delay	t_{OFF}		35		40		50		60	ns	
Row Address Strobe Precharge Time	t_{RP}	100		100		120		120		ns	
Row Address Strobe Pulse Width	t_{RAS}	120	10,000	150	10,000	200	10,000	250	10,000	ns	
Row Address Strobe Hold Time	t_{RSH}	80		100		135		165		ns	
Column Address Strobe Pulse Width	t_{CAS}	80		100		135		165		ns	
Column Address Strobe Hold Time	t_{CSH}	120		150		200		250		ns	
Row to Column Strobe Lead Time	t_{RCD}	15	40	20	50	25	65	35	85	ns	17
Row Address Setup Time	t_{ASR}	0		0		0		0		ns	
Row Address Hold Time	t_{RAH}	15		20		25		35		ns	
Column Address Setup Time	t_{ASC}	-5		-10		-10		-10		ns	
Column Address Hold Time	t_{CAH}	40		45		55		75		ns	
Column Address Hold Time Referenced to $\overline{\text{RAS}}$	t_{AR}	80		95		120		160		ns	
Chip Select Setup Time	t_{CSC}	0		-10		-10		-10		ns	
Chip Select Hold Time	t_{CH}	40		45		55		75		ns	
Chip Select Hold Time Referenced to $\overline{\text{RAS}}$	t_{CHR}	80		95		120		160		ns	
Transition Time Rise and Fall	t_T	3	35	3	35	3	50	3	50	ns	18
Read Command Setup Time	t_{RCS}	0		0		0		0		ns	
Read Command Hold Time	t_{RCH}	0		0		0		0		ns	
Write Command Hold Time	t_{WCH}	40		45		55		75		ns	
Write Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{WCR}	80		95		120		160		ns	
Write Command Pulse Width	t_{WP}	40		45		55		75		ns	
Write Command to Row Strobe Lead Time	t_{RWL}	50		50		70		85		ns	
Write Command to Column Strobe Lead Time	t_{CWL}	50		50		70		85		ns	
Data in Setup Time	t_{DS}	0		0		0		0		ns	19
Data in Hold Time	t_{DH}	40		45		55		75		ns	19
Data in Hold Time Referenced to $\overline{\text{RAS}}$	t_{DHR}	80		95		120		160		ns	
Column to Row Strobe Precharge Time	t_{CRP}	0		0		0		0		ns	
Column Precharge Time	t_{CP}	60		60		80		110		ns	
Refresh Period	t_{RFSH}		2		2		2		2	ms	
Write Command Setup Time	t_{WCS}	0		0		0		0		ns	
$\overline{\text{CAS}}$ to $\overline{\text{WRITE}}$ Delay	t_{CWD}	60		60		80		90		ns	20
$\overline{\text{RAS}}$ to $\overline{\text{WRITE}}$ Delay	t_{RWD}	100		110		145		175		ns	20
Data Out Hold Time	t_{DOH}	10		10		10		10		µs	

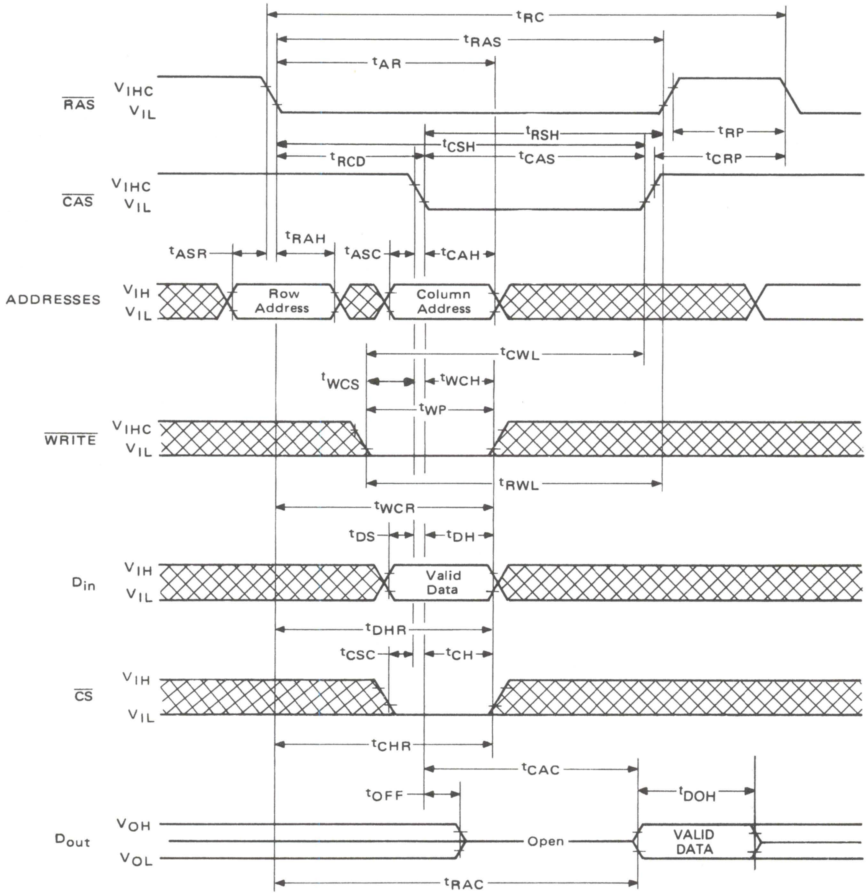
NOTES 12 through 20:

12. AC measurements assume t_T = 5 ns.
13. The specifications for t_{RC}(min) and t_{RWC}(min) are used only to indicate cycle time at which proper operation over the full temperature range ($0^{\circ}C \leqslant T_A \leqslant 70^{\circ}C$) is assured.
14. Assumes that $t_{RCD} \leqslant t_{RCD}$(max).
15. Assumes that $t_{RCD} \geqslant t_{RCD}$ (max).
16. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
17. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
18. V_{IHC}(min) or V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.
19. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in random write cycles and to $\overline{\text{WRITE}}$ leading edge in delayed write or read-modify write cycles.
20. t_{WCS}, t_{CWD}, and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characterisitcs only: If $t_{WCS} \geqslant t_{WCS}$(min), the cycle is an early write cycle and Data Out will contain the data written into the selected cell. If $t_{CWD} \geqslant t_{CWD}$(min) and $t_{RWD} \geqslant t_{RWD}$(min), the cycle is a read-write cycle and Data Out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of Data Out (at access time) is indeterminate.

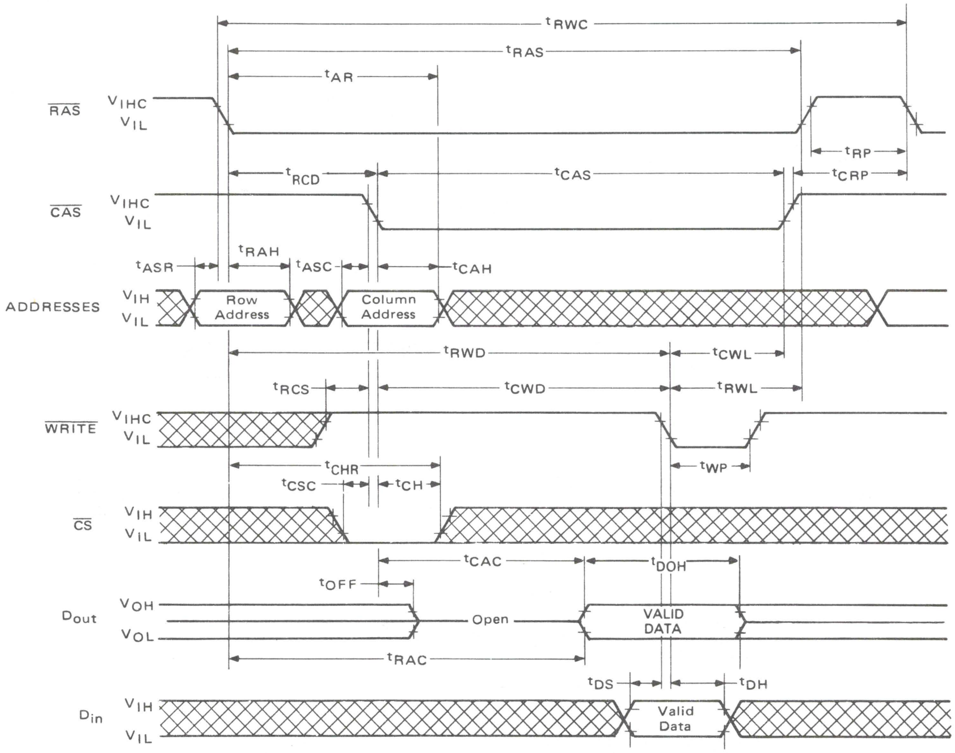
READ CYCLE TIMING


RAS
CAS
ADDRESSES
WRITE
CS
Dout
VIHC
VIL
VIH
VOH
VOL
tRC
tRAS
tAR
tRSH
tCSH
tRP
tRCD
tCAS
tCRP
tRAH
tASR
tASC
tCAH
Row Address
Column Address
tRCS
tRCH
tCHR
tCSC
tCH
tCAC
tDOH
tOFF
tRAC
VALID DATA

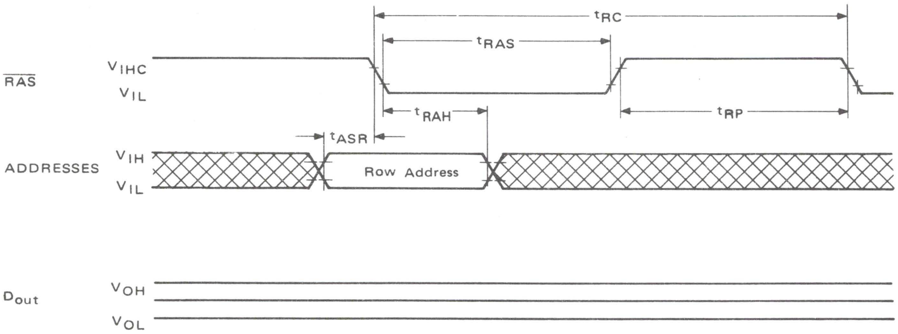
WRITE CYCLE TIMING


t_{RC}
t_{RAS}
t_{AR}
$\overline{RAS}$
V_{IHC}
V_{IL}
t_{RSH}
t_{CSH}
t_{RP}
t_{RCD}
t_{CAS}
t_{CRP}
$\overline{CAS}$
V_{IHC}
V_{IL}
t_{RAH}
t_{ASR}
t_{ASC}
t_{CAH}
ADDRESSES
V_{IH}
V_{IL}
Row Address
Column Address
t_{CWL}
t_{WCS}
t_{WCH}
t_{WP}
$\overline{WRITE}$
V_{IHC}
V_{IL}
t_{RWL}
t_{WCR}
t_{DS}
t_{DH}
D_{in}
V_{IH}
V_{IL}
Valid Data
t_{DHR}
t_{CSC}
t_{CH}
$\overline{CS}$
V_{IH}
V_{IL}
t_{CHR}
t_{CAC}
t_{OFF}
t_{DOH}
D_{out}
V_{OH}
V_{OL}
Open
VALID DATA
t_{RAC}

READ-MODIFY-WRITE TIMING


t_{RWC}
t_{RAS}
t_{AR}
$\overline{RAS}$
V_{IHC}
V_{IL}
t_{RP}
t_{RCD}
t_{CAS}
t_{CRP}
$\overline{CAS}$
V_{IHC}
V_{IL}
t_{RAH}
t_{ASR}
t_{ASC}
t_{CAH}
ADDRESSES
V_{IH}
V_{IL}
Row Address
Column Address
t_{RWD}
t_{CWL}
t_{RCS}
t_{CWD}
t_{RWL}
$\overline{WRITE}$
V_{IHC}
V_{IL}
t_{CHR}
t_{WP}
t_{CSC}
t_{CH}
$\overline{CS}$
V_{IH}
V_{IL}
t_{CAC}
t_{DOH}
t_{OFF}
D_{out}
V_{OH}
V_{OL}
Open
VALID DATA
t_{RAC}
t_{DS}
t_{DH}
D_{in}
V_{IH}
V_{IL}
Valid Data

$\overline{RAS}$ ONLY REFRESH TIMING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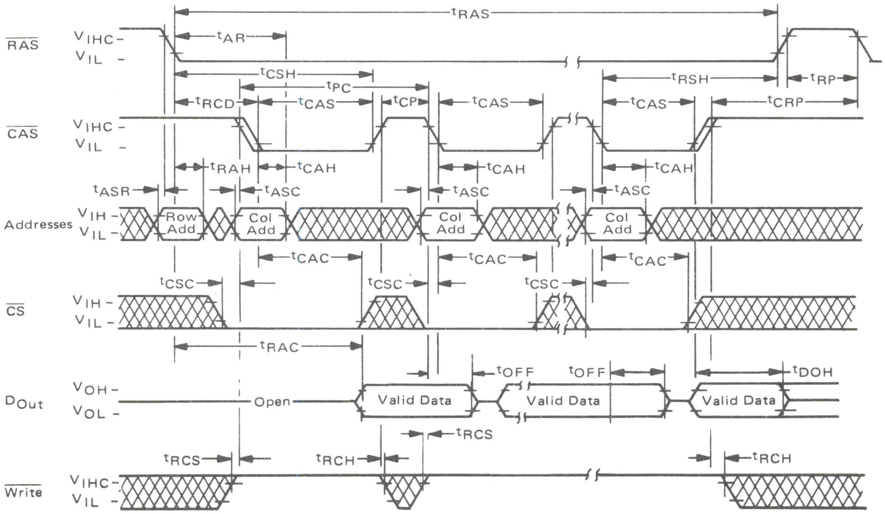
V_{IHC}
V_{IL}
t_{RAH}
t_{RP}
t_{ASR}
ADDRESSES
V_{IH}
V_{IL}
Row Address
D_{out}
V_{OH}
V_{OL}

PAGE MODE READ CYCLE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RAS
VIHC
VIL
tAR
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tPC
tRSH
tRP
tRCD
tCAS
tCP
tCRP
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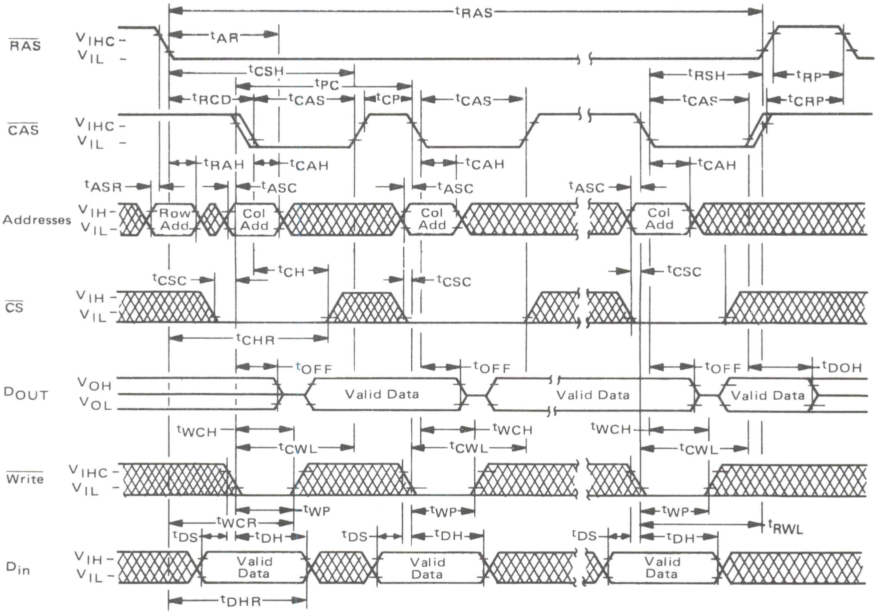
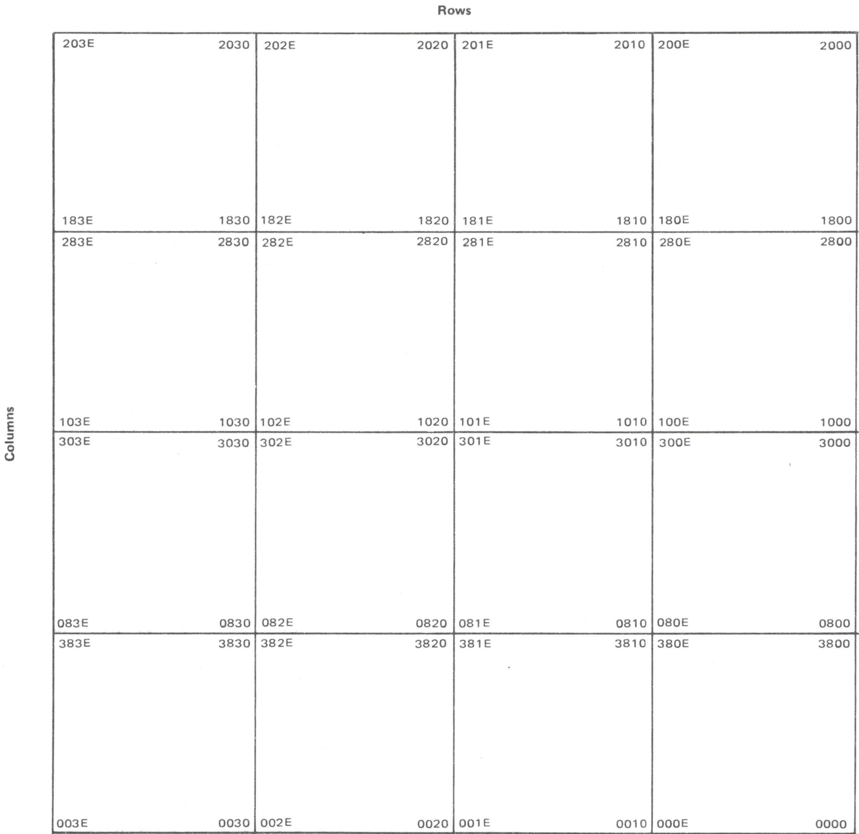
tCAH
tASR
tASC
Addresses
VIH
VIL
Row Add
Col Add
tCAC
tCSC
CS
tRAC
tOFF
tDOH
Dout
VOH
VOL
Open
Valid Data
tRCS
tRCH
Write

PAGE MODE WRITE CYCLE


tRAS
RAS
VIHC
VIL
tAR
tCSH
tPC
tRSH
tRP
tRCD
tCAS
tCP
tCRP
CAS
tRAH
tCAH
tASR
tASC
Addresses
VIH
VIL
Row Add
Col Add
tCH
tCSC
CS
tCHR
tOFF
tDOH
DOUT
VOH
VOL
Valid Data
tWCH
tCWL
Write
tWP
tWCR
tRWL
tDS
tDH
Din
Valid Data
tDHR

Row Address A5 A4 A3 A2 A1 A0
Column Address A5 A4 A3 A2 A1 A0


Rows
Columns
203E
2030
202E
2020
201E
2010
200E
2000
183E
1830
182E
1820
181E
1810
180E
1800
283E
2830
282E
2820
281E
2810
280E
2800
103E
1030
102E
1020
101E
1010
100E
1000
303E
3030
302E
3020
301E
3010
300E
3000
083E
0830
082E
0820
081E
0810
080E
0800
383E
3830
382E
3820
381E
3810
380E
3800
003E
0030
002E
0020
001E
0010
000E
0000

Column Addresses

A 5	A 4	A 3	A 2	A 1	A 0	Hex
H	L	L	L	L	L	20
H	L	L	L	L	H	21
L	H	H	H	H	H	1F
L	H	H	H	H	L	1E
H	L	L	L	H	L	22
H	L	L	L	H	H	23
L	H	H	H	L	H	1D
L	H	H	H	L	L	1C
H	L	L	H	L	L	24
H	L	L	H	L	H	25
L	H	H	L	H	H	1B
L	H	H	L	H	L	1A
H	L	L	H	H	L	26
H	L	L	H	H	H	27
L	H	H	L	L	H	19
L	H	H	L	L	L	18
H	L	H	L	L	L	28
H	L	H	L	L	H	29
L	H	L	H	H	H	17
L	H	L	H	H	L	16
H	L	H	L	H	L	2A
H	L	H	L	H	H	2B
L	H	L	H	L	H	15
L	H	L	H	L	L	14
H	L	H	H	L	L	2C
H	L	H	H	L	H	2D
L	H	L	L	H	H	13
L	H	L	L	H	L	12
H	L	H	H	H	L	2E
H	L	H	H	H	H	2F
L	H	L	L	L	H	11
L	H	L	L	L	L	10
H	H	L	L	L	L	30
H	H	L	L	L	H	31
L	L	H	H	H	H	0F
L	L	H	H	H	L	0E
H	H	L	L	H	L	32
H	H	L	L	H	H	33
L	L	H	H	L	H	0D
L	L	H	H	L	L	0C
H	H	L	H	L	L	34
H	H	L	H	L	H	35
L	L	H	L	H	H	0B
L	L	H	L	H	L	0A
H	H	L	H	H	L	36
H	H	L	H	H	H	37
L	L	H	L	L	H	09
L	L	H	L	L	L	08
H	H	H	L	L	L	38
H	H	H	L	L	H	39
L	L	L	H	H	H	07
L	L	L	H	H	L	06
H	H	H	L	H	L	3A
H	H	H	L	H	H	3B
L	L	L	H	L	H	05
L	L	L	H	L	L	04
H	H	H	H	L	L	3C
H	H	H	H	L	H	3D
L	L	L	L	H	H	03
L	L	L	L	H	L	02
H	H	H	H	H	L	3E
H	H	H	H	H	H	3F
L	L	L	L	L	H	01
L	L	L	L	L	L	00

Row Addresses

Hex	A 5	A 4	A 3	A 2	A 1	A 0
3E	H	H	H	H	H	L
3F					H	H
3D					L	H
3C				H	L	L
3A				L	H	L
3B					H	H
39					L	H
38			H	L	L	L
36			L	H	H	L
37					H	H
35					L	H
34				H	L	L
32				L	H	L
33					H	H
31					L	H
30		H	L	L	L	L
2E		L	H	H	H	L
2F					H	H
2D					L	H
2C				H	L	L
2A				L	H	L
2B					H	H
29					L	H
28			H	L	L	L
26			L	H	H	L
27					H	H
25					L	H
24				H	L	L
22				L	H	L
23					H	H
21					L	H
20	H	L	L	L	L	L
1E	L	H	H	H	H	L
1F					H	H
1D					L	H
1C				H	L	L
1A				L	H	L
1B					H	H
19					L	H
18			H	L	L	L
16			L	H	H	L
17					H	H
15					L	H
14				H	L	L
12				L	H	L
13					H	H
11					L	H
10		H	L	L	L	L
0E		L	H	H	H	L
0F					H	H
0D					L	H
0C				H	L	L
0A				L	H	L
0B					H	H
09					L	H
08			H	L	L	L
06	L	L	L	H	H	L
07	L	L	L	H	H	H
05	L	L	L	H	L	H
04	L	L	L	H	L	L
02	L	L	L	L	H	L
03	L	L	L	L	H	H
01	L	L	L	L	L	H
00	L	L	L	L	L	L

Pin 1

MCM4027A BIT ADDRESS MAP

MOTOROLA

MCM4116B

16,384-BIT DYNAMIC RANDOM ACCESS MEMORY

The MCM4116B is a 16,384-bit, high-speed dynamic Random Access Memory designed for high-performance, low-cost applications in mainframe and buffer memories and peripheral storage. Organized as 16,384 one-bit words and fabricated using Motorola's highly reliable N-channel double-polysilicon technology, this device optimizes speed, power, and density tradeoffs.

By multiplexing row and column address inputs, the MCM4116B requires only seven address lines and permits packaging in Motorola's standard 16-pin dual in-line packages. This packaging technique allows high system density and is compatible with widely available automated test and insertion equipment. Complete address decoding is done on chip with address latches incorporated.

All inputs are TTL compatible, and the output is 3-state TTL compatible. The data output of the MCM4116B is controlled by the column address strobe and remains valid from access time until the column address strobe returns to the high state. This output scheme allows higher degrees of system design flexibility such as common input/output operation and two dimensional memory selection by decoding both row address and column address strobes.

The MCM4116B incorporates a one-transistor cell design and dynamic storage techniques, with each of the 128 row addresses requiring a refresh cycle every 2 milliseconds.

- Flexible Timing with Read-Modify-Write, RAS-Only Refresh, and Page-Mode Capability
- Industry Standard 16-Pin Package
- 16,384 X 1 Organization
- ±10% Tolerance on All Power Supplies
- All Inputs are Fully TTL Compatible
- Three-State Fully TTL-Compatible Output
- Common I/O Capability When Using "Early Write" Mode
- On-Chip Latches for Addresses and Data In
- Low Power Dissipation — 463 mW Active, 20 mW Standby (Max)
- Fast Access Time Options:
  150 ns — MCM4116BP-15, BC-15
  200 ns — MCM4116BP-20, BC-20
  250 ns — MCM4116BP-25, BC-25
  300 ns — MCM4116BP-30, BC-30
- Easy Upgrade from 16-Pin 4K RAMs

ABSOLUTE MAXIMUM RATINGS (See Note)

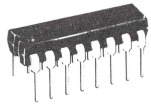
Rating	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{BB}	V_{in}, V_{out}	-0.5 to +20	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Power Dissipation	P_D	1.0	W
Data Out Current	I_{out}	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

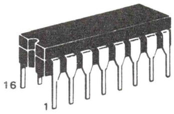
MOS

(N-CHANNEL)

16,384-BIT DYNAMIC
RANDOM ACCESS
MEMORY

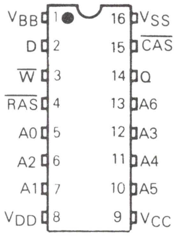


P SUFFIX
PLASTIC PACKAGE
CASE 648



C SUFFIX
FRIT-SEAL CERAMIC PACKAGE
CASE 620

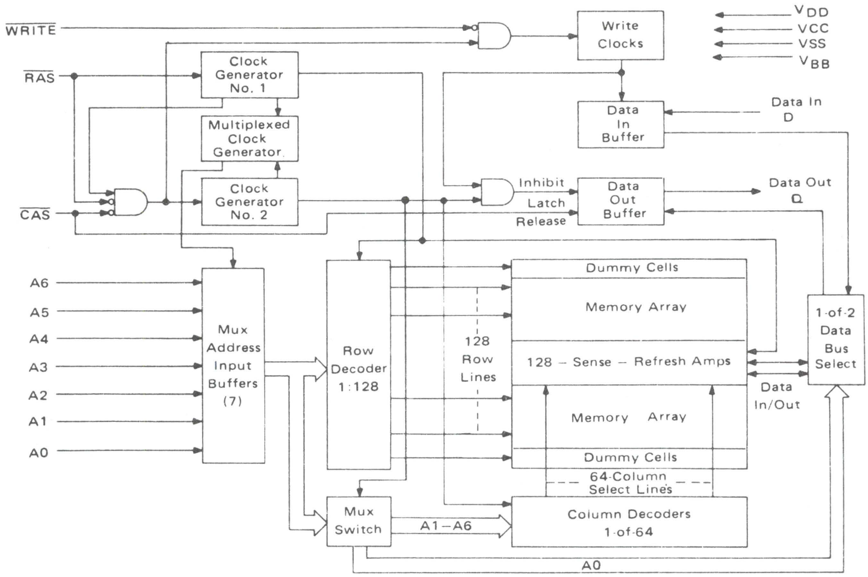
PIN ASSIGNMENT



PIN NAMES	
A0-A6	Address Inputs
$\overline{\text{CAS}}$	Column Address Strobe
D	Data In
Q	Data Out
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{W}}$	Read/Write Input
V_{BB}	Power (−5 V)
V_{CC}	Power (+5 V)
V_{DD}	Power (+12 V)
V_{SS}	Ground

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

BLOCK DIAGRAM


WRITE
RAS
CAS
Clock Generator No. 1
Multiplexed Clock Generator
Clock Generator No. 2
Write Clocks
VDD
VCC
VSS
VBB
Data In D
Data In Buffer
Inhibit
Latch Release
Data Out Buffer
Data Out Q
A6
A5
A4
A3
A2
A1
A0
Mux Address Input Buffers (7)
Row Decoder 1:128
128 Row Lines
Dummy Cells
Memory Array
128 – Sense – Refresh Amps
Memory Array
Dummy Cells
64-Column Select Lines
1-of-2 Data Bus Select
Data In/Out
Mux Switch
A1–A6
Column Decoders 1-of-64
A0

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	V_{DD}	10.8	12.0	13.2	V	1
	V_{CC}	4.5	5.0	5.5	V	1, 2
	V_{SS}	0	0	0	V	1
	V_{BB}	-4.5	-5.0	-5.5	V	1
Logic 1 Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IHC}	2.4	–	7.0	V	1
Logic 1 Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IH}	2.4	–	7.0	V	1
Logic 0 Voltage, all inputs	V_{IL}	-1.0	–	0.8	V	1

DC CHARACTERISTICS (V_{DD} = 12 V ± 10%, V_{CC} = 5.0 V ± 10%, V_{BB} = -5.0 V ± 10%, V_{SS} = 0 V, T_A = 0 to 70°C.)

Characteristic	Symbol	Min	Max	Units	Notes
Average V_{DD} Power Supply Current	I_{DD1}	–	35	mA	4
V_{CC} Power Supply Current	I_{CC}	–	–	mA	5
Average V_{BB} Power Supply Current	$I_{BB1,3}$	–	200	μA	
Standby V_{BB} Power Supply Current	I_{BB2}	–	100	μA	
Standby V_{DD} Power Supply Current	I_{DD2}	–	1.5	mA	6
Average V_{DD} Power Supply Current during "$\overline{RAS}$ only" cycles	I_{DD3}	–	27	mA	4
Input Leakage Current (any input)	$I_{I(L)}$	–	10	μA	
Output Leakage Current	$I_{O(L)}$	–	10	μA	6, 7
Output Logic 1 Voltage @ I_{out} = -5 mA	V_{OH}	2.4	–	V	2
Output Logic 0 Voltage @ I_{out} = 4.2 mA	V_{OL}	–	0.4	V	

NOTES:

1. All voltages referenced to V_{SS}. V_{BB} must be applied before and removed after other supply voltages.
2. Output voltage will swing from V_{SS} to V_{CC} under open circuit conditions. For purposes of maintaining data in power-down mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations. V_{OH}(min) specification is not guaranteed in this mode.
3. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate.
4. Current is proportional to cycle rate; maximum current is measured at the fastest cycle rate.
5. I_{CC} depends upon output loading. The V_{CC} supply is connected to the output buffer only.
6. Output is disabled (open-circuit) when $\overline{CAS}$ is at a logic 1.
7. 0 V $\leqslant V_{out} \leqslant$ +5.5 V.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, periodically sampled rather than 100% tested) (See Note 8)

Parameter	Symbol	Typ	Max	Unit	Notes
Input Capacitance (A0-A5), D_{in}	C_{I1}	4.0	5.0	pF	9
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	C_{I2}	8.0	10	pF	9
Output Capacitance (D_{out})	C_O	5.0	7.0	pF	7, 9

AC OPERATING CONDITIONS AND CHARACTERISTICS (See Notes 3, 9, 14)

READ, WRITE, AND READ-MODIFY-WRITE CYCLES

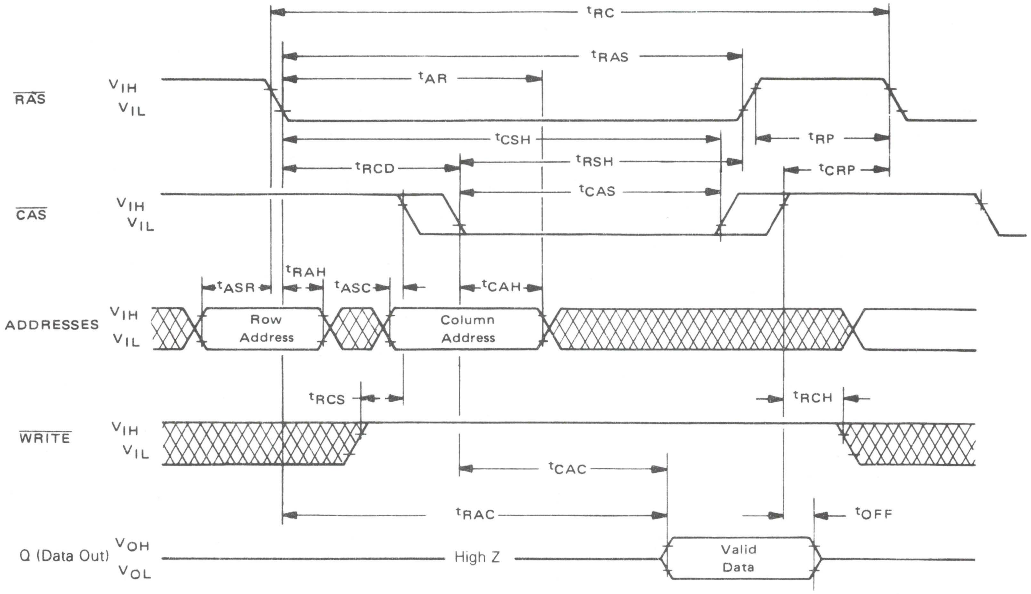
(V_{DD} = 12 V ± 10%, V_{CC} = 5.0 V ± 10%, V_{BB} = −5.0 V ± 10%, V_{SS} = 0 V, T_A = 0 to 70°C.)

		MCM4116B-15		MCM4116B-20		MCM4116B-25		MCM4116B-30			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
Random Read or Write Cycle Time	t_{RC}	375	–	375	–	410	–	480	–	ns	
Read Write Cycle Time	t_{RWC}	375	–	375	–	515	–	660	–	ns	
Access Time from Row Address Strobe	t_{RAC}	–	150	–	200	–	250	–	300	ns	10, 12
Access Time from Column Address Strobe	t_{CAC}	–	100	–	135	–	165	–	200	ns	11, 12
Output Buffer and Turn-off Delay	t_{OFF}	0	50	0	50	0	60	0	60	ns	17
Row Address Strobe Precharge Time	t_{RP}	100	–	120	–	150	–	180	–	ns	
Row Address Strobe Pulse Width	t_{RAS}	150	10,000	200	10,000	250	10,000	300	10,000	ns	
Column Address Strobe Pulse Width	t_{CAS}	100	10,000	135	10,000	165	10,000	200	10,000	ns	
Row to Column Strobe Lead Time	t_{RCD}	20	50	25	65	35	85	60	100	ns	13
Row Address Setup Time	t_{ASR}	0	–	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RAH}	20	–	25	–	35	–	60	–	ns	
Column Address Setup Time	t_{ASC}	−10	–	−10	–	−10	–	−10	–	ns	
Column Address Hold Time	t_{CAH}	45	–	55	–	75	–	100	–	ns	
Column Address Hold Time Referenced to $\overline{\text{RAS}}$	t_{AR}	95	–	120	–	160	–	200	–	ns	
Transition Time (Rise and Fall)	t_T	3.0	35	3.0	50	3.0	50	3.0	50	ns	14
Read Command Setup Time	t_{RCS}	0	–	0	–	0	–	0	–	ns	
Read Command Hold Time	t_{RCH}	0	–	0	–	0	–	0	–	ns	
Write Command Hold Time	t_{WCH}	45	–	55	–	75	–	100	–	ns	
Write Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{WCR}	95	–	120	–	160	–	200	–	ns	
Write Command Pulse Width	t_{WP}	45	–	55	–	75	–	100	–	ns	
Write Command to Row Strobe Lead Time	t_{RWL}	60	–	80	–	100	–	180	–	ns	
Write Command to Column Strobe Lead Time	t_{CWL}	60	–	80	–	100	–	180	–	ns	
Data in Setup Time	t_{DS}	0	–	0	–	0	–	0	–	ns	15
Data in Hold Time	t_{DH}	45	–	55	–	75	–	100	–	ns	15
Data in Hold Time Referenced to $\overline{\text{RAS}}$	t_{DHR}	95	–	120	–	160	–	200	–	ns	
Column to Row Strobe Precharge Time	t_{CRP}	−20	–	−20	–	−20	–	−20	–	ns	
$\overline{\text{RAS}}$ Hold Time	t_{RSH}	100	–	135	–	165	–	200	–	ns	
Refresh Period	t_{RFSH}	–	2.0	–	2.0	–	2.0	–	2.0	ms	
$\overline{\text{WRITE}}$ Command Setup Time	t_{WCS}	−20	–	−20	–	−20	–	−20	–	ns	
$\overline{\text{CAS}}$ to $\overline{\text{WRITE}}$ Delay	t_{CWD}	70	–	95	–	125	–	180	–	ns	16
$\overline{\text{RAS}}$ to $\overline{\text{WRITE}}$ Delay	t_{RWD}	120	–	160	–	210	–	280	–	ns	16
$\overline{\text{CAS}}$ Precharge Time (Page mode cycle only)	t_{CP}	60	–	80	–	100	–	100	–	ns	
Page Mode Cycle Time	t_{PC}	170	–	225	–	275	–	325	–	ns	
$\overline{\text{CAS}}$ Hold Time	t_{CSH}	150	–	200	–	250	–	300	–	ns	

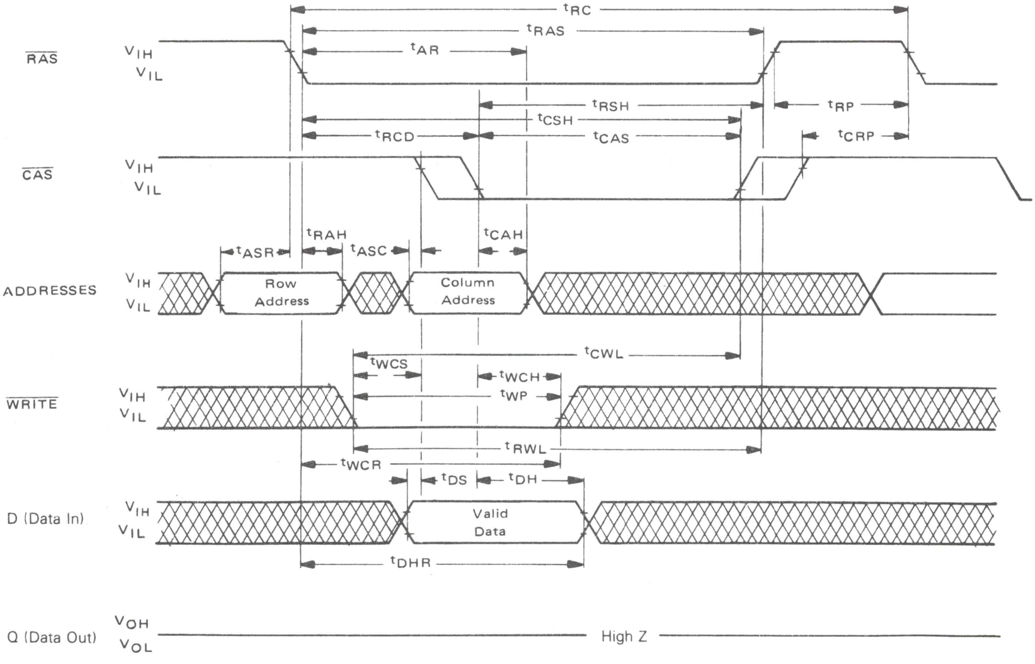
NOTES: (continued)

8. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = \frac{I\Delta_t}{\Delta V}$.
9. AC measurements assume t_T = 5.0 ns.
10. Assumes that $t_{RCD} + t_T \leqslant t_{RCD}$ (max).
11. Assumes that $t_{RCD} + t_T \geqslant t_{RCD}$ (max).
12. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
13. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
14. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transistion times are measured between V_{IHC} or V_{IH} and V_{IL}.
15. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in random write cycles and to $\overline{\text{WRITE}}$ leading edge in delayed write or read-modify-write cycles.
16. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: If $t_{WCS} \geqslant t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{CWD} \geqslant t_{CWD}$ (min) and $t_{RWD} \geqslant t_{RWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell; If neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
17. Assumes that $t_{CRP} > 50$ ns.

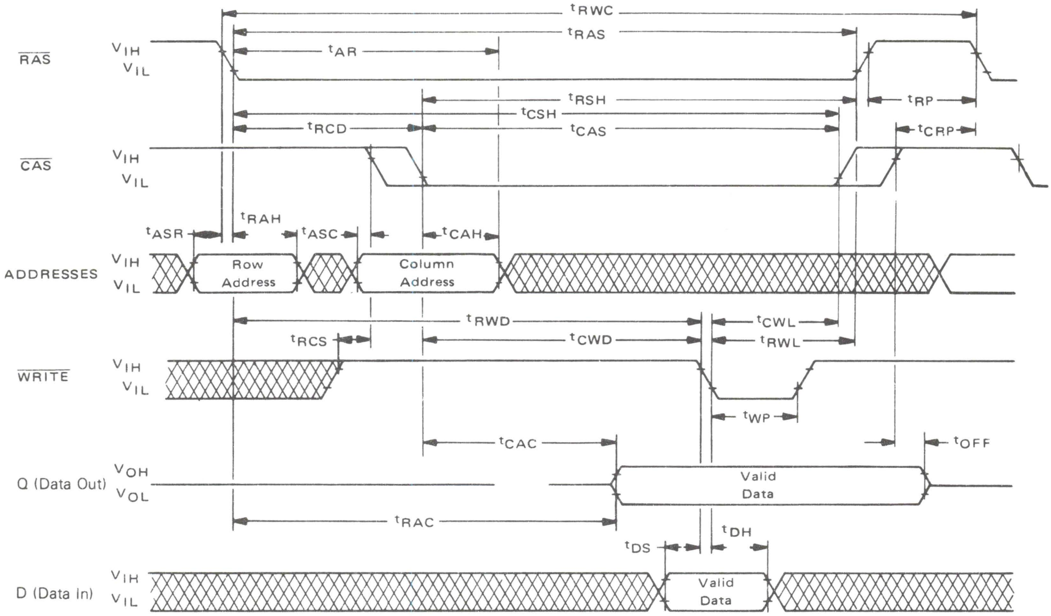
READ CYCLE TIMING


tRC
tRAS
tAR
RAS
VIH
VIL
tCSH
tRP
tRCD
tRSH
tCRP
tCAS
CAS
VIH
VIL
tRAH
tASR
tASC
tCAH
ADDRESSES
VIH
VIL
Row Address
Column Address
tRCS
tRCH
WRITE
VIH
VIL
tCAC
tRAC
tOFF
Q (Data Out)
VOH
VOL
High Z
Valid Data

WRITE CYCLE TIMING

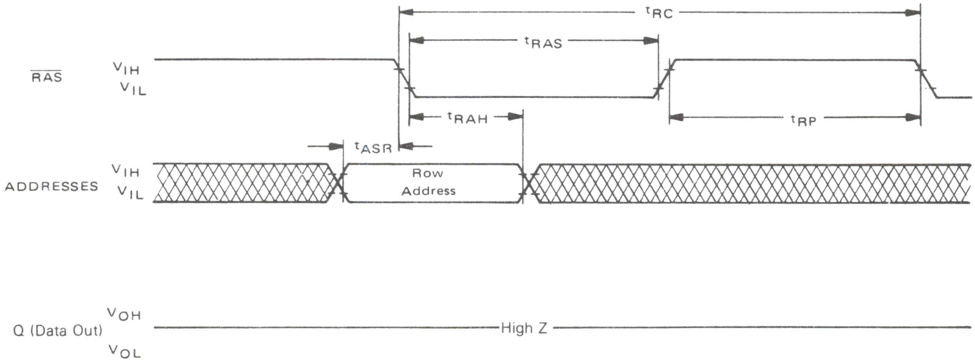

tRC
tRAS
tAR
RAS
VIH
VIL
tRSH
tRP
tCSH
tRCD
tCAS
tCRP
CAS
VIH
VIL
tRAH
tCAH
tASR
tASC
ADDRESSES
VIH
VIL
Row Address
Column Address
tCWL
tWCS
tWCH
tWP
WRITE
VIH
VIL
tRWL
tWCR
tDS
tDH
D (Data In)
VIH
VIL
Valid Data
tDHR
Q (Data Out)
VOH
VOL
High Z

READ-WRITE/READ-MODIFY-WRITE CYCLE

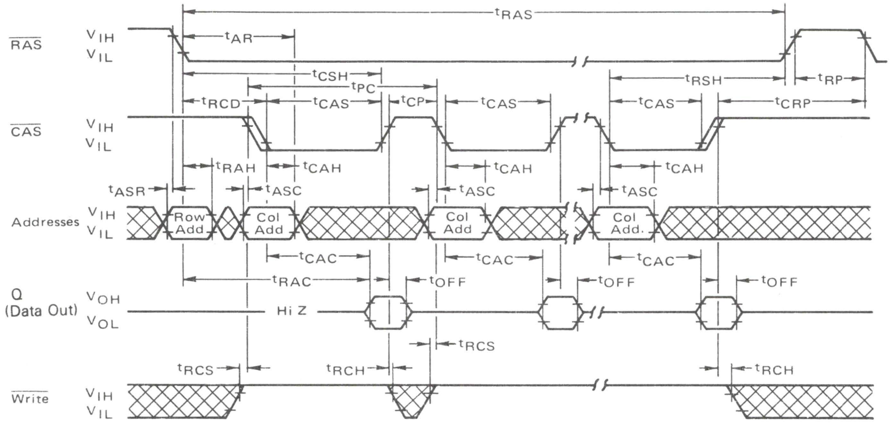

tRWC
tRAS
tAR
RAS
VIH
VIL
tRSH
tRP
tCSH
tRCD
tCAS
tCRP
CAS
VIH
VIL
tASR
tRAH
tASC
tCAH
ADDRESSES
VIH
VIL
Row Address
Column Address
tRWD
tCWL
tRCS
tCWD
tRWL
WRITE
VIH
VIL
tWP
tCAC
tOFF
Q (Data Out)
VOH
VOL
Valid Data
tRAC
tDH
tDS
D (Data In)
VIH
VIL
Valid Data

RAS ONLY REFRESH TIMING

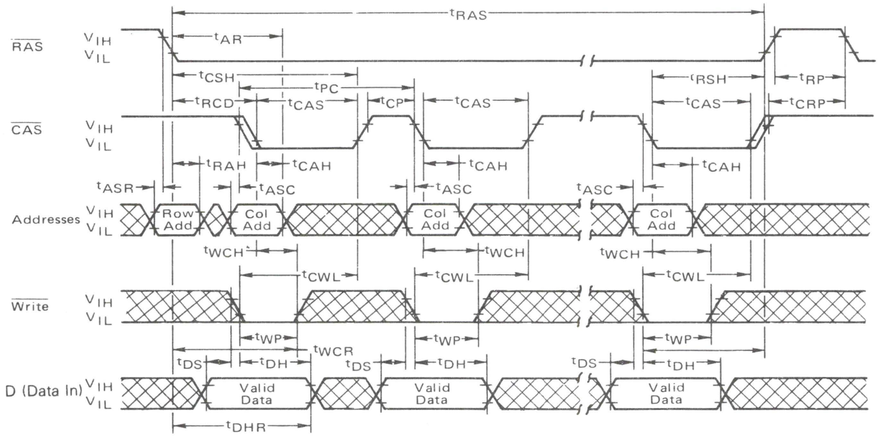
Note: $\overline{\text{CAS}}$ = V_{IHC}, $\overline{\text{WRITE}}$ = Don't Care


tRC
tRAS
RAS
VIH
VIL
tRAH
tRP
tASR
ADDRESSES
VIH
VIL
Row Address
Q (Data Out)
VOH
VOL
High Z

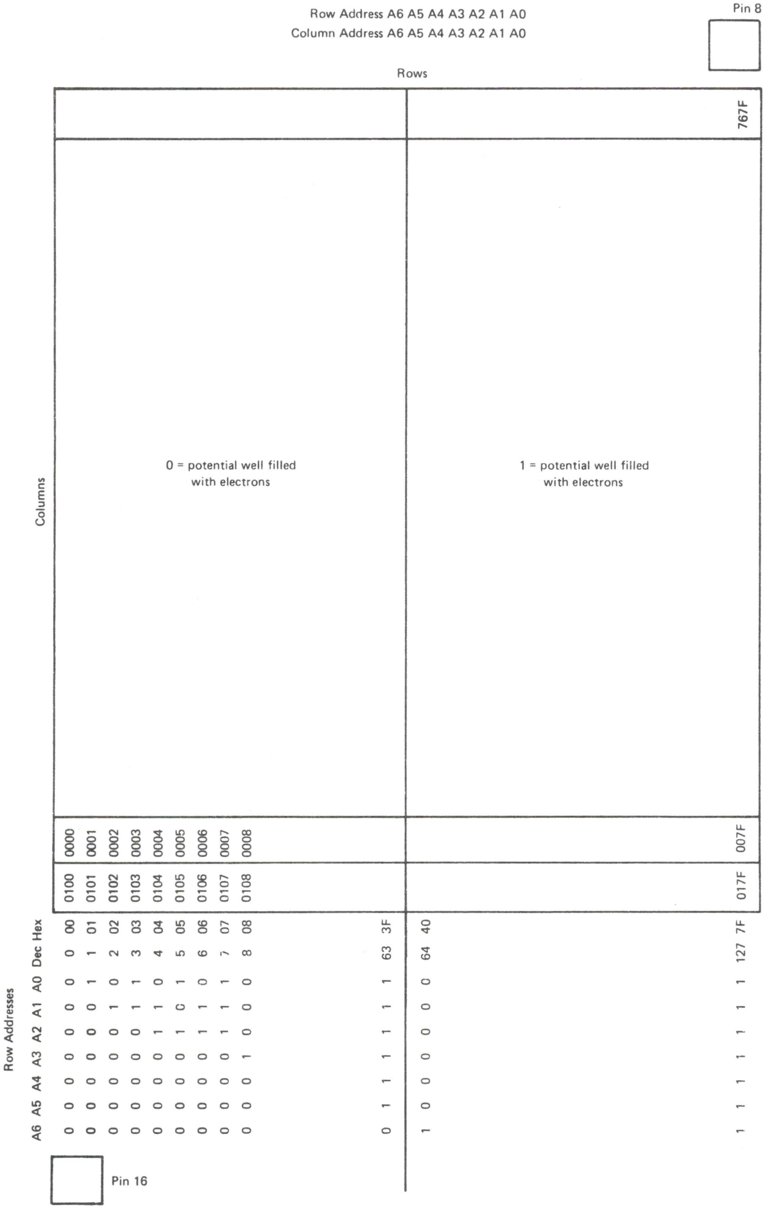
PAGE MODE READ CYCLE


tRAS
RAS
VIH
VIL
tAR
tCSH
tPC
tRSH
tRP
tRCD
tCAS
tCP
tCAS
tCAS
tCRP
CAS
VIH
VIL
tRAH
tCAH
tCAH
tCAH
tASR
tASC
tASC
tASC
Addresses
VIH
VIL
Row Add
Col Add
Col Add
Col Add.
tCAC
tCAC
tCAC
tRAC
tOFF
tOFF
tOFF
Q
(Data Out)
VOH
VOL
Hi Z
tRCS
tRCS
tRCH
tRCH
Write
VIH
VIL

PAGE MODE WRITE CYCLE


tRAS
RAS
VIH
VIL
tAR
tCSH
tPC
tRSH
tRP
tRCD
tCAS
tCP
tCAS
tCAS
tCRP
CAS
VIH
VIL
tRAH
tCAH
tCAH
tCAH
tASR
tASC
tASC
tASC
Addresses
VIH
VIL
Row Add
Col Add
Col Add
Col Add
tWCH
tWCH
tWCH
tCWL
tCWL
tCWL
Write
VIH
VIL
tWP
tWP
tWP
tWCR
tDS
tDH
tDS
tDH
tDS
tDH
D (Data In)
VIH
VIL
Valid Data
Valid Data
Valid Data
tDHR

MCM4116B BIT ADDRESS MAP


Row Address A6 A5 A4 A3 A2 A1 A0
Column Address A6 A5 A4 A3 A2 A1 A0
Rows
Pin 8
767F
Columns
0 = potential well filled with electrons
1 = potential well filled with electrons
0000 0001 0002 0003 0004 0005 0006 0007 0008
007F
0100 0101 0102 0103 0104 0105 0106 0107 0108
017F
Row Addresses
A6 A5 A4 A3 A2 A1 A0 Dec Hex
0 00
1 01
2 02
3 03
4 04
5 05
6 06
7 07
8 08
63 3F
64 40
127 7F
Pin 16

Column Addresses

Hex	Dec	A6	A5	A4	A3	A2	A1	A0
76	118	1	1	1	0	1	1	0
77	119	1	1	1	0	1	1	1
16	22	0	0	1	0	1	1	0
17	23	0	0	1	0	1	1	1
14	20	0	0	1	0	1	0	0
15	21	0	0	1	0	1	0	1
12	18	0	0	1	0	0	1	0
13	19	0	0	1	0	0	1	1
10	16	0	0	1	0	0	0	0
11	17	0	0	1	0	0	0	1
1E	30	0	0	1	1	1	1	0
1F	31	0	0	1	1	1	1	1
1C	28	0	0	1	1	1	0	0
1D	29	0	0	1	1	1	0	1
1A	26	0	0	1	1	0	1	0
1B	27	0	0	1	1	0	1	1
18	24	0	0	1	1	0	0	0
19	25	0	0	1	1	0	0	1
0E	14	0	0	0	1	1	1	0
0F	15	0	0	0	1	1	1	1
0C	12	0	0	0	1	1	0	0
0D	13	0	0	0	1	1	0	1
0A	10	0	0	0	1	0	1	0
0B	11	0	0	0	1	0	1	1
08	8	0	0	0	1	0	0	0
09	9	0	0	0	1	0	0	1
06	6	0	0	0	0	1	1	0
07	7	0	0	0	0	1	1	1
04	4	0	0	0	0	1	0	0
05	5	0	0	0	0	1	0	1
02	2	0	0	0	0	0	1	0
03	3	0	0	0	0	0	1	1
00	0	0	0	0	0	0	0	0
01	1	0	0	0	0	0	0	1

MOTOROLA

MCM4517

Advance Information

16,384-BIT DYNAMIC RAM

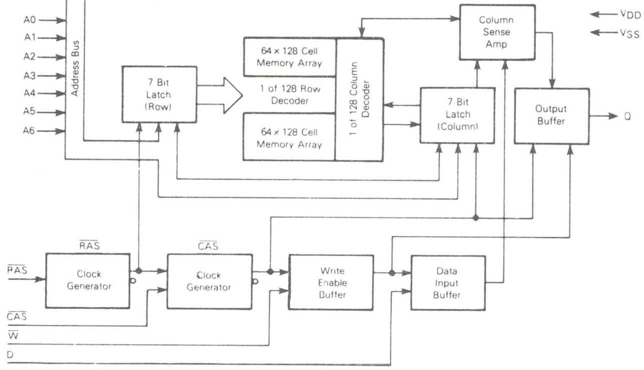
The MCM4517 is a 16,384-bit, high-speed, dynamic Random-Access Memory. Organized as 16,384 one-bit words and fabricated using HMOS high-performance, N-channel, silicon-gate technology. This new breed of 5-volt only dynamic RAM combines high performance with low cost and improved reliability.

By multiplexing row- and column-address inputs, the MCM4517 requires only seven address lines and permits packaging in standard 16-pin dual-in-line packages. Complete address decoding is done on chip with address latches incorporated. Data out is controlled by $\overline{\text{CAS}}$ allowing for greater system flexibility.

All inputs and outputs, including clocks, are fully TTL compatible. The MCM4517 incorporates a one-transistor cell design and dynamic storage techniques.

- Organized as 16,384 Words of 1 Bit
- Single +5 Volt Operation
- Fast 100 ns Operation
- Low Power Dissipation:
  170 mW Maximum (Active)
  14 mW Maximum (Standby)
- Maximum Access Time
  MCM4517-10 — 100 ns
  MCM4517-12 — 120 ns
  MCM4517-15 — 150 ns
  MCM4517-20 — 200 ns
- Three-State Data Output
- Internal Latches for Address and Data Input
- Early-Write Common I/O Output Capability
- 64K Compatible 128-cycle, 2 ms Refresh
- $\overline{\text{RAS}}$-only Refresh Mode
- $\overline{\text{CAS}}$ Controlled Output
- Upward Pin Compatibility from the 16K RAM (MCM4116) to the 64K RAM (MCM6664)
- Allows Undershoot V_{IL} min = −2 V
- Hidden $\overline{\text{RAS}}$ Only Refresh Capability

BLOCK DIAGRAM

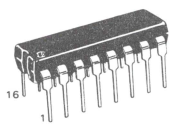

A0
A1
A2
A3
A4
A5
A6
Address Bus
7 Bit Latch (Row)
64 × 128 Cell Memory Array
1 of 128 Row Decoder
64 × 128 Cell Memory Array
1 of 128 Column Decoder
Column Sense Amp
7 Bit Latch (Column)
Output Buffer
Q
VDD
VSS
RAS
Clock Generator
CAS
Clock Generator
Write Enable Buffer
Data Input Buffer
RAS
CAS
W
D

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MOS

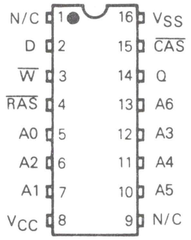
(N-CHANNEL, SILICON-GATE)

16,384-BIT
DYNAMIC RAM



P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT


N/C 1
D 2
W 3
RAS 4
A0 5
A2 6
A1 7
VCC 8
16 VSS
15 CAS
14 Q
13 A6
12 A3
11 A4
10 A5
9 N/C

PIN NAMES	
A0-A6	Address Input
D	Data In
Q	Data Out
$\overline{\text{W}}$	Read/Write Input
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
V_{CC}	Power (+5 V)
V_{SS}	Ground

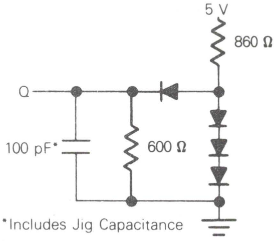
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_{in}, V_{out}	−2 to +7	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Power Dissipation	P_D	1.0	W
Data Out Current	I_{out}	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

FIGURE 1 — OUTPUT LOAD



*Includes Jig Capacitance

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full Operating Voltage and Temperature Range Unless Otherwise Noted.)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	V_{CC} V_{SS}	4.5 0	5.0 0	5.5 0	V	1
Logic 1 Voltage, All Inputs	V_{IH}	2.4	–	7.0	V	1
Logic 0 Voltage, All Inputs	V_{IL}	−2.0	–	0.8	V	1

DC CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Units	Notes
V_{CC} Supply Current (Standby)	I_{CC1}	–	1.8	2.5	mA	5
V_{CC} Supply Current (Operating)	I_{CC2}				mA	4
4517-10, $t_{RC}=235$		–	22	31		
4517-12, $t_{RC}=270$		–	20	28		
4517-15, $t_{RC}=320$		–	18	25		
4517-20, $t_{RC}=350$		–	16	23		
V_{CC} Supply Current (RAS-Only Cycle)	I_{CC3}				mA	4
4517-10, $t_{RC}=235$		–	14	23		
4517-12, $t_{RC}=270$		–	12	21		
4517-15, $t_{RC}=320$		–	11	19		
4517-20, $t_{RC}=350$		–	10	18		
V_{CC} Standby Current (Standby, Output Enable) ($\overline{CAS}$ at V_{IL}, $\overline{RAS}$ at V_{IH})	I_{CC4}	–	2	5	mA	
V_{CC} Supply Current (Page Mode Cycle Only)	I_{CC5}				mA	
4517-10, $t_{RC}=235$		–	17	23		
4517-12, $t_{RC}=270$		–	15	21		
4517-15, $t_{RC}=320$		–	13	18		
4517-20, $t_{RC}=350$		–	10	15		
Input Leakage Current (Any Input)	$I_{I(L)}$	–	–	10	μA	
Output Leakage Current ($0 \leq V_{out} \leq 5.5$) ($\overline{CAS}$ at Logic 1)	$I_{O(L)}$	–	–	10	μA	
Output Logic 1 Voltage@$I_{out}=-4$ mA	V_{OH}	2.4	–	–	V	
Output Logic 0 Voltage@$I_{out}=4$ mA	V_{OL}	–	–	0.4	V	

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full Operating Voltage and Temperature Range Unless Otherwise Noted)

(See Notes 2, 3, 9, 14 and Figure 1)

Parameter	Symbol	MCM4517-10		MCM4517-12		MCM4516-15		MCM4517-20		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	235	–	270	–	320	–	365	–	ns	8, 9
Read-Modify-Write Cycle Time	t_{RWC}	285	–	320	–	410	–	440	–	ns	8, 9
Access Time from Row Address Strobe	t_{RAC}	–	100	–	120	–	150	–	200	ns	10, 12
Access Time from Column Address Strobe	t_{CAC}	–	55	–	65	–	80	–	120	ns	11, 12
Output Buffer and Turn-Off Delay	t_{OFF}	0	45	0	50	0	60	0	70	ns	18
Row Address Strobe Precharge Time	t_{RP}	110	–	120	–	135	–	150	–	ns	
Row Address Strobe Pulse Width	t_{RAS}	115	10000	140	10000	175	10000	200	10000	ns	19
Column Address Strobe Pulse Width	t_{CAS}	55	10000	65	10000	95	10000	120	10000	ns	19
Row to Column Strobe Lead Time	t_{RCD}	25	45	25	55	25	70	30	80	ns	13
Row Address Setup Time	t_{ASR}	0	–	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RAH}	15	–	15	–	15	–	25	–	ns	
Column Address Setup Time	t_{ASC}	0	–	0	–	0	–	0	–	ns	
Column Address Hold Time	t_{CAH}	15	–	15	–	20	–	20	–	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{AR}	60	–	70	–	90	–	140	–	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	ns	6

AC OPERATING CONDITIONS AND CHARACTERISTICS (Continued)

Parameter	Symbol	MCM4517-10		MCM4517-12		MCM4517-15		MCM4517-20		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Command Setup Time	t_{RCS}	0	–	0	–	0	–	0	–	ns	
Read Command Hold Time	t_{RCH}	0	–	0	–	0	–	0	–	ns	14
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{RRH}	20	–	25	–	35	–	40	–	ns	14
Write Command Hold Time	t_{WCH}	25	–	30	–	45	–	60	–	ns	
Write Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{WCR}	70	–	85	–	115	–	140	–	ns	
Write Command Pulse Width	t_{WP}	25	–	30	–	50	–	50	–	ns	
Write Command to Row Strobe Lead Time	t_{RWL}	60	–	65	–	110	–	110	–	ns	
Write Command to Column Strobe Lead Time	t_{CWL}	45	–	50	–	100	–	100	–	ns	
Data in Setup Time	t_{DS}	0	–	0	–	0	–	0	–	ns	15
Data in Hold Time	t_{DH}	25	–	30	–	45	–	60	–	ns	15
Data in Hold Time Referenced to $\overline{\text{RAS}}$	t_{DHR}	70	–	85	–	115	–	140	–	ns	
Column to Row Strobe Precharge Time	t_{CRP}	0	–	0	–	0	–	0	–	ns	
$\overline{\text{RAS}}$ Hold Time	t_{RSH}	70	–	85	–	105	–	120	–	ns	
Refresh Period	t_{RFSH}	–	2.0	–	2.0	–	2.0	–	2.0	ms	
Write Command Setup Time	t_{WCS}	0	–	0	–	0	–	0	–	ns	16
$\overline{\text{CAS}}$ to $\overline{\text{WRITE}}$ Delay	t_{CWD}	55	–	65	–	80	–	100	–	ns	16
$\overline{\text{RAS}}$ to $\overline{\text{WRITE}}$ Delay	t_{RWD}	100	–	120	–	150	–	160	–	ns	16
$\overline{\text{CAS}}$ Hold Time	t_{CSH}	100	–	120	–	165	–	200	–	ns	
$\overline{\text{CAS}}$ Precharge, Non Page Mode	t_{CPN}	50	–	55	–	70	–	90	–	ns	
RMW Cycle $\overline{\text{RAS}}$ Pulse Width	t_{RRW}	135	10000	160	10000	195	10000	220	10000	ns	
RMW Cycle $\overline{\text{CAS}}$ Pulse Width	t_{CRW}	95	10000	110	10000	130	10000	140	10000	ns	
Page Mode Cycle Time	t_{PC}	125	–	145	–	190	–	260	–	ns	
Page Mode Cycle Time (Read-Modify-Write)	t_{PCM}	175	–	200	–	280	–	360	–	ns	
$\overline{\text{CAS}}$ Precharge Time (Page Mode Cycle Only)	t_{CP}	60	–	70	–	85	–	105	–	ns	
$\overline{\text{RAS}}$ Pulse Width (Page Mode Cycle Only)	t_{RPM}	115	10000	140	10000	175	10000	235	10000	ns	

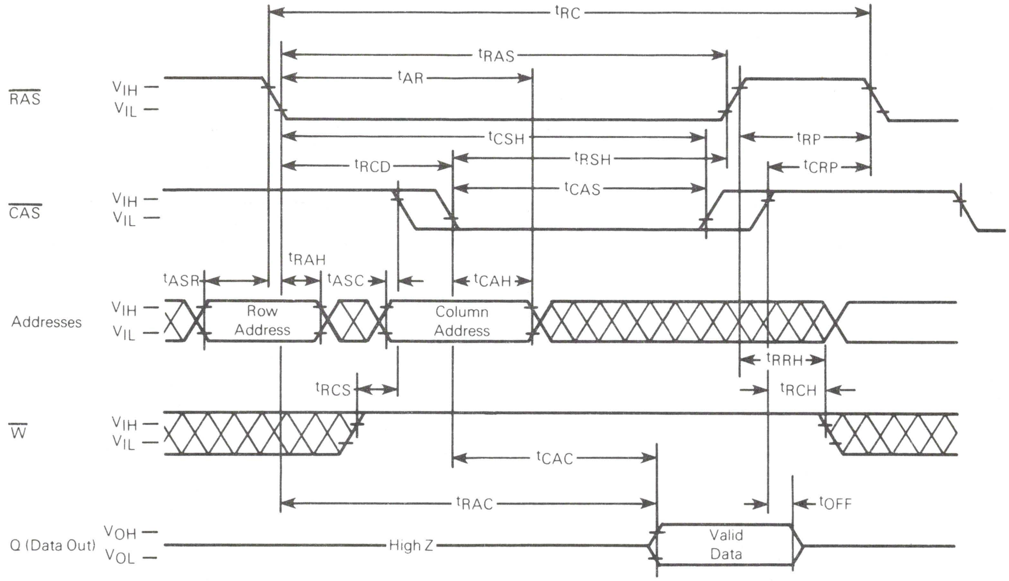
CAPACITANCE ($f = 1.0$ MHz, $T_A = 25°C$, $V_{CC} = +5$ V. Periodically sampled rather than 100% tested.)

Parameter	Symbol	Typ	Max	Units	Notes
Input Capacitance (A0-A6), D_{in}	C_{I1}	4.0	5.0	pF	7
Input Capacitance $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WRITE}}$	C_{I2}	5.0	7.0	pF	7

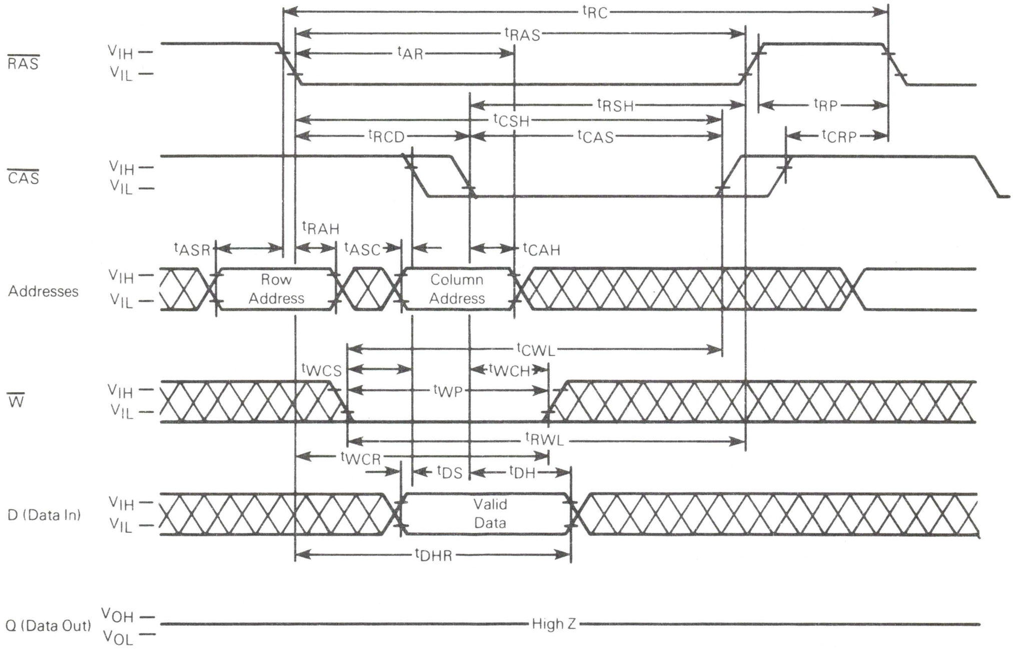
NOTES:

1. All voltages referenced to V_{SS}.
2. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
3. An initial pause of 100 μs is required after power-up followed by any 8 $\overline{\text{RAS}}$ cycles before proper device operation guaranteed.
4. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
5. Output is disabled (open-circuit) and $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are both at a logic 1.
6. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transmit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
7. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I_{\Delta t}/\Delta V$
8. The specifications for t_{RC} (min), and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
9. AC measurements assume $t_T = 5.0$ ns.
10. Assumes that $t_{RCD} \leq t_{RCD}$ (Max)
11. Assumes that $t_{RCD} \geq t_{RCD}$ (Max)
12. Measured with a current load equivalent to 2 TTL loads (+200 μA, −4 mA) and 100 pF ($V_{OH} = 2.0$ V, $V_{OL} = 0.8$ V).
13. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in random write cycles and to $\overline{\text{WRITE}}$ leading edge in delayed write or read-modify-write cycles.
16. t_{WCS}, t_{CWD}, and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
17. Addresses, data-in and $\overline{\text{WRITE}}$ are don't care. Data-out depends on the state of $\overline{\text{CAS}}$. If $\overline{\text{CAS}}$ remains low, the previous output will remain valid. $\overline{\text{CAS}}$ is allowed to make an active to inactive transition during the $\overline{\text{RAS}}$-only refresh cycle. When $\overline{\text{CAS}}$ is brought high, the output will assume a high-impedance state.
18. t_{off} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
19. For read and write cycles only.

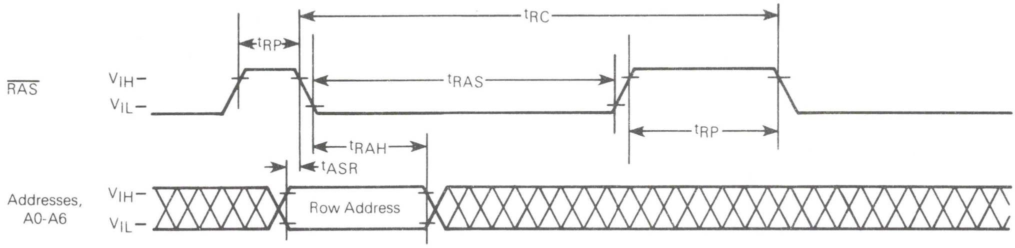
READ CYCLE TIMING


tRC
tRAS
tAR
RAS
VIH
VIL
tCSH
tRP
tRCD
tRSH
tCRP
tCAS
CAS
VIH
VIL
tRAH
tASR
tASC
tCAH
Addresses
VIH
VIL
Row Address
Column Address
tRRH
tRCS
tRCH
W
VIH
VIL
tCAC
tRAC
tOFF
Q (Data Out)
VOH
VOL
High Z
Valid Data

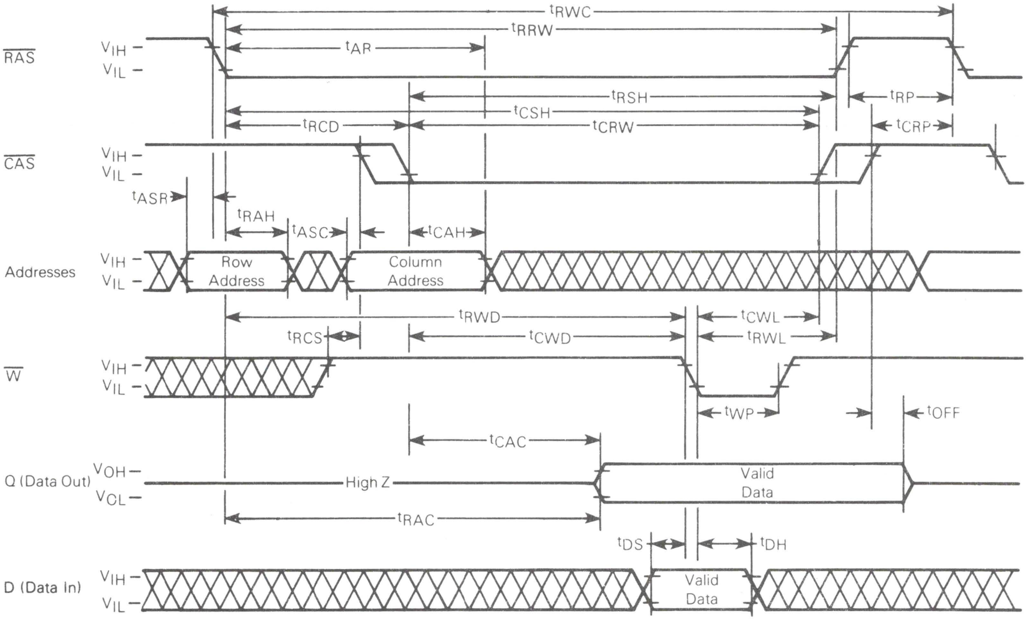
WRITE CYCLE TIMING


tRC
tRAS
tAR
RAS
VIH
VIL
tRSH
tRP
tCSH
tRCD
tCAS
tCRP
CAS
VIH
VIL
tRAH
tASR
tASC
tCAH
Addresses
VIH
VIL
Row Address
Column Address
tCWL
tWCS
tWCH
tWP
W
VIH
VIL
tRWL
tWCR
tDS
tDH
D (Data In)
VIH
VIL
Valid Data
tDHR
Q (Data Out)
VOH
VOL
High Z

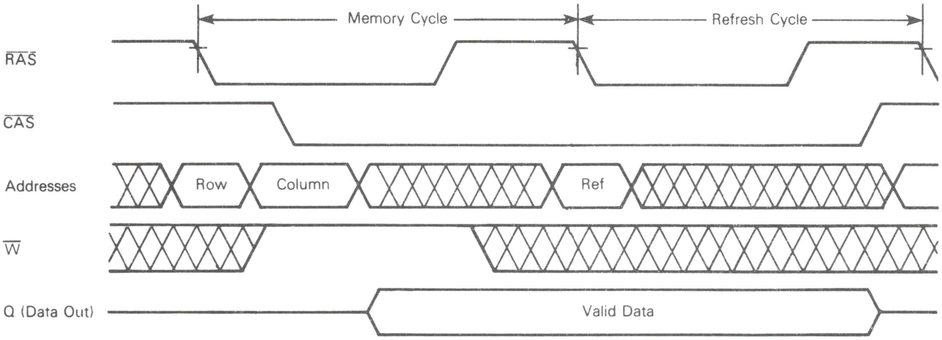
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE
(Data-In and $\overline{\text{Write}}$ are Don't Care, $\overline{\text{CAS}}$ is HIGH)


t_{RC}
t_{RP}
$\overline{\text{RAS}}$
V_{IH}
V_{IL}
t_{RAS}
t_{RP}
t_{RAH}
t_{ASR}
Addresses, A0-A6
V_{IH}
V_{IL}
Row Address

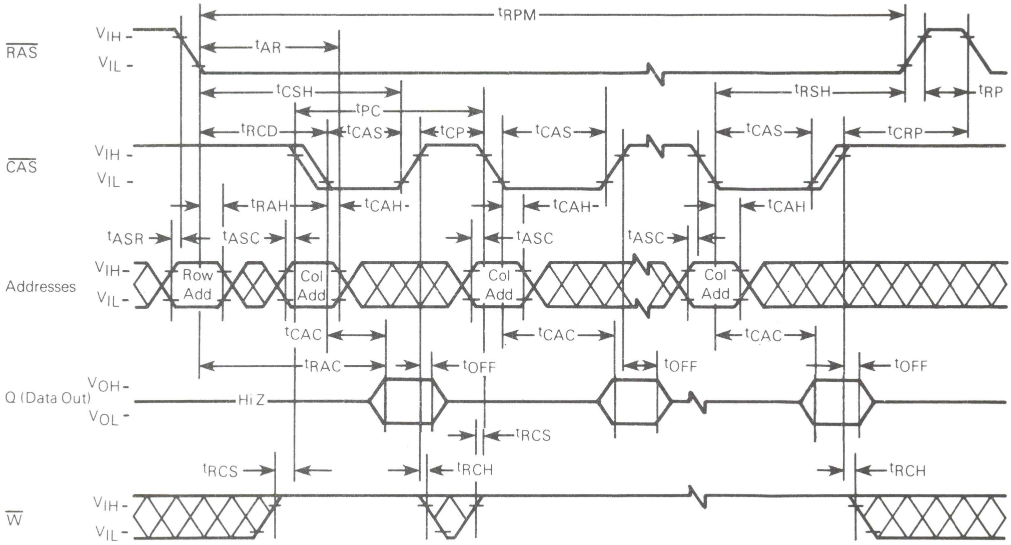
READ-WRITE/READ-MODIFY-WRITE CYCLE


t_{RWC}
t_{RRW}
t_{AR}
$\overline{\text{RAS}}$
V_{IH}
V_{IL}
t_{RSH}
t_{RP}
t_{CSH}
t_{RCD}
t_{CRW}
t_{CRP}
$\overline{\text{CAS}}$
V_{IH}
V_{IL}
t_{ASR}
t_{RAH}
t_{ASC}
t_{CAH}
Addresses
V_{IH}
V_{IL}
Row Address
Column Address
t_{RWD}
t_{CWL}
t_{RCS}
t_{CWD}
t_{RWL}
$\overline{\text{W}}$
V_{IH}
V_{IL}
t_{WP}
t_{OFF}
t_{CAC}
Q (Data Out)
V_{OH}
V_{OL}
High Z
Valid Data
t_{RAC}
t_{DS}
t_{DH}
D (Data In)
V_{IH}
V_{IL}
Valid Data

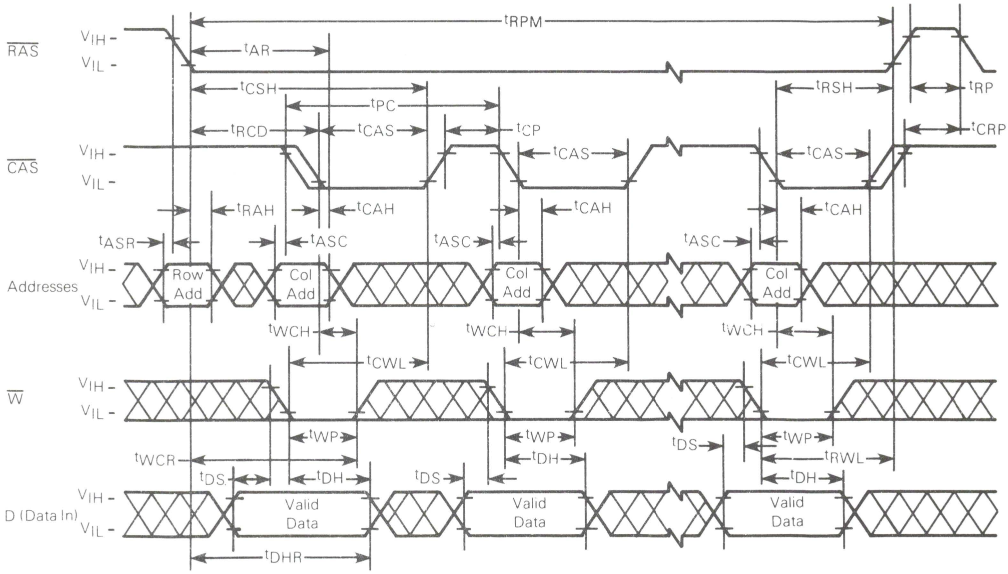
HIDDEN $\overline{\text{RAS}}$-ONLY REFRESH CYCLE (See Note 18)


Memory Cycle
Refresh Cycle
$\overline{\text{RAS}}$
$\overline{\text{CAS}}$
Addresses
Row
Column
Ref
$\overline{\text{W}}$
Q (Data Out)
Valid Data

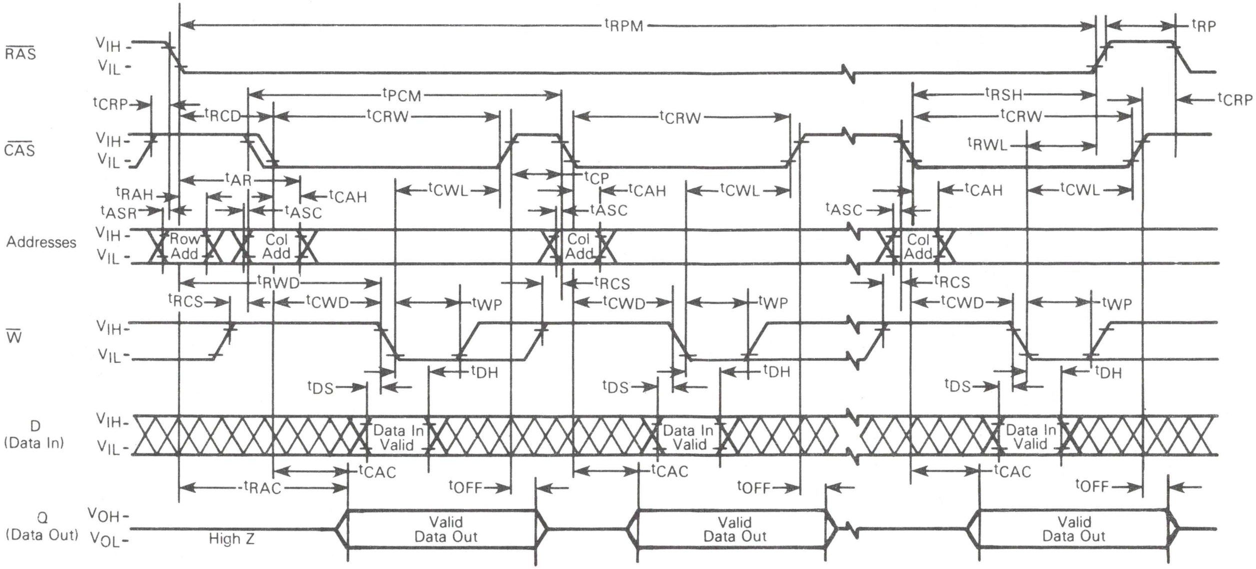
PAGE MODE READ CYCLE


RAS
CAS
Addresses
Q (Data Out)
W
VIH
VIL
VOH
VOL
tRPM
tAR
tCSH
tPC
tRCD
tCAS
tCP
tRSH
tRP
tCRP
tRAH
tCAH
tASR
tASC
Row Add
Col Add
tCAC
tRAC
tOFF
Hi Z
tRCS
tRCH

PAGE MODE WRITE CYCLE


RAS
CAS
Addresses
W
D (Data In)
VIH
VIL
tRPM
tAR
tCSH
tPC
tRCD
tCAS
tCP
tRSH
tRP
tCRP
tRAH
tCAH
tASR
tASC
Row Add
Col Add
tWCH
tCWL
tWP
tWCR
tDS
tDH
tRWL
Valid Data
tDHR

PAGE MODE READ-MODIFY-WRITE CYCLE


RAS
CAS
Addresses
W
D (Data In)
Q (Data Out)
VIH
VIL
VOH
VOL
tRPM
tRP
tCRP
tRCD
tPCM
tCRW
tRSH
tRWL
tAR
tRAH
tASR
tCAH
tASC
tCWL
tCP
Row Add
Col Add
tRWD
tRCS
tCWD
tWP
tDS
tDH
Data In Valid
tCAC
tRAC
tOFF
High Z
Valid Data Out

MOTOROLA

MCM6632A

Advance Information

32K BIT DYNAMIC RAM

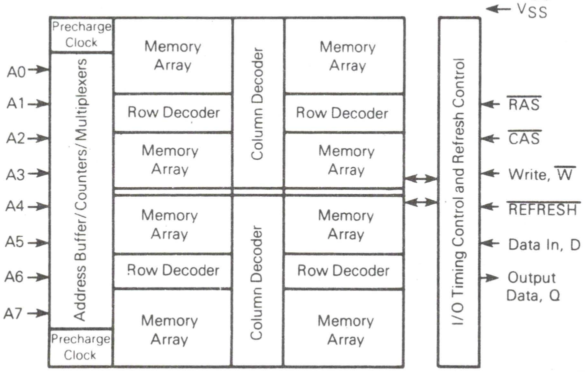
The MCM6632A is a 32,768 bit, high-speed, dynamic Random-Access Memory. Organized as 32,768 one-bit words and fabricated using HMOS high-performance N-channel silicon-gate technology, this new breed of 5-volt only dynamic RAM combines high performance with low cost and improved reliability.

By multiplexing row- and column-address inputs, the MCM6632A requires only eight address lines and permits packaging in standard 16-pin dual-in-line packages. Complete address decoding is done on chip with address latches incorporated. Data out is controlled by $\overline{\text{CAS}}$ allowing for greater system flexibility.

All inputs and outputs, including clocks, are fully TTL compatible. The MCM6632A incorporates a one-transistor cell design and dynamic storage techniques. In addition to the $\overline{\text{RAS}}$-only refresh mode, the refresh control function available on pin 1 provides two additional modes of refresh, automatic and self-refresh.

- Organized as 32,768 Words of 1 Bit
- Single 5 Volt Operation (± 10%)
- Maximum Access Time
  - MCM6632A-12 = 120 ns
  - MCM6632A-15 = 150 ns
  - MCM6632A-20 = 200 ns
- Low Power Dissipation
  - 302.5 mW Maximum (Active) (MCM6632A-15)
  - 22 mW Maximum (Standby)
- Early-Write Common I/O Capability
- Control on Pin 1 for Automatic and Self Refresh
- $\overline{\text{RAS}}$-only Refresh Mode
- $\overline{\text{CAS}}$ Controlled Output
- Low Soft Error Rate < 0.1% per 1000 Hours (See Soft Error Testing)
- One Half of the 64K Dynamic Ram MCM6664A
- The Operating Half of the MCM6632A is indicated by Device Marking: MCM66320A Tie A7 $\overline{\text{CAS}}$ (A15) Low "0"; MCM66321A Tie A7 $\overline{\text{CAS}}$ (A15) High "1"

BLOCK DIAGRAM



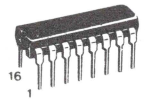
V_{CC}
V_{SS}
Precharge Clock
Memory Array
Column Decoder
Memory Array
Row Decoder
Row Decoder
Memory Array
Memory Array
Memory Array
Column Decoder
Memory Array
Row Decoder
Row Decoder
Memory Array
Memory Array
Precharge Clock
Address Buffer/Counters/Multiplexers
I/O Timing Control and Refresh Control
A0
A1
A2
A3
A4
A5
A6
A7
$\overline{\text{RAS}}$
$\overline{\text{CAS}}$
Write, $\overline{\text{W}}$
$\overline{\text{REFRESH}}$
Data In, D
Output Data, Q

This document contains information on a new product. Specifications and information herein are subject to change without notice.

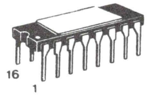
MOS

(N-CHANNEL, SILICON-GATE)

32,768-BIT DYNAMIC RANDOM ACCESS MEMORY

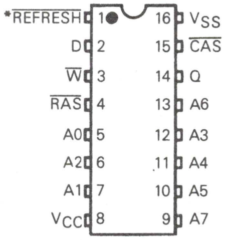


P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 690

PIN ASSIGNMENT



*$\overline{\text{REFRESH}}$ 1
D 2
$\overline{\text{W}}$ 3
$\overline{\text{RAS}}$ 4
A0 5
A2 6
A1 7
V_{CC} 8
16 V_{SS}
15 $\overline{\text{CAS}}$
14 Q
13 A6
12 A3
11 A4
10 A5
9 A7

*If pin is not used, it should be connected to V_{CC} through a 10 k resistor.

PIN NAMES

$\overline{\text{REFRESH}}$	Refresh
A0-A7	Address Input
D	Data In
Q	Data Out
$\overline{\text{W}}$	Read/Write Input
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
V_{CC}	Power (+5 V)
V_{SS}	Ground

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

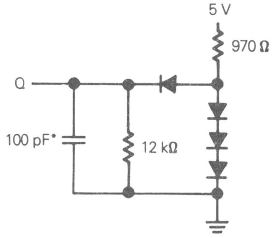
ADI-901/4-82

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS} (except V_{CC})	V_{in}, V_{out}	−2 to +7	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Power Dissipation	P_D	1.0	W
Data Out Current (Short Circuit)	I_{out}	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

FIGURE 1 — OUTPUT LOAD



*Includes Jig Capacitance

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	MCM6632A-12, -15, -20	V_{CC}	4.5	5.0	5.5	V	1
		V_{SS}	0	0	0	V	1
Logic 1 Voltage, All Inputs		V_{IH}	2.4	—	$V_{CC}+1$	V	1
Logic 0 Voltage, All Inputs		V_{IL}	−1.0	—	0.8	V	1, 19

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Units	Notes
V_{CC} Power Supply Current (Standby)	I_{CC2}	—	4.0	mA	5
V_{CC} Power Supply Current 6632A-12, $t_{RC}=250$ ns 6632A-15, $t_{RC}=270$ ns 6632A-20, $t_{RC}=330$ ns	I_{CC1}	 — — —	 60 55 50	mA	4
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles 6632A-12, $t_{RC}=250$ ns 6632A-15, $t_{RC}=270$ ns 6632A-20, $t_{RC}=330$ ns	I_{CC3}	 — — —	 50 45 40	mA	4
V_{CC} Power Supply Current During Page Mode Cycle for $t_{RAS}=10$ μsec 6632A-12, $t_{PC}=t_{RP}=120$ ns 6632A-15, $t_{PC}=t_{RP}=145$ ns 6632A-20, $t_{PC}=t_{RP}=200$ ns	I_{CC4}	—	 45 40 35	mA	4
Input Leakage Current ($V_{SS} \leq V_{in} \leq V_{CC}$) (Any Input Except $\overline{REFRESH}$)	$I_{I(L)}$	—	10	μA	—
$\overline{REFRESH}$ Input Current ($V_{SS} \leq V_{in} \leq V_{CC}$)	$I_{I(F)}$	—	20	μA	--
Output Leakage Current ($\overline{CAS}$ at logic 1, $V_{SS} \leq V_{out} \leq V_{CC}$)	$I_{O(L)}$	—	10	μA	—
Output Logic 1 Voltage @ $I_{out}=-4$ mA	V_{OH}	2.4	—	V	—
Output Logic 0 Voltage @ $I_{out}=4$ mA	V_{OL}	—	0.4	V	—

CAPACITANCE (f = 1.0 MHz, $T_A=25°C$, $V_{CC}=5$ V Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit	Notes
Input Capacitance (A0-A7), D	C_{I1}	3	5	pF	7
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{REFRESH}$	C_{I2}	6	8	pF	7
Output Capacitance (Q), ($\overline{CAS}=V_{IH}$ to disable output)	C_O	5	7	pF	7

NOTES:
1. All voltages referenced to V_{SS}.
2. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
3. An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation guaranteed.
4. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
5. $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1.
6. The transition time specification applies for all inputs signals. In addition to meeting the transition rate specification, all input signals must transmit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
7. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta t/\Delta V$
8. The specifications for t_{RC} (min), and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
9. AC measurements $t_T=5.0$ ns.
10. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
11. Assumes that $t_{RCD} \geq t_{RCD}$ (max)
12. Measured with a current load equivalent to 2 TTL (−200 μA, +4 mA) loads and 100 pF with the data output trip points set at $V_{OH}=2.0$ V and $V_{OL}=0.8$ V.

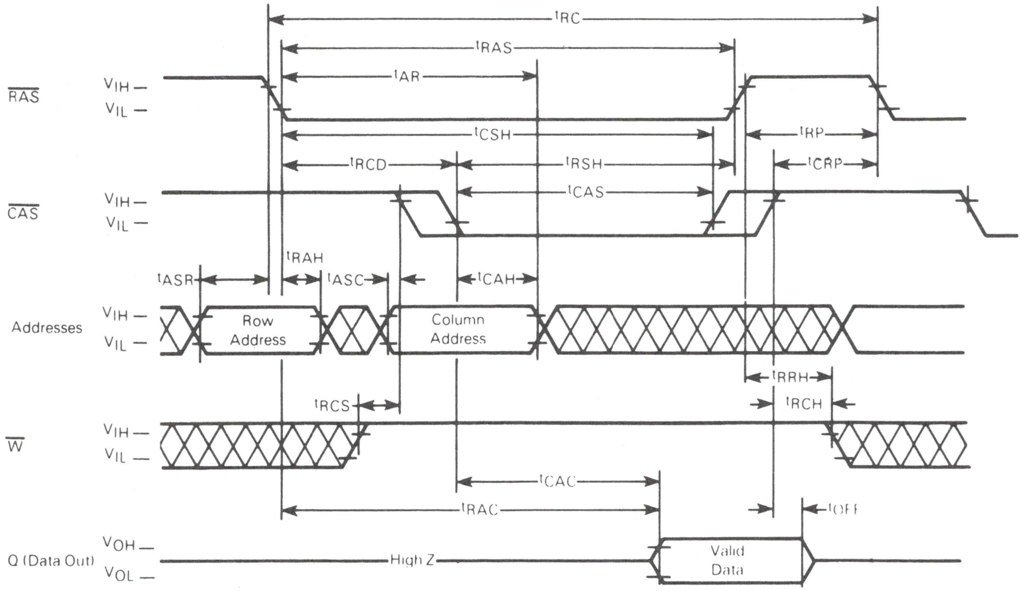
AC OPERATING CONDITIONS AND CHARACTERISTICS (Read, Write, and Read-Modify-Write Cycles)

(Full Operating Voltage and Temperature Range Unless Otherwise Noted . See Notes 2, 3, 6, and Figure 1)

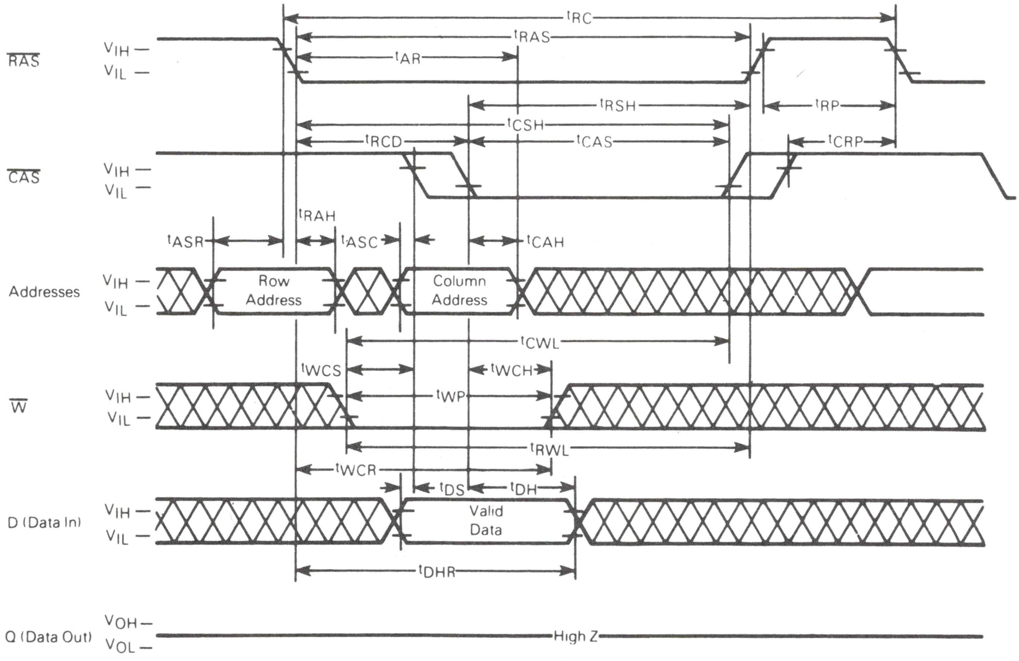
Parameter	Symbol	6632A-12		6632A-15		6632A-20		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	250	–	270	–	330	–	ns	8, 9
Read Write Cycle Time	t_{RWC}	255	–	280	–	345	–	ns	8, 9
Access Time from Row Address Strobe	t_{RAC}	–	120	–	150	–	200	ns	10, 12
Access Time from Column Address Strobe	t_{CAC}	–	60	–	75	–	100	ns	11, 12
Output Buffer and Turn-Off Delay	t_{OFF}	0	30	0	30	0	40	ns	18
Row Address Strobe Precharge Time	t_{RP}	100	–	100	–	120	–	ns	–
Row Address Strobe Pulse Width	t_{RAS}	120	10000	150	10000	200	10000	ns	–
Column Address Strobe Pulse Width	t_{CAS}	60	10000	75	10000	100	10000	ns	–
Row to Column Strobe Lead Time	t_{RCD}	25	60	30	75	35	100	ns	13
Row Address Setup Time	t_{ASR}	0	–	0	–	0	–	ns	–
Row Address Hold Time	t_{RAH}	15	–	20	–	25	–	ns	–
Column Address Setup Time	t_{ASC}	0	–	0	–	0	–	ns	–
Column Address Hold Time	t_{CAH}	25	–	35	–	45	–	ns	–
Column Address Hold Time Referenced to $\overline{\text{RAS}}$	t_{AR}	85	–	95	–	120	–	ns	17
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	6
Read Command Setup Time	t_{RCS}	0	–	0	–	0	–	ns	–
Read Command Hold Time	t_{RCH}	0	–	0	–	0	–	ns	14
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{RRH}	0	–	0	–	0	–	ns	14
Write Command Hold Time	t_{WCH}	25	–	35	–	45	–	ns	–
Write Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{WCR}	85	–	95	–	120	–	ns	17
Write Command Pulse Width	t_{WP}	25	–	35	–	45	–	ns	–
Write Command to Row Strobe Lead Time	t_{RWL}	40	–	45	–	55	–	ns	–
Write Command to Column Strobe Lead Time	t_{CWL}	40	–	45	–	55	–	ns	–
Data in Setup Time	t_{DS}	0	–	0	–	0	–	ns	15
Data in Hold Time	t_{DH}	25	–	35	–	45	–	ns	15
Data in Hold Time Referenced to $\overline{\text{RAS}}$	t_{DHR}	85	–	95	–	120	–	ns	17
Column to Row Strobe Precharge Time	t_{CRP}	–10	–	–10	–	–10	–	ns	–
$\overline{\text{RAS}}$ Hold Time	t_{RSH}	60	–	75	–	100	–	ns	–
Refresh Period	t_{RFSH}	–	2.0	–	2.0	–	2.0	ms	–
$\overline{\text{WRITE}}$ Command Setup Time	t_{WCS}	–10	–	–10	–	–10	–	ns	16
$\overline{\text{CAS}}$ to $\overline{\text{WRITE}}$ Delay	t_{CWD}	40	–	45	–	55	–	ns	16
$\overline{\text{RAS}}$ to $\overline{\text{WRITE}}$ Delay	t_{RWD}	100	–	120	–	155	–	ns	16
$\overline{\text{CAS}}$ Hold Time	t_{CSH}	120	–	150	–	200	–	ns	–
$\overline{\text{CAS}}$ Precharge Time (Page Mode Cycle Only)	t_{CP}	50	–	60	–	80	–	ns	–
Page Mode Cycle Time	t_{PC}	120	–	145	–	200	–	ns	–
$\overline{\text{RAS}}$ to $\overline{\text{REFRESH}}$ Delay	t_{RFD}	–10	–	–10	–	–10	–	ns	–
$\overline{\text{REFRESH}}$ Period (Battery Backup Mode)	t_{FBP}	2000	–	2000	–	2000	–	ns	–
$\overline{\text{REFRESH}}$ to $\overline{\text{RAS}}$ Precharge Time (Battery Backup Mode)	t_{FBR}	290	–	320	–	400	–	ns	–
$\overline{\text{REFRESH}}$ Cycle Time (Auto Pulse Mode)	t_{FC}	250	–	270	–	330	–	ns	–
$\overline{\text{REFRESH}}$ Pulse Period (Auto Period Mode)	t_{FP}	60	2000	60	2000	60	2000	ns	–
$\overline{\text{REFRESH}}$ to $\overline{\text{RAS}}$ Setup Time (Auto Pulse Mode)	t_{FSR}	–30	–	–30	–	–30	–	ns	–
$\overline{\text{REFRESH}}$ to $\overline{\text{RAS}}$ Delay Time (Auto Pulse Mode)	t_{FRD}	290	–	320	–	400	–	ns	–
$\overline{\text{REFRESH}}$ Inactive Time	t_{FI}	60	–	60	–	60	–	ns	–
$\overline{\text{RAS}}$ to $\overline{\text{REFRESH}}$ Lead Time	t_{FRL}	350	–	370	–	450	–	ns	–
$\overline{\text{RAS}}$ Inactive Time During $\overline{\text{REFRESH}}$	t_{FRI}	350	–	370	–	450	–	ns	–

13. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{WRITE}}$ leading edge in delayed write or read-modify-write cycles.
16. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
17. t_{AR} min $\leq$ $t_{AR} = t_{RCD} + t_{CAH}$, t_{DHR} min $\leq$ $t_{DHR} = t_{RCD} + t_{DH}$, t_{WCR} min $\leq$ $t_{WCR} = t_{RCD} + t_{WCH}$
18. t_{off} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
19. The device will withstand undershoots to the –2 volt level with a maximum pulse width of 20 ns at the –1.5 volt level. This is periodically sampled rather than 100% tested.

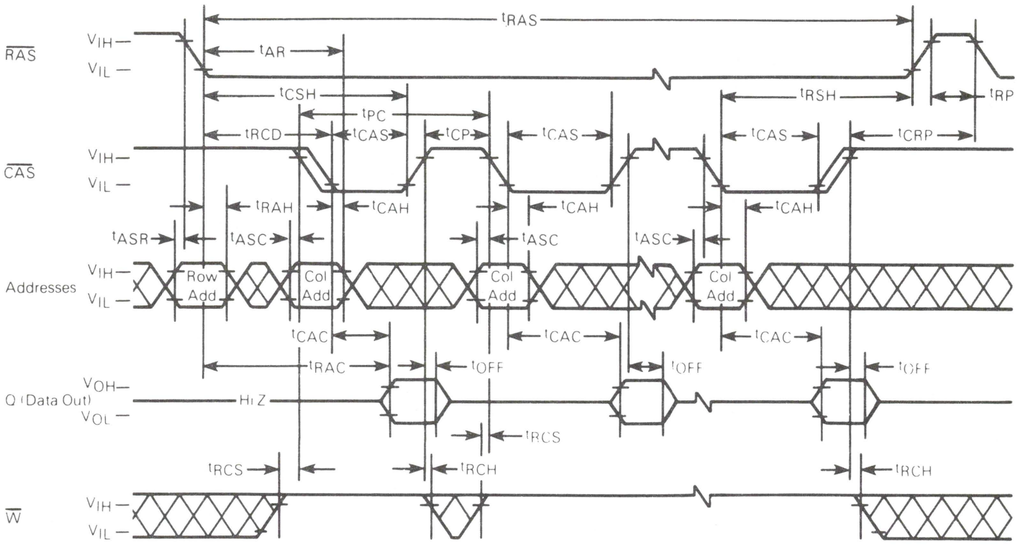
READ CYCLE TIMING


t_{RC}
t_{RAS}
t_{AR}
$\overline{RAS}$
V_{IH} —
V_{IL} —
t_{CSH}
t_{RP}
t_{RCD}
t_{RSH}
t_{CRP}
t_{CAS}
$\overline{CAS}$
V_{IH} —
V_{IL} —
t_{RAH}
t_{ASR}
t_{ASC}
t_{CAH}
Addresses
V_{IH} —
V_{IL} —
Row Address
Column Address
t_{RRH}
t_{RCS}
t_{RCH}
$\overline{W}$
V_{IH} —
V_{IL} —
t_{CAC}
t_{RAC}
t_{OFF}
Q (Data Out)
V_{OH} —
V_{OL} —
High Z
Valid Data

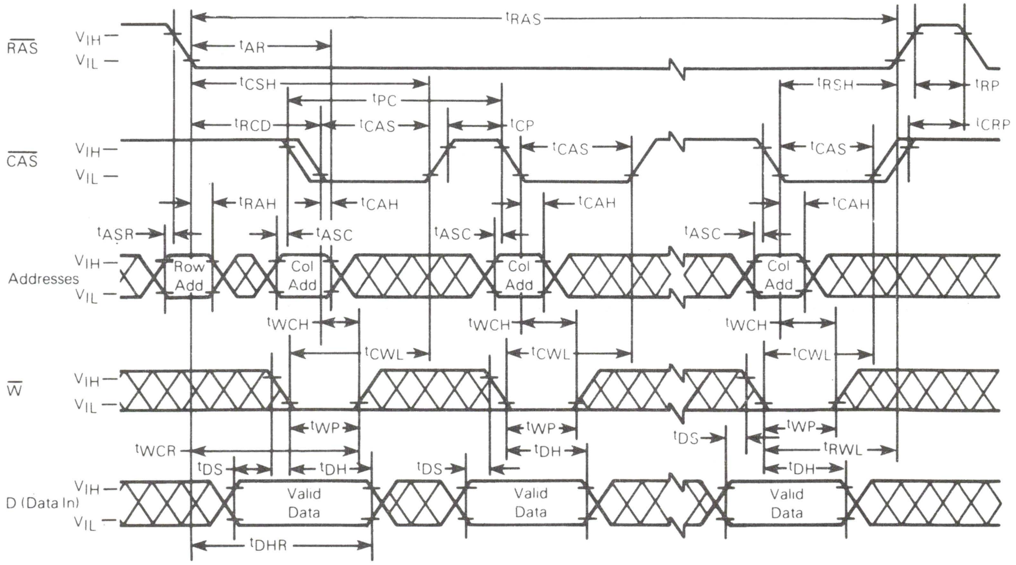
WRITE CYCLE TIMING


t_{RC}
t_{RAS}
t_{AR}
$\overline{RAS}$
V_{IH} —
V_{IL} —
t_{RSH}
t_{RP}
t_{CSH}
t_{RCD}
t_{CAS}
t_{CRP}
$\overline{CAS}$
V_{IH} —
V_{IL} —
t_{RAH}
t_{ASR}
t_{ASC}
t_{CAH}
Addresses
V_{IH} —
V_{IL} —
Row Address
Column Address
t_{CWL}
t_{WCS}
t_{WCH}
t_{WP}
$\overline{W}$
V_{IH} —
V_{IL} —
t_{RWL}
t_{WCR}
t_{DS}
t_{DH}
D (Data In)
V_{IH} —
V_{IL} —
Valid Data
t_{DHR}
Q (Data Out)
V_{OH} —
V_{OL} —
High Z

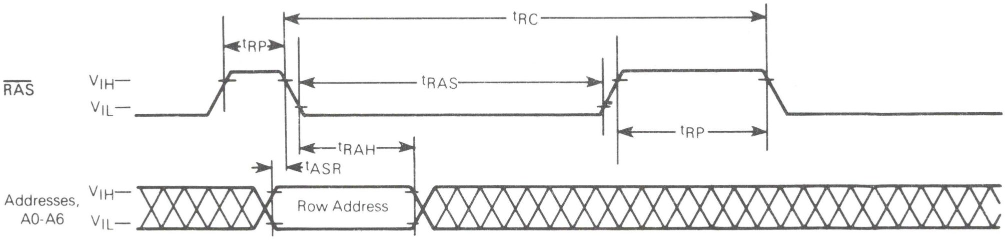
PAGE MODE READ CYCLE


RAS
CAS
Addresses
Q (Data Out)
W
V_{IH}
V_{IL}
V_{OH}
V_{OL}
t_{RAS}
t_{AR}
t_{CSH}
t_{PC}
t_{RSH}
t_{RP}
t_{RCD}
t_{CAS}
t_{CP}
t_{CRP}
t_{RAH}
t_{CAH}
t_{ASR}
t_{ASC}
Row Add
Col Add
t_{CAC}
t_{RAC}
t_{OFF}
Hi Z
t_{RCS}
t_{RCH}

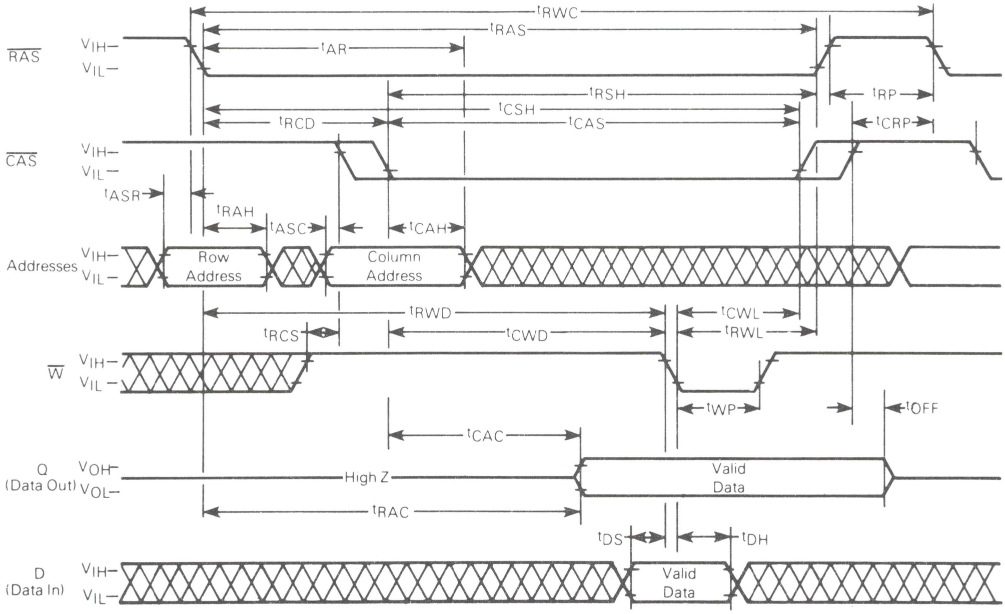
PAGE MODE WRITE CYCLE

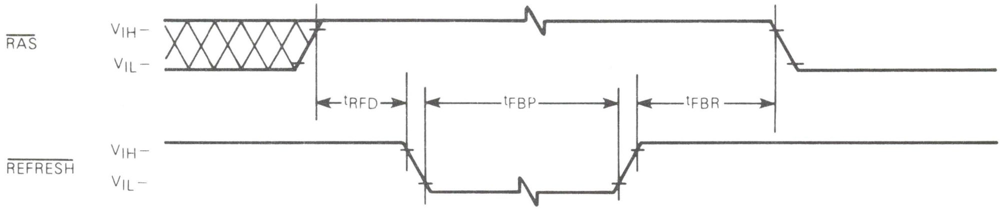

RAS
CAS
Addresses
W
D (Data In)
V_{IH}
V_{IL}
t_{RAS}
t_{AR}
t_{CSH}
t_{PC}
t_{RSH}
t_{RP}
t_{RCD}
t_{CAS}
t_{CP}
t_{CRP}
t_{RAH}
t_{CAH}
t_{ASR}
t_{ASC}
Row Add
Col Add
t_{WCH}
t_{CWL}
t_{WP}
t_{WCR}
t_{DS}
t_{DH}
t_{RWL}
Valid Data
t_{DHR}

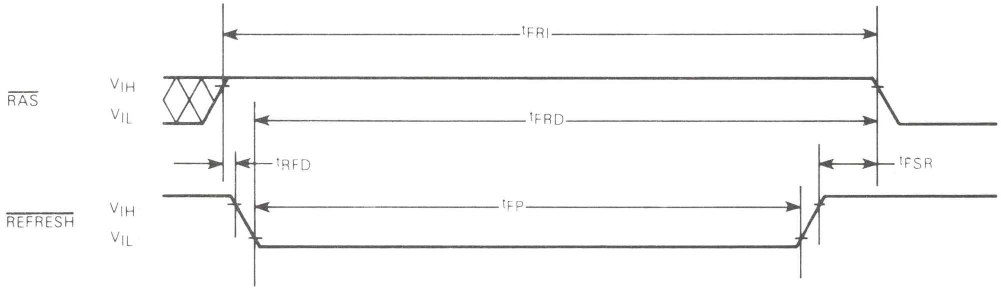
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE
(Data-in and Write are Don't Care, $\overline{\text{CAS}}$ is HIGH)

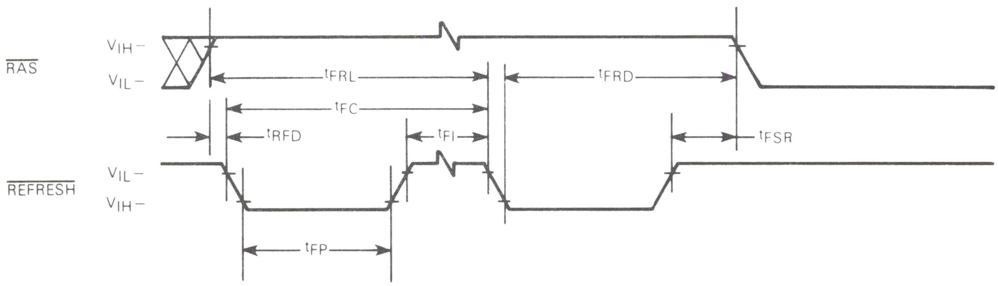

tRC
tRP
tRAS
$\overline{\text{RAS}}$ VIH— VIL—
tRP
tRAH
tASR
Addresses, A0-A6 VIH— VIL—
Row Address

READ-WRITE/READ-MODIFY-WRITE CYCLE


tRWC
tRAS
tAR
$\overline{\text{RAS}}$ VIH— VIL—
tRSH
tRP
tCSH
tRCD
tCAS
tCRP
$\overline{\text{CAS}}$ VIH— VIL—
tASR
tRAH
tASC
tCAH
Addresses VIH— VIL—
Row Address
Column Address
tRWD
tCWL
tRCS
tCWD
tRWL
$\overline{\text{W}}$ VIH— VIL—
tWP
tOFF
tCAC
Q (Data Out) VOH— VOL—
High Z
Valid Data
tRAC
tDS
tDH
D (Data In) VIH— VIL—
Valid Data


SELF REFRESH MODE (Battery Backup)*
RAS
V_IH –
V_IL –
t_RFD
t_FBP
t_FBR
REFRESH
V_IH –
V_IL –


AUTOMATIC PULSE REFRESH CYCLE — SINGLE PULSE*
t_FRI
RAS
V_IH
V_IL
t_FRD
t_RFD
t_FSR
REFRESH
V_IH
V_IL
t_FP


AUTOMATIC PULSE REFRESH CYCLE — MULTIPLE PULSE*
RAS
V_IH –
V_IL –
t_FRL
t_FRD
t_FC
t_RFD
t_FI
t_FSR
REFRESH
V_IL –
V_IH –
t_FP

*Addresses, data-in and WRITE are don't care.

TYPICAL CHARACTERISTICS

FIGURE 2 — $\overline{\text{RAS}}$ ACCESS TIME versus SUPPLY VOLTAGE

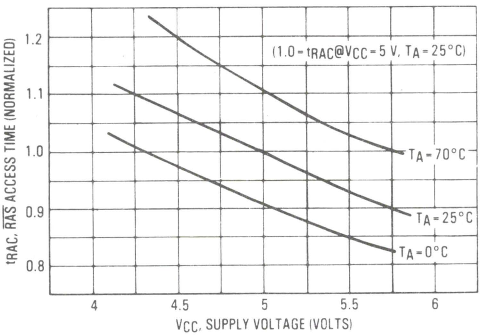


FIGURE 3 — $\overline{\text{CAS}}$ ACCESS TIME versus SUPPLY VOLTAGE

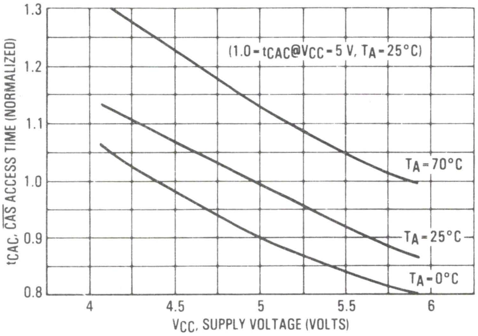


FIGURE 4 — $\overline{\text{RAS}}$ ACCESS TIME versus AMBIENT TEMPERATURE

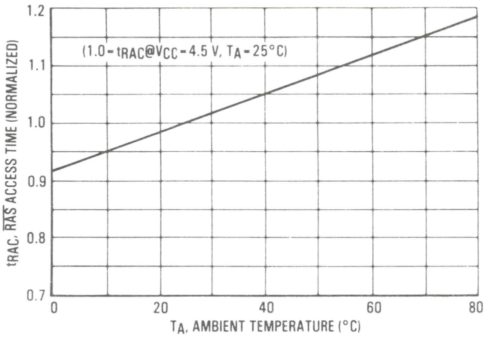


FIGURE 5 — $\overline{\text{CAS}}$ ACCESS TIME versus AMBIENT TEMPERATURE

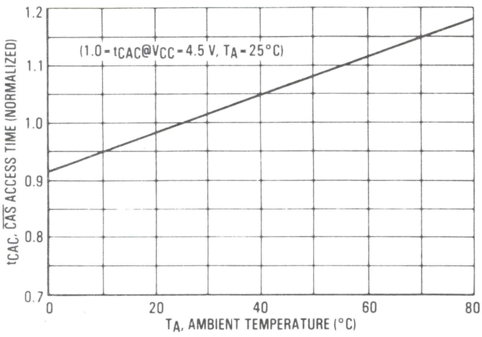


FIGURE 6 — $\overline{\text{RAS}}$, $\overline{\text{W}}$ INPUT LEVEL versus SUPPLY VOLTAGE

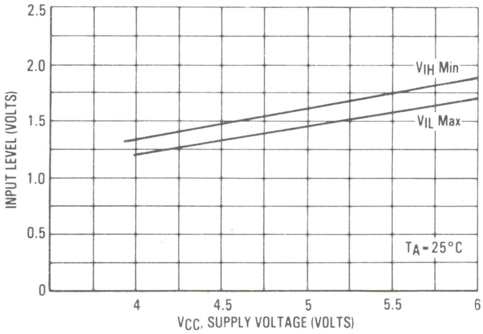
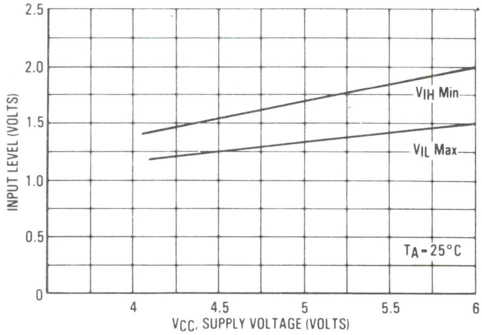


FIGURE 7 — $\overline{\text{CAS}}$, $\overline{\text{W}}$ INPUT LEVEL versus SUPPLY VOLTAGE



TYPICAL CHARACTERISTICS (continued)

FIGURE 8 — I_{CC1} SUPPLY CURRENT versus CYCLE RATE

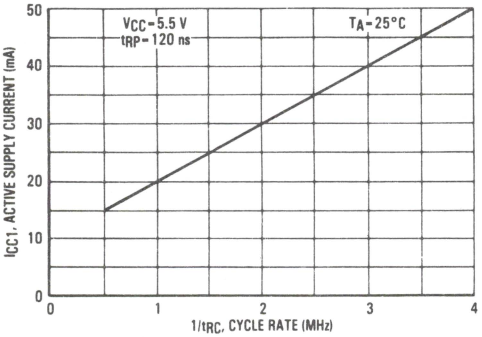


FIGURE 9 — I_{CC1} SUPPLY CURRENT versus SUPPLY VOLTAGE

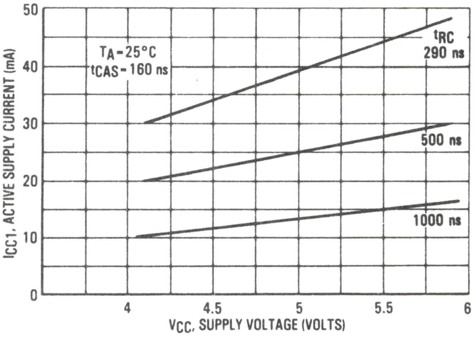


FIGURE 10 — I_{CC1} SUPPLY CURRENT versus SUPPLY VOLTAGE

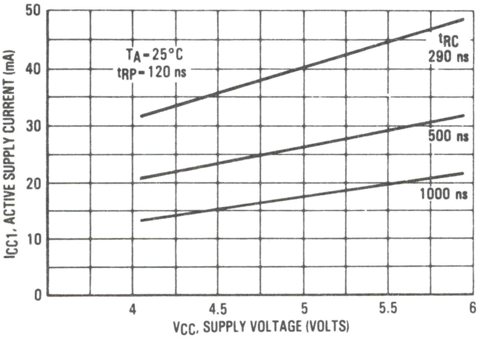


FIGURE 11 — I_{CC1} SUPPLY CURRENT versus AMBIENT TEMPERATURE (min t_{RP})

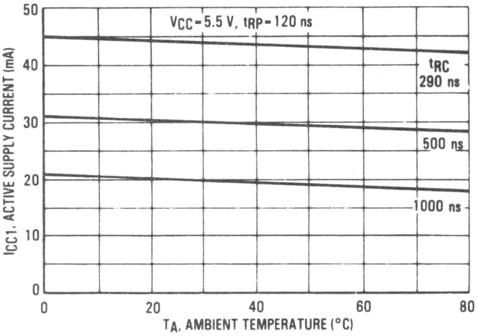


FIGURE 12 — I_{CC1} SUPPLY CURRENT versus AMBIENT TEMPERATURE (min $\overline{RAS}$)

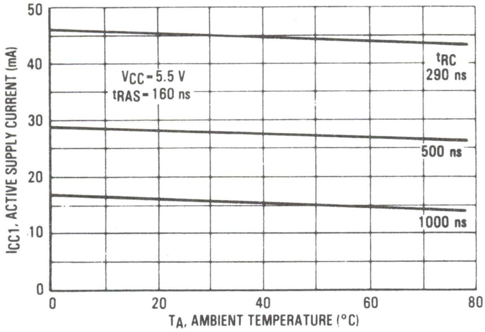
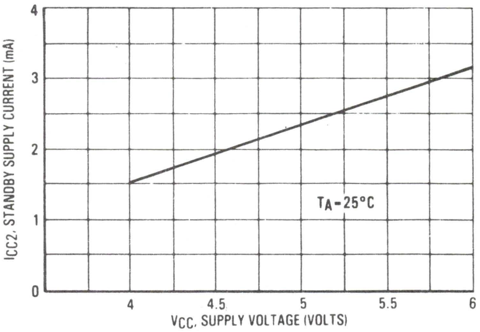


FIGURE 13 — I_{CC2} SUPPLY CURRENT versus SUPPLY VOLTAGE



TYPICAL CHARACTERISTICS (continued)

FIGURE 14 — I_{CC2} STANDBY CURRENT versus AMBIENT TEMPERATURE

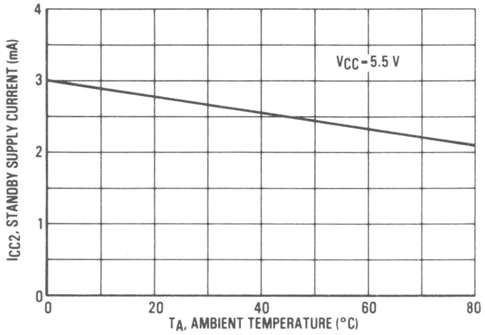


FIGURE 15 — I_{CC3} SUPPLY CURRENT versus CYCLE RATE

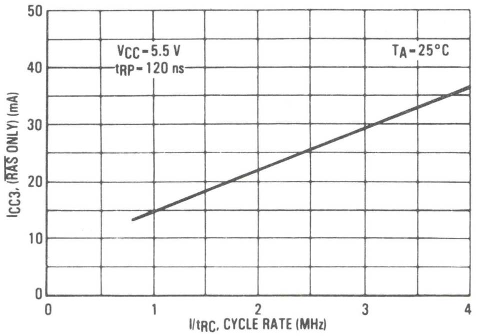


FIGURE 16 — ADDRESS INPUT LEVEL versus SUPPLY VOLTAGE

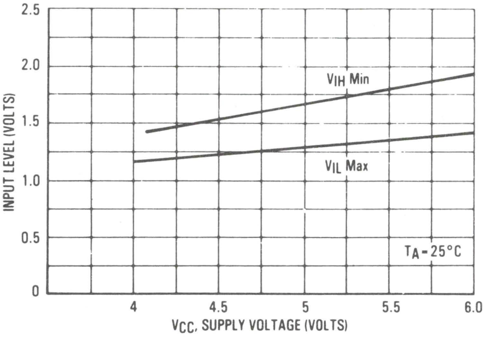
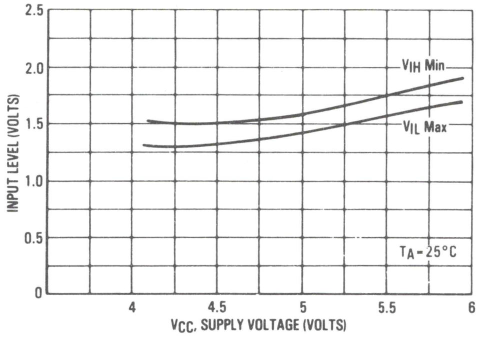


FIGURE 17 — DATA INPUT LEVEL versus SUPPLY VOLTAGE



SOFT ERROR TESTING

The storage cell depletion regions as well as the sense amplifier and its associated bit lines are susceptible to charge collection of electrons from an alpha "hit." However, the susceptibility of these vulnerable regions varies. Depleted storage cells are vulnerable at all times, whereas the sense amplifiers and associated bit lines are susceptible only during the small portion of the memory cycle just prior to sensing. Hence, an increase in the frequency of dynamic RAM access will cause a corresponding increase in the soft error rate.

To take this memory access dependency into account, the total soft error rate profile includes a cycle time component. The soft error rate due to bit line hits at the system's memory cycle rate is added to the soft error rate due to storage cell hits which are not frequency dependent. Figure 18 illustrates the impact that frequency of access has on the MCM6664A/MCM6665A overall soft error rate.

Under normal operating conditions, the die will be exposed to radiation levels of less than 0.01 alpha/cm^2/hr. Accelerated soft error testing data is generated from at least three high-intensity sources having an Alpha Flux Density range of 1 × 10^5 to 6 × 10^5 (alpha/cm^{2}hr) placed over uncoated die. Figure 19 shows the soft error rate for a given alpha flux density at a cycle rate of 100 kHz. The accelerated data of Figures 18 and 19 project that the soft error rate for package level radiation will be less than 0.1%/1000 hours.

SYSTEM LIFE OPERATING TEST CONDITIONS

1) Cycle time: 1 microsecond for read, write and refresh cycles
2) Refresh Rate: 1 millisecond
3) Voltage: 5.0 V
4) Temperature: 30°C ±2°C (ambient temperature inside enclosure)
5) Elevation: Approximately 620 feet above mean sea level
6) Data Patterns: Write the entire memory space sequentially with all "1"s and then perform continuous sequential reads for 6 hours. Next, write the entire memory space with all "0"s sequentially and then perform continuous sequential reads for 6 hours. Next, go back to the all "1"s pattern and repeat the sequences all over again.

FIGURE 18 — ACCELERATED SOFT ERROR versus CYCLE TIME

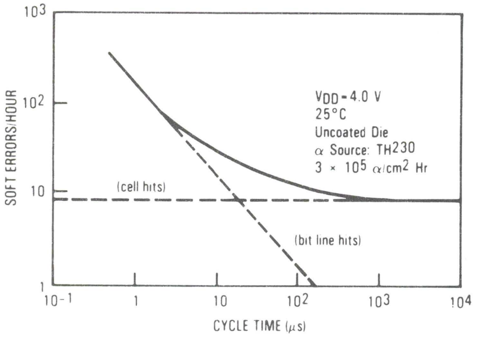
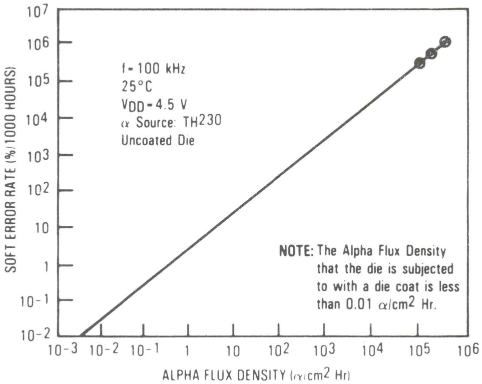


FIGURE 19 — SOFT ERROR RATE versus ALPHA FLUX DENSITY



CURRENT WAVEFORMS

FIGURE 20 — $\overline{RAS}/\overline{CAS}$ CYCLE

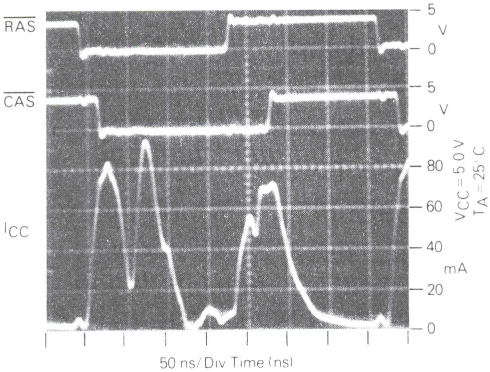


FIGURE 21 — LONG $\overline{RAS}/\overline{CAS}$ CYCLE

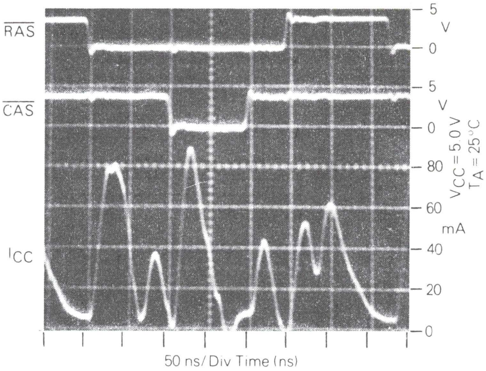


FIGURE 22 — $\overline{RAS}$ ONLY CYCLE

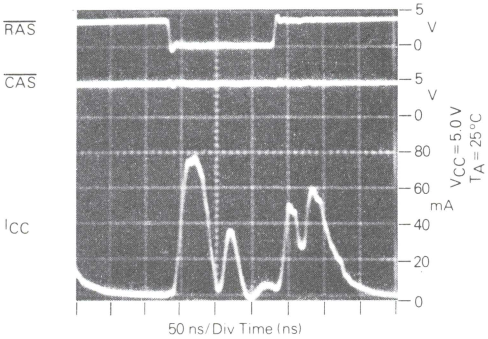


FIGURE 23 — PAGE MODE CYCLE

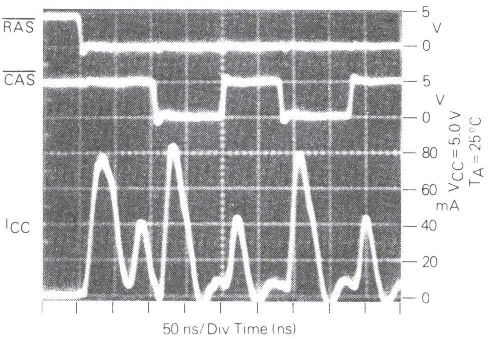
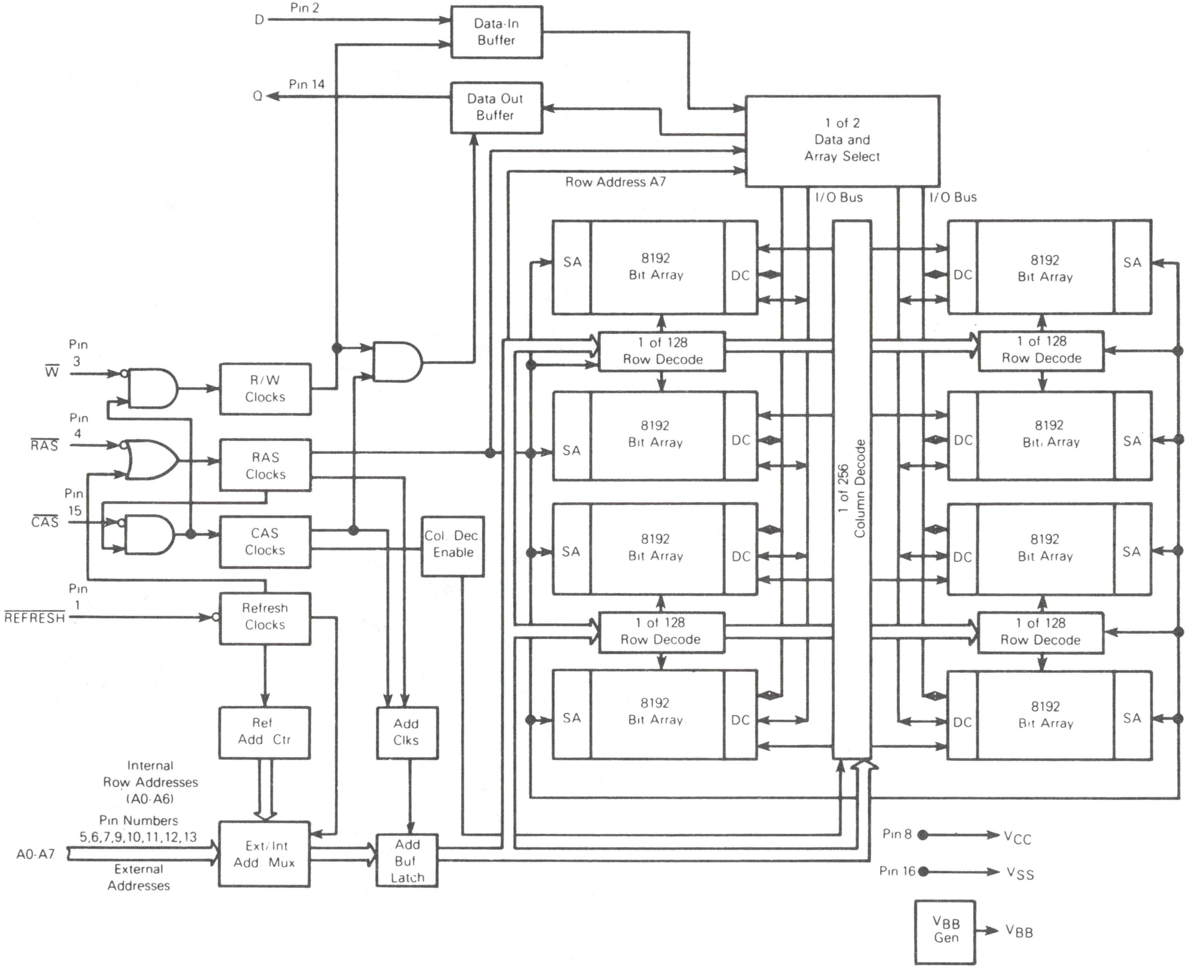


FIGURE 24 — FUNCTIONAL BLOCK DIAGRAM


D
Pin 2
Data-In Buffer
Q
Pin 14
Data Out Buffer
1 of 2 Data and Array Select
Row Address A7
I/O Bus
I/O Bus
SA
8192 Bit Array
DC
1 of 128 Row Decode
1 of 256 Column Decode
Pin 3
W
Pin 4
RAS
Pin 15
CAS
Pin 1
REFRESH
R/W Clocks
RAS Clocks
CAS Clocks
Col Dec Enable
Refresh Clocks
Ref Add Ctr
Add Clks
Internal Row Addresses (A0-A6)
Pin Numbers 5,6,7,9,10,11,12,13
A0-A7
External Addresses
Ext/Int Add Mux
Add Buf Latch
Pin 8
VCC
Pin 16
VSS
VBB Gen
VBB

DEVICE INITIALIZATION

Since the 32K dynamic RAM is a single supply 5 V only device, the need for power supply sequencing is no longer required as was the case in older generation dynamic RAMs. On power-up an initial pause of 100 microseconds is required for the internal substrate generator pump to establish the correct bias voltage. This is to be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize the various dynamic nodes internal to the device. During an extended inactive state of the device (greater than 2 ms with device powered up) the wake up sequence (8 active cycles) will be necessary to assure proper device operation. See Figures 25 and 26 for power on characteristics of the RAM for two conditions (clocks active, clocks inactive).

The row address strobe is the primary "clock" that activates the device and maintains the data when the RAM is in the standby mode. This is the main feature that distinquishes it as a dynamic RAM as opposed to a static RAM. A dynamic RAM is placed in a low power standby mode when the device receives a positive-going row address strobe. The variation in the power dissipation of a dynamic RAM from the active to the standby state is an order of magnitude or more for NMOS devices. This feature is used to its fullest advantage with high density mainframe memory systems, where only a very small percentage of the devices are in the active mode at any one time and the rest of the devices are in the standby mode. Thus, large memory systems can be assembled that dissipate very low power per bit compared to a system where all devices are active continuously.

ADDRESSING THE RAM

The eight address pins on the device are time multiplexed with two separate 8-bit address fields that are strobed at the beginning of the memory cycle by two clocks (active negative) called the row address strobe and the column address strobe. A total of fifteen address bits will decode one of the 32,768 cell locations in the device. The column address strobe follows the row address strobe by a specified minimum and maximum time called "t_{RCD}," which is the row to column strobe delay. This time interval is also referred to as the multiplex window which gives flexibility to a system designer to set up his external addresses into the RAM. These conditions have to be met for normal read or write cycles. This initial portion of the cycle accomplishes the normal addressing of the device. There are, however, two other variations in addressing the 32K RAM, one is called the page mode cycle (described later) where an 8-bit column address field is presented on the input pins and latched by the $\overline{CAS}$ clock; and the other is the $\overline{RAS}$ only refresh cycle (described later) where a 7-bit row address field is presented on the input pins and latched by the $\overline{RAS}$ clock. In the latter case, the most significant bit on Row Address A7 (pin 9) is not required for refresh. See bit address map for the topology of the cells and their address selection.

NORMAL READ CYCLE

A read cycle is referred to as normal read cycle to differentiate it from a page-mode-read cycle, a read-while-write cycle, and read-modify-write cycle which are covered in a later section.

The memory read cycle begins with the row addresses valid and the $\overline{RAS}$ clock transitioning from V_{IH} to the V_{IL} level. The $\overline{CAS}$ clock must also make a transition from V_{IH} to the V_{IL} level at the specified t_{RCD} timing limits when the column addresses are latched. Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. Also, these clocks are linked in such a manner that the access time of the device is independent of the address multiplex window. The only stipulation is that the $\overline{CAS}$ clock must be active before or at

CURRENT WAVEFORMS

FIGURE 25 — SUPPLY CURRENT versus SUPPLY VOLTAGE DURING POWER UP, $\overline{RAS}$, $\overline{CAS}$ = V_{CC}

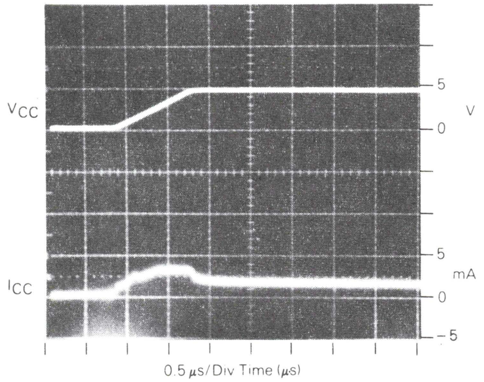
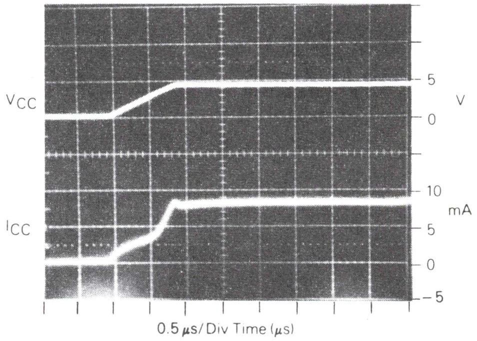


FIGURE 26 — SUPPLY CURRENT versus SUPPLY VOLTAGE DURING POWER UP, $\overline{RAS}$, $\overline{CAS}$ = V_{SS}



the t_{RCD} maximum specification for an access (data valid) from the $\overline{\text{RAS}}$ clock edge to be guaranteed (t_{RAC}). If the t_{RCD} maximum condition is not met, the access (t_{CAC}) from the $\overline{\text{CAS}}$ clock active transition will determine read access time. The external $\overline{\text{CAS}}$ signal is ignored until an internal $\overline{\text{RAS}}$ signal is available, as noted in the functional block diagram, Figure 24. This gating feature on the $\overline{\text{CAS}}$ clock will allow the external $\overline{\text{CAS}}$ signal to become active as soon as the row address hold time (t_{RAH}) specification has been met and defines the t_{RCD} minimum specification. The time difference between t_{RCD} minimum and t_{RCD} maximum can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{\text{CAS}}$ clock.

Once the clocks have become active, they must stay active for the minimum (t_{RAS}) period for the $\overline{\text{RAS}}$ clock and the minimum (t_{CAS}) period for the $\overline{\text{CAS}}$ clock. The $\overline{\text{RAS}}$ clock must stay inactive for the minimum (t_{RP}) time. The former is for the completion of the cycle in progress, and the latter is for the device internal circuitry to be precharged for the next active cycle.

Data out is not latched and is valid as long as the $\overline{\text{CAS}}$ clock is active; the output will switch to the three-state mode when the $\overline{\text{CAS}}$ clock goes inactive. The $\overline{\text{CAS}}$ clock can remain active for a maximum of 10 ns (t_{CRP}) into the next cycle. To perform a read cycle, the write ($\overline{\text{W}}$) input must be held at the V_{IH} level from the time the $\overline{\text{CAS}}$ clock makes its active transition (t_{RCS}) to the time when it transitions into the inactive (t_{RCH}) mode.

WRITE CYCLE

A write cycle is similar to a read cycle except that the Write ($\overline{\text{W}}$) clock must go active (V_{IL} level) at or before the $\overline{\text{CAS}}$ clock goes active at a minimum t_{WCS} time. If the above condition is met, then the cycle in progress is referred to as a early write cycle. In an early write cycle, the write clock and the data in is referenced to the active transition of the $\overline{\text{CAS}}$ clock edge. There are two important parameters with respect to the write cycle: the column strobe to write lead time (t_{CWL}) and the row strobe to write lead time (t_{RWL}). These define the minimum time that $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks need to be active after the write operation has started (($\overline{\text{W}}$) clock at V_{IL} level).

It is also possible to perform a late write cycle. For this cycle the write clock is activated after the $\overline{\text{CAS}}$ goes low which is beyond t_{WCS} minimum time. Thus the parameters t_{CWL} and t_{RWL} must be satisfied before terminating this cycle. The difference between an early write cycle and a late write cycle is that in a late write cycle the write ($\overline{\text{W}}$) clock can occur much later in time with respect to the active transition of the $\overline{\text{CAS}}$ clock. This time could be as long as 10 microseconds — $[t_{RWL} + t_{RP} + 2T_t]$.

At the start of a write cycle, the data out is in a three-state condition and remains inactive throughout the cycle. The data out remains three-state because of the active transition of the write ($\overline{\text{W}}$) clock prevents the $\overline{\text{CAS}}$ clock from enabling the data-out buffers as noted in Functional Block Diagram. The three-state condition (high impedence) of the Data Out Pin during a write cycle can be effectively utilized in a systems that has a common input/output bus. The only stipulation is that the system use only early write mode operations for all write cycles to avoid bus contention.

READ-MODIFY-WRITE AND READ-WHILE-WRITE CYLES

As the name implies, both a read and a write cycle is accomplished at a selected bit during a single access. The read-modify-write cycle is similar to the late write cycle discussed above.

For the read-modify-write cycle a normal read cycle is initiated with the write ($\overline{\text{W}}$) clock at the V_{IH} level until the read data occurs at the device access time (t_{RAC}). At this time the write ($\overline{\text{W}}$) clock is asserted. The data in is setup and held with respect to the active edge of the write clock. The cycle described assumes a zero modify time between read and write.

Another variation of the read-modify-write cycle is the read-while-write cycle. For this cycle, the following parameters (t_{RWD}, t_{CWD}) play an important role. A read-while-write cycle starts as a normal read cycle with the write ($\overline{\text{W}}$) clock being asserted at minimum t_{RWD} or minimum t_{CWD} time, depending upon the application. This results in starting a write operation to the selected cell even before data out occurs. The minimum specification on t_{RWD} and t_{CWD} assure that data out does occur. In this case, the data in is set up with respect to write ($\overline{\text{W}}$) clock active edge.

PAGE-MODE CYCLES

Page mode operation allows faster successive data operations at the 128 column locations. Page access (t_{CAC}) is typically half the regular $\overline{\text{RAS}}$ clock access (t_{RAC}) on the Motorola 64K dynamic RAM. Page mode operation consists of holding the $\overline{\text{RAS}}$ clock active while cycling the $\overline{\text{CAS}}$ clock to access the column locations determined by the 8-bit column address field. There are two controlling factors that limit the access to all 128 column locations in one $\overline{\text{RAS}}$ clock active operation. These are the refresh interval of the device (2 ms/128 = 15.6 microseconds) and the maximum active time specification for the $\overline{\text{RAS}}$ clock (10 microseconds). Since 10 microseconds is the smaller value, the maximum specification of the $\overline{\text{RAS}}$ clock on time is the limiting factor of the number of sequential page accesses possible. Ten microseconds will provide approximately 50 successive page accesses (10 microseconds ÷ page mode cycle time) for each row address selected before the $\overline{\text{RAS}}$ clock is reset.

The page cycle is always initiated with a row address being provided and latched by the $\overline{\text{RAS}}$ clock, followed by the column address and $\overline{\text{CAS}}$ clock. From the timing illustrated, the initial cycle is a normal read or write cycle, that has been previously described, followed by the shorter $\overline{\text{CAS}}$ cycles (t_{PC}). The $\overline{\text{CAS}}$ cycle time (t_{PC}) consists of the $\overline{\text{CAS}}$ clock active time (t_{CAS}), and $\overline{\text{CAS}}$ clock precharge time (t_{CP}) and two transitions. In addition to read and write cycles, a read-modify-write cycle can also be performed in a page mode operation. For a read-modify-write or read-while-write type cycle, the conditions normal to that mode of operation will apply in the page mode also. The page mode cycle illustrated show a series of sequential reads separated by a series of sequential writes. This is just one mode of operation. In practice, any combination of read, write and read-modify-write cycles can be performed to suit a particular application.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to

degrade with time and temperature. Therefore, to retain the correct information, the bits need to be refreshed at least once every 2 ms. This is accomplished by sequentially cycling through the 128 row address locations every 2 ms, or at least one row every 15.6 microseconds. A normal read or write operation is to RAM will serve to refresh all the bits (256) associated with that particular row decoded.

$\overline{\text{RAS}}$ Only Refresh — When the memory component is in standby the $\overline{\text{RAS}}$ only refresh scheme is employed. This refresh method performs a $\overline{\text{RAS}}$ only cycle on all 128 row addresses every 2 ms. The row addresses are latched in with the $\overline{\text{RAS}}$ clock, and the associated internal row locations are refreshed. As the heading implies, the $\overline{\text{CAS}}$ clock is not required and should be inactive or at a V_{IH} level to conserve power.

Auto Refresh Mode and Self Refresh Mode (MCM6632A only) — With the MCM6632A, two additional refresh methods are available to the user. These special functions are incorporated on pin 1 of the device and have been approved by JEDEC as an alternative function for that pin on the 32K dynamic memory. The auto refresh mode is accomplished by asserting pin 1 active (V_{IL} level) during the time interval when there are no memory cycles. In the auto refresh mode, the $\overline{\text{REFRESH}}$ active pulse (t_{FP}) must be limited to 2 microseconds or less. The 2 microsecond time is specified to prevent the device from transitioning into the self refresh mode. Auto refresh can be performed in a distributed mode (refresh cycle every 15.6 microseconds) and in a burst mode where all 128 refresh cycles are done one after the other until complete. An onboard address counter generates the internal row address to refresh a particular row and increments itself at the end of each cycle.

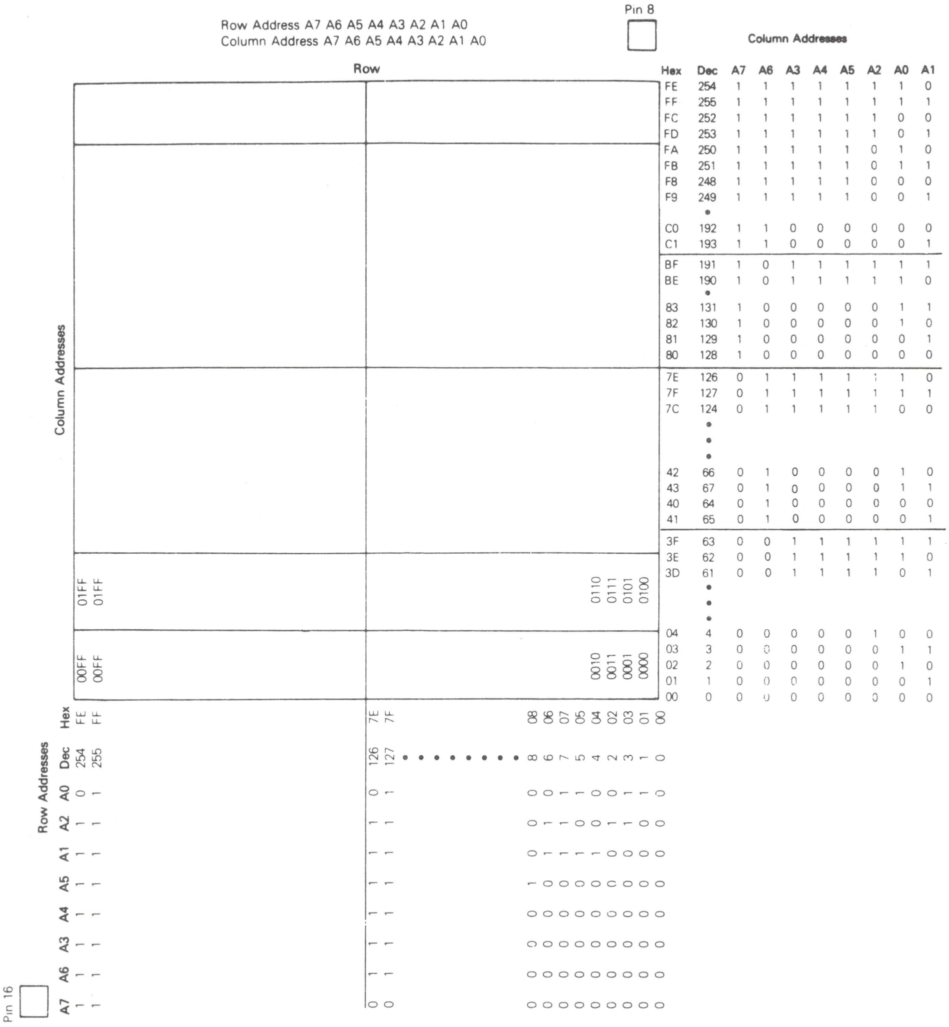
Another variation of refresh is the self refresh mode. This mode is similar to the auto refresh method except that the active pulse width (t_{FBP}) must be greater than 2 microseconds or held down active indefinitely. With pin 1 in the self refresh mode, an internal row address is generated by the internal refresh counter approximately every 15.6 microseconds. This mode of refresh is used for systems requiring battery back-up, and saves additional system power by not requiring an external refresh address counter and address buffers. The power dissipation for either $\overline{\text{REFRESH}}$ mode is the same.

ORDERING INFORMATION

Part Number	Description	Speed	Marking*
MCM6632AL15	32K Dynamic	150	MCM66320AL15/MCM66321AL15
MCM66320AL15	Random Access	150	MCM66320AL15
MCM66321AL15	Memory	150	MCM66321AL15
MCM6632AL20	Sidebraze	200	MCM66320AL20/MCM66321AL20
MCM66320AL20	Package "L"	200	MCM66320AL20
MCM66321AL20		200	MCM66321AL20

*MCM66320A = Tie A7 CAS (A15) Low "0"
MCM66321A = Tie A7 CAS (A15) High "1"

MCM6664A BIT ADDRESS MAP


Pin 8
Row Address A7 A6 A5 A4 A3 A2 A1 A0
Column Address A7 A6 A5 A4 A3 A2 A1 A0
Row
Column Addresses
01FF
01FF
0110
0111
0101
0100
00FF
00FF
0010
0011
0001
0000
Row Addresses
Pin 16

Column Addresses

Hex	Dec	A7	A6	A3	A4	A5	A2	A0	A1
FE	254	1	1	1	1	1	1	1	0
FF	255	1	1	1	1	1	1	1	1
FC	252	1	1	1	1	1	1	0	0
FD	253	1	1	1	1	1	1	0	1
FA	250	1	1	1	1	1	0	1	0
FB	251	1	1	1	1	1	0	1	1
F8	248	1	1	1	1	1	0	0	0
F9	249	1	1	1	1	1	0	0	1
	•								
C0	192	1	1	0	0	0	0	0	0
C1	193	1	1	0	0	0	0	0	1
BF	191	1	0	1	1	1	1	1	1
BE	190	1	0	1	1	1	1	1	0
	•								
83	131	1	0	0	0	0	0	1	1
82	130	1	0	0	0	0	0	1	0
81	129	1	0	0	0	0	0	0	1
80	128	1	0	0	0	0	0	0	0
7E	126	0	1	1	1	1	1	1	0
7F	127	0	1	1	1	1	1	1	1
7C	124	0	1	1	1	1	1	0	0
	•								
	•								
	•								
42	66	0	1	0	0	0	0	1	0
43	67	0	1	0	0	0	0	1	1
40	64	0	1	0	0	0	0	0	0
41	65	0	1	0	0	0	0	0	1
3F	63	0	0	1	1	1	1	1	1
3E	62	0	0	1	1	1	1	1	0
3D	61	0	0	1	1	1	1	0	1
	•								
	•								
	•								
04	4	0	0	0	0	0	1	0	0
03	3	0	0	0	0	0	0	1	1
02	2	0	0	0	0	0	0	1	0
01	1	0	0	0	0	0	0	0	1
00	0	0	0	0	0	0	0	0	0

Row Addresses

Hex	Dec	A0	A2	A1	A5	A4	A3	A6	A7
FE	254	0	1	1	1	1	1	1	1
FF	255	1	1	1	1	1	1	1	1
7E	126	0	1	1	1	1	1	1	0
7F	127	1	1	1	1	1	1	1	0
	• • • • • • • •								
08	8	0	0	0	1	0	0	0	0
06	6	0	1	1	0	0	0	0	0
07	7	1	1	1	0	0	0	0	0
05	5	1	0	1	0	0	0	0	0
04	4	0	0	1	0	0	0	0	0
02	2	0	1	0	0	0	0	0	0
03	3	1	1	0	0	0	0	0	0
01	1	1	0	0	0	0	0	0	0
00	0	0	0	0	0	0	0	0	0

Data Stored = $D_{in} \oplus A_{0X} \oplus A_{1Y}$

Column Address A1	Row Address A0	Data Stored
0	0	True
0	1	Inverted
1	0	Inverted
1	1	True

MOTOROLA

MCM6633A

32K BIT DYNAMIC RAM

The MCM6633A is a 32,768 bit, high-speed, dynamic Random-Access Memory. Organized as 32,768 one-bit words and fabricated using HMOS high-performance N-channel silicon-gate technology. This new breed of 5-volt only dynamic RAM combines high performance with low cost and improved reliability.

By multiplexing row- and column-address inputs, the MCM6633A requires only eight address lines and permits packaging in standard 16-pin dual-in-line packages. Complete address decoding is done on chip with address latches incorporated. Data out is controlled by $\overline{\text{CAS}}$ allowing for greater system flexibility.

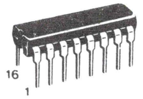
All inputs and outputs, including clocks, are fully TTL compatible. The MCM6633A incorporates a one-transistor cell design and dynamic storage techniques.

- Organized as 32,768 Words of 1 Bit
- Single +5 V Operation (±10%)
- Full Power Supply Range Capabilities
- Maximum Access Time
  MCM6633A-12 = 120 ns
  MCM6633A-15 = 150 ns
  MCM6633A-20 = 200 ns
- Low Power Dissipation
  302.5 mW Maximum (Active) (MCM6633A-15)
  22 mW Maximum (Standby)
- Three-State Data Output
- Internal Latches for Address and Data Input
- Early-Write Common I/O Capability
- 16K Compatible 128-Cycle, 2 ms Refresh
- $\overline{\text{RAS}}$-only Refresh Mode
- $\overline{\text{CAS}}$ Controlled Output
- Upward Pin Compatible from the 16K RAM (MCM4116, MCM4517)
- Fast Page Mode Cycle Time
- Low Soft Error Rate <0.1% per 1000 Hours (See Soft Error Testing)
- One Half of the 64K Dynamic RAM MCM6665A
- The Operating Half of the MCM6633A is Indicated By Device Marking: MCM66330A TIE A7 $\overline{\text{CAS}}$ (A15) Low "0"; MCM66331A TIE A7 $\overline{\text{CAS}}$ (A15) High "1"

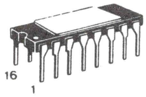
MOS

(N-CHANNEL, SILICON-GATE)

32,768-BIT DYNAMIC RANDOM ACCESS MEMORY

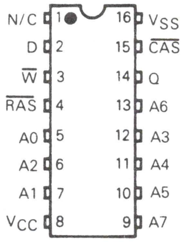


P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 690

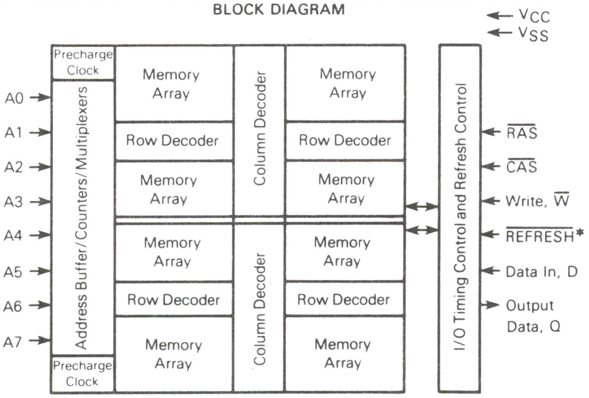
PIN ASSIGNMENT


N/C 1
D 2
$\overline{\text{W}}$ 3
$\overline{\text{RAS}}$ 4
A0 5
A2 6
A1 7
V_{CC} 8
16 V_{SS}
15 $\overline{\text{CAS}}$
14 Q
13 A6
12 A3
11 A4
10 A5
9 A7

PIN NAMES

A0-A7	Address Input
D	Data In
Q	Data Out
$\overline{\text{W}}$	Read/Write Input
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
V_{CC}	Power (+5 V)
V_{SS}	Ground

BLOCK DIAGRAM


V_{CC}
V_{SS}
Precharge Clock
A0
A1
A2
A3
A4
A5
A6
A7
Address Buffer/Counters/Multiplexers
Precharge Clock
Memory Array
Row Decoder
Memory Array
Memory Array
Row Decoder
Memory Array
Column Decoder
Memory Array
Row Decoder
Memory Array
Memory Array
Row Decoder
Memory Array
Column Decoder
I/O Timing Control and Refresh Control
$\overline{\text{RAS}}$
$\overline{\text{CAS}}$
Write, $\overline{\text{W}}$
$\overline{\text{REFRESH}}$*
Data In, D
Output Data, Q

*Refresh Function Available on MCM6632A

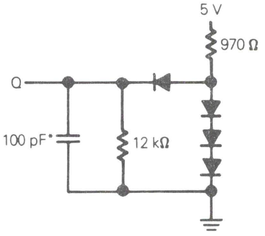
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS} (except V_{CC})	V_{in}, V_{out}	−2 to +7	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Power Dissipation	P_D	1.0	W
Data Out Current	I_{out}	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

FIGURE 1 — OUTPUT LOAD



*Includes Jig Capacitance

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	MCM6633A-12, -15, -20	V_{CC}	4.5	5.0	5.5	V	1
		V_{SS}	0	0	0	V	1
Logic 1 Voltage, All Inputs		V_{IH}	2.4	–	$V_{CC}+1$	V	1
Logic 0 Voltage, All Inputs		V_{IL}	−1.0*	–	0.8	V	1

*The device will withstand undershoots to the −2 volt level with a maximum pulse width of 20 ns at the −1.5 volt level. This is periodically sampled rather than 100% tested.

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Units	Notes
V_{CC} Power Supply Current (Standby)	I_{CC2}	–	4.0	mA	5
V_{CC} Power Supply Current 6633A-12, $t_{RC}=250$ ns 6633A-15, $t_{RC}=270$ ns 6633A-20, $t_{RC}=330$ ns	I_{CC1}	– – –	60 55 50	mA	4
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles 6633A-12, $t_{RC}=250$ ns 6633A-15, $t_{RC}=270$ ns 6633A-20, $t_{RC}=330$ ns	I_{CC3}	– – –	50 45 40	mA	4
V_{CC} Power Supply Current During Page Mode Cycle for $t_{RAS}=10$ μsec 6633A-12, $t_{PC}=t_{RP}=120$ ns 6633A-15, $t_{PC}=t_{RP}=145$ ns 6633A-20, $t_{PC}=t_{RP}=200$ ns	I_{CC4}	– – –	45 40 35	mA	4
Input Leakage Current ($V_{SS} \leq V_{in} \leq V_{CC}$)	$I_{I(L)}$	–	10	μA	–
Output Leakage Current ($\overline{CAS}$ at logic 1, $V_{SS} \leq V_{out} \leq V_{CC}$)	$I_{O(L)}$	–	10	μA	–
Output Logic 1 Voltage @ $I_{out}=-4$ mA	V_{OH}	2.4	–	V	–
Output Logic 0 Voltage @ $I_{out}=4$ mA	V_{OL}	–	0.4	V	–

CAPACITANCE (f = 1.0 MHz, $T_A=25$°C, $V_{CC}=5$ V Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit	Notes
Input Capacitance (A0-A7), D	C_{I1}	3	5	pF	7
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	C_{I2}	6	8	pF	7
Output Capacitance (Q), ($\overline{CAS}=V_{IH}$ to disable output)	C_O	5	7	pF	7

NOTES:
1. All voltages referenced to V_{SS}.
2. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
3. An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is guaranteed
4. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
5. $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1.
6. The transition time specification applies for all inputs signals. In addition to meeting the transition rate specification, all input signals must transmit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
7. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C=\frac{I\Delta t}{\Delta V}$

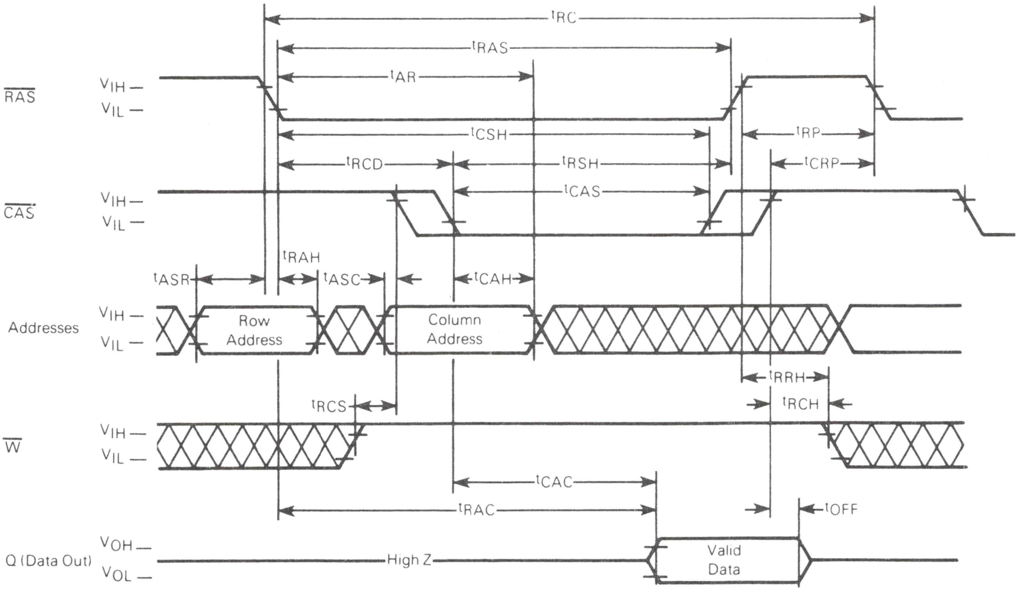
AC OPERATING CONDITIONS AND CHARACTERISTICS (Read, Write, and Read-Modify-Write Cycles)

(Full Operating Voltage and Temperature Range Unless Otherwise Noted; See Notes 2, 3, 6, and Figure 1)

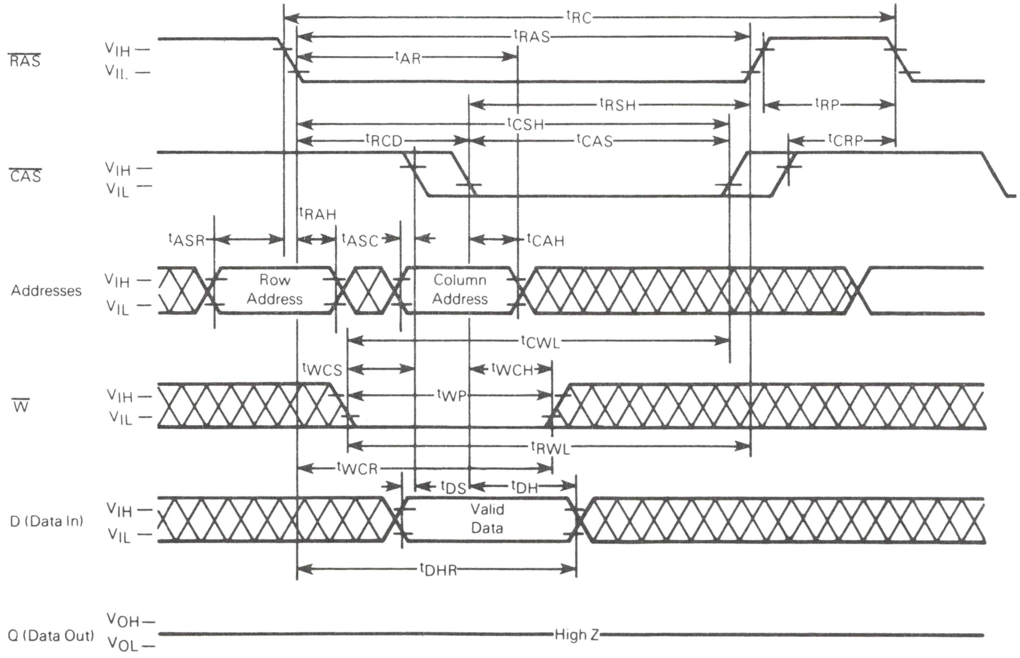
Parameter	Symbol	6633A-12		6633A-15		6633A-20		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	250	–	270	–	330	–	ns	8, 9
Read Write Cycle Time	t_{RWC}	255	–	280	–	345	–	ns	8, 9
Access Time from Row Address Strobe	t_{RAC}	–	120	–	150	–	200	ns	10, 12
Access Time from Column Address Strobe	t_{CAC}	–	60	–	75	–	100	ns	11, 12
Output Buffer and Turn-Off Delay	t_{OFF}	0	30	0	30	0	40	ns	18
Row Address Strobe Precharge Time	t_{RP}	100	–	100	–	120	–	ns	–
Row Address Strobe Pulse Width	t_{RAS}	120	10000	150	10000	200	10000	ns	–
Column Address Strobe Pulse Width	t_{CAS}	60	10000	75	10000	100	10000	ns	–
Row to Column Strobe Lead Time	t_{RCD}	25	60	30	75	35	100	ns	13
Row Address Setup Time	t_{ASR}	0	–	0	–	0	–	ns	–
Row Address Hold Time	t_{RAH}	15	–	20	–	25	–	ns	–
Column Address Setup Time	t_{ASC}	0	–	0	–	0	–	ns	–
Column Address Hold Time	t_{CAH}	25	–	35	–	45	–	ns	–
Column Address Hold Time Referenced to $\overline{RAS}$	t_{AR}	85	–	95	–	120	–	ns	17
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	6
Read Command Setup Time	t_{RCS}	0	–	0	–	0	–	ns	–
Read Command Hold Time	t_{RCH}	0	–	0	–	0	–	ns	14
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	0	–	ns	14
Write Command Hold Time	t_{WCH}	25	–	35	–	45	–	ns	–
Write Command Hold Time Referenced to $\overline{RAS}$	t_{WCR}	85	–	95	–	120	–	ns	17
Write Command Pulse Width	t_{WP}	25	–	35	–	45	–	ns	–
Write Command to Row Strobe Lead Time	t_{RWL}	40	–	45	–	55	–	ns	–
Write Command to Column Strobe Lead Time	t_{CWL}	40	–	45	–	55	–	ns	–
Data in Setup Time	t_{DS}	0	–	0	–	0	–	ns	15
Data in Hold Time	t_{DH}	25	–	35	–	45	–	ns	15
Data in Hold Time Referenced to $\overline{RAS}$	t_{DHR}	85	–	95	–	120	–	ns	17
Column to Row Strobe Precharge Time	t_{CRP}	– 10	–	– 10	–	– 10	–	ns	–
$\overline{RAS}$ Hold Time	t_{RSH}	60	–	75	–	100	–	ns	–
Refresh Period	t_{RFSH}	–	2.0	–	2.0	–	2.0	ms	–
$\overline{WRITE}$ Command Setup Time	t_{WCS}	– 10	–	– 10	–	– 10	–	ns	16
$\overline{CAS}$ to $\overline{WRITE}$ Delay	t_{CWD}	40	–	45	–	55	–	ns	16
$\overline{RAS}$ to $\overline{WRITE}$ Delay	t_{RWD}	100	–	120	–	155	–	ns	16
$\overline{CAS}$ Hold Time	t_{CSH}	120	–	150	–	200	–	ns	–
$\overline{CAS}$ Precharge Time (Page Mode Cycle Only)	t_{CP}	50	–	60	–	80	–	ns	–
Page Mode Cycle Time	t_{PC}	120	–	145	–	200	–	ns	–

8. The specifications for t_{RC} (min), and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
9. AC measurements $t_T = 5.0$ ns.
10. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
11. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
12. Measured with a current load equivalent to 2 TTL (-200 µA, $+4$ mA) loads and 100 pF with the data output trip points set at $V_{OH} = 2.0$ V and $V_{OL} = 0.8$ V.
13. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
16. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
17. t_{AR} min $\leq t_{AR} = t_{RCD} + t_{CAH}$
    t_{DHR} min $\leq t_{DHR} = t_{RCD} + t_{DH}$
    t_{WCR} min $\leq t_{WCR} = t_{RCD} + t_{WCH}$
18. t_{off} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

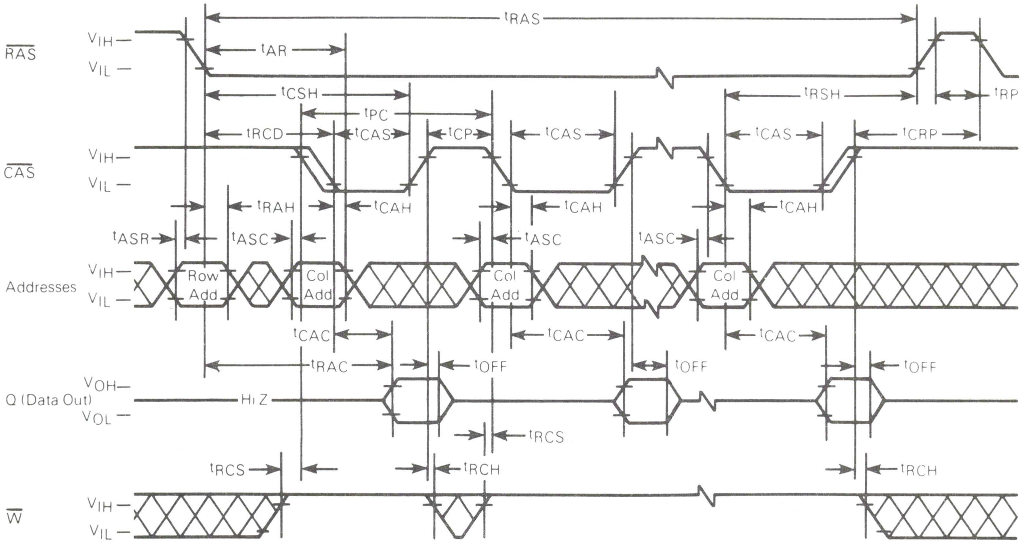
READ CYCLE TIMING


tRC
tRAS
tAR
RAS
VIH
VIL
tCSH
tRP
tRCD
tRSH
tCRP
tCAS
CAS
VIH
VIL
tRAH
tASR
tASC
tCAH
Addresses
VIH
VIL
Row Address
Column Address
tRRH
tRCS
tRCH
W
VIH
VIL
tCAC
tRAC
tOFF
Q (Data Out)
VOH
VOL
High Z
Valid Data

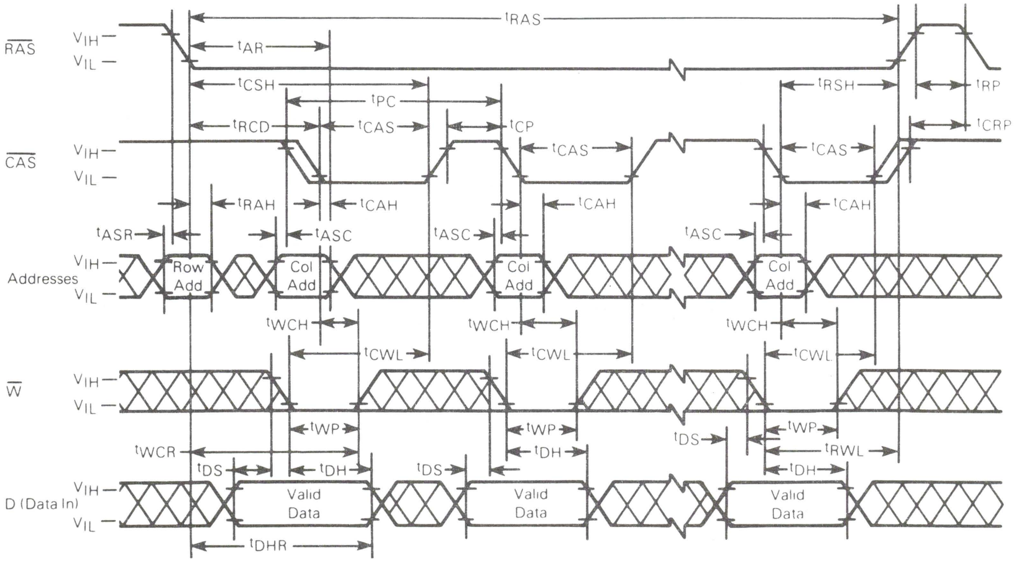
WRITE CYCLE TIMING


tRC
tRAS
tAR
RAS
VIH
VIL
tRSH
tRP
tCSH
tRCD
tCAS
tCRP
CAS
VIH
VIL
tRAH
tASR
tASC
tCAH
Addresses
VIH
VIL
Row Address
Column Address
tCWL
tWCS
tWCH
tWP
W
VIH
VIL
tRWL
tWCR
tDS
tDH
D (Data In)
VIH
VIL
Valid Data
tDHR
Q (Data Out)
VOH
VOL
High Z

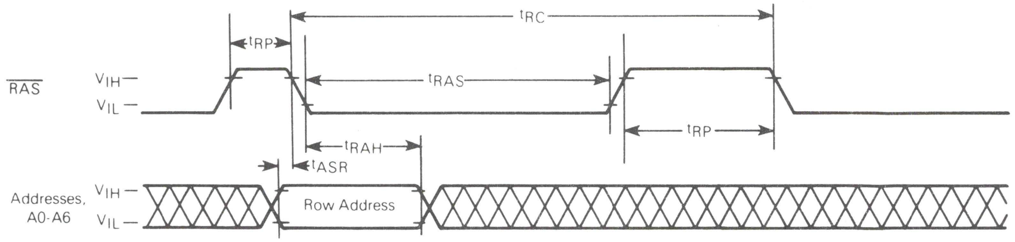
PAGE MODE READ CYCLE


tRAS
RAS
VIH
VIL
tAR
tCSH
tRSH
tRP
tPC
tRCD
tCAS
tCP
tCAS
tCAS
tCRP
CAS
VIH
VIL
tRAH
tCAH
tCAH
tCAH
tASR
tASC
tASC
tASC
Addresses
VIH
VIL
Row Add
Col Add
Col Add
Col Add
tCAC
tCAC
tCAC
tRAC
tOFF
tOFF
tOFF
Q (Data Out)
VOH
VOL
Hi Z
tRCS
tRCS
tRCH
tRCH
W
VIH
VIL

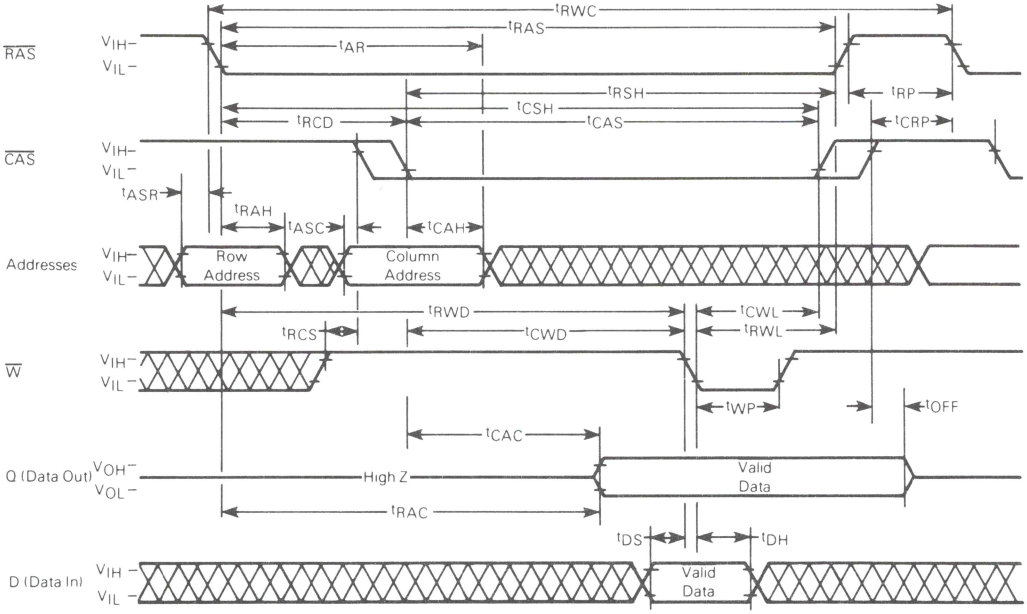
PAGE MODE WRITE CYCLE


tRAS
RAS
VIH
VIL
tAR
tCSH
tRSH
tRP
tPC
tRCD
tCAS
tCP
tCRP
CAS
VIH
VIL
tCAS
tCAS
tRAH
tCAH
tCAH
tCAH
tASR
tASC
tASC
tASC
Addresses
VIH
VIL
Row Add
Col Add
Col Add
Col Add
tWCH
tWCH
tWCH
tCWL
tCWL
tCWL
W
VIH
VIL
tWP
tWP
tWP
tDS
tRWL
tWCR
tDH
tDH
tDH
tDS
tDS
D (Data In)
VIH
VIL
Valid Data
Valid Data
Valid Data
tDHR

RAS-ONLY REFRESH CYCLE
(Data-in and Write are Don't Care, CAS is HIGH)


tRC
tRP
RAS
VIH
VIL
tRAS
tRP
tRAH
tASR
Addresses, A0-A6
VIH
VIL
Row Address

READ-WRITE/READ-MODIFY-WRITE CYCLE


tRWC
tRAS
tAR
RAS
VIH
VIL
tRSH
tCSH
tRP
tRCD
tCAS
tCRP
CAS
VIH
VIL
tASR
tRAH
tASC
tCAH
Addresses
VIH
VIL
Row Address
Column Address
tRWD
tCWL
tRCS
tCWD
tRWL
W
VIH
VIL
tWP
tOFF
tCAC
Q (Data Out)
VOH
VOL
High Z
Valid Data
tRAC
tDS
tDH
D (Data In)
VIH
VIL
Valid Data

TYPICAL CHARACTERISTICS

FIGURE 2 — $\overline{\text{RAS}}$ ACCESS TIME versus SUPPLY VOLTAGE

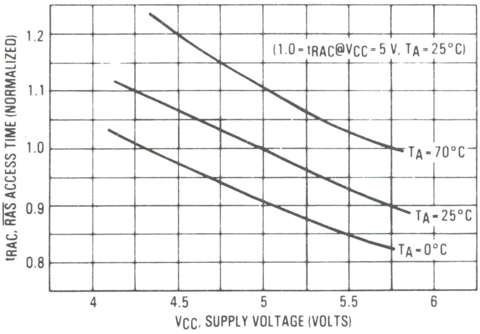


FIGURE 3 — $\overline{\text{CAS}}$ ACCESS TIME versus SUPPLY VOLTAGE

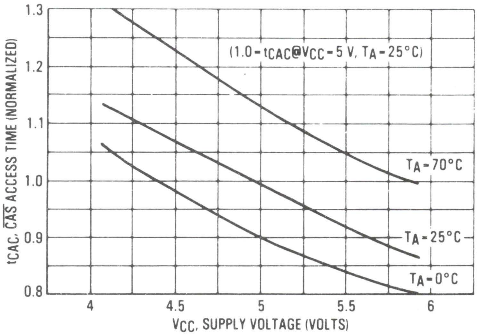


FIGURE 4 — $\overline{\text{RAS}}$ ACCESS TIME versus AMBIENT TEMPERATURE

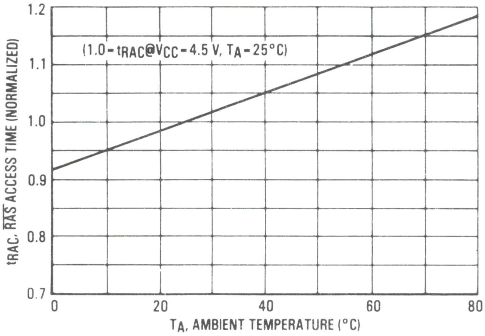


FIGURE 5 — $\overline{\text{CAS}}$ ACCESS TIME versus AMBIENT TEMPERATURE

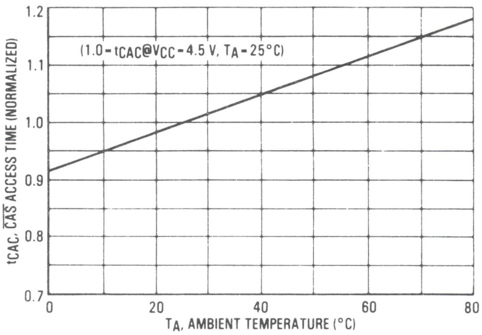


FIGURE 6 — $\overline{\text{RAS}}$, $\overline{\text{W}}$ INPUT LEVEL versus SUPPLY VOLTAGE

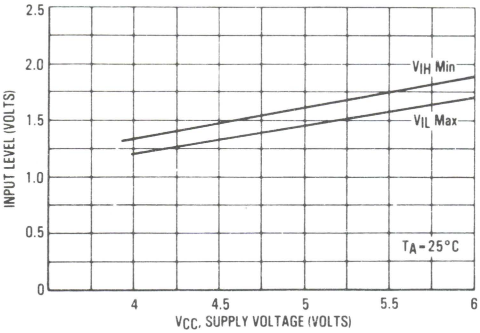
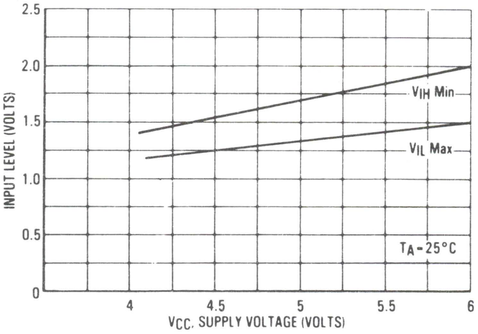


FIGURE 7 — $\overline{\text{CAS}}$, $\overline{\text{W}}$ INPUT LEVEL versus SUPPLY VOLTAGE



TYPICAL CHARACTERISTICS (continued)

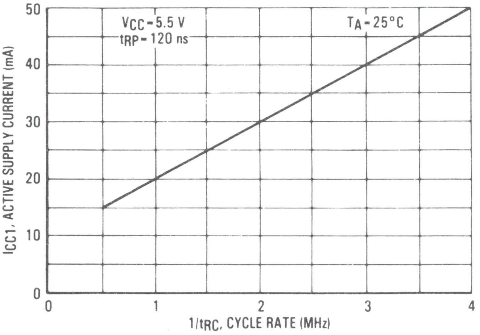


FIGURE 8 — I_{CC1} SUPPLY CURRENT versus CYCLE RATE

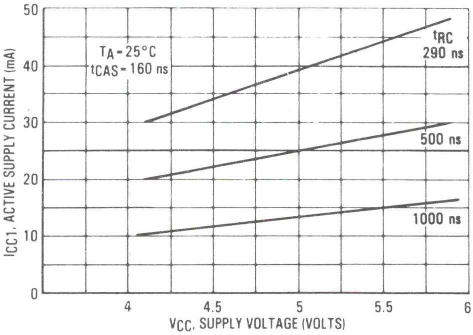


FIGURE 9 — I_{CC1} SUPPLY CURRENT versus SUPPLY VOLTAGE

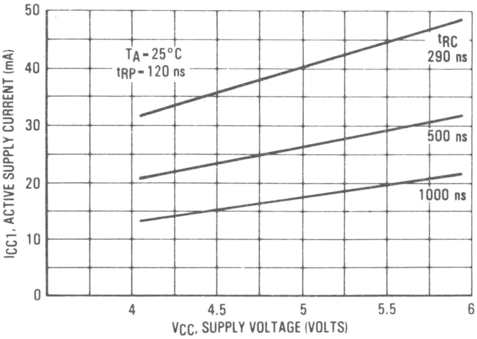


FIGURE 10 — I_{CC1} SUPPLY CURRENT versus SUPPLY VOLTAGE

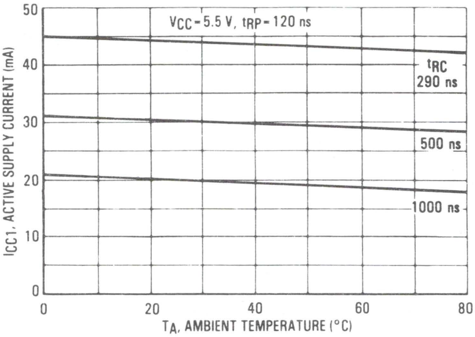


FIGURE 11 — I_{CC1} SUPPLY CURRENT versus AMBIENT TEMPERATURE (min t_{RP})

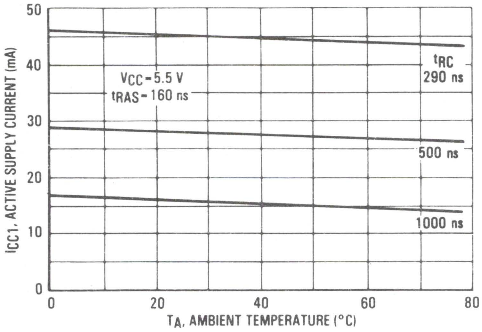


FIGURE 12 — I_{CC1} SUPPLY CURRENT versus AMBIENT TEMPERATURE (min $\overline{RAS}$)

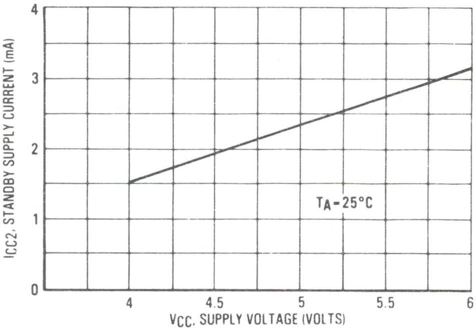


FIGURE 13 — I_{CC2} SUPPLY CURRENT versus SUPPLY VOLTAGE

TYPICAL CHARACTERISTICS (continued)

FIGURE 14 — I_{CC2} STANDBY CURRENT versus AMBIENT TEMPERATURE

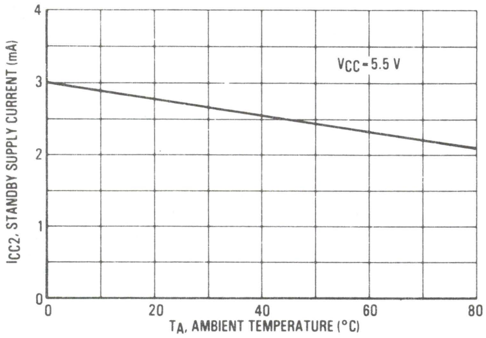


FIGURE 15 — I_{CC3} SUPPLY CURRENT versus CYCLE RATE

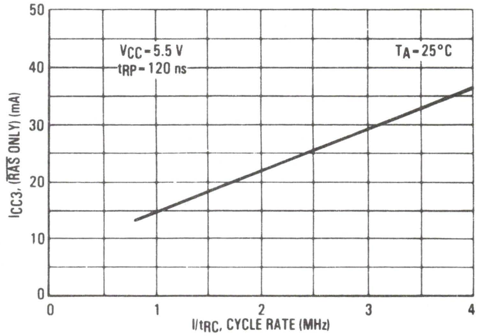


FIGURE 16 — ADDRESS INPUT LEVEL versus SUPPLY VOLTAGE

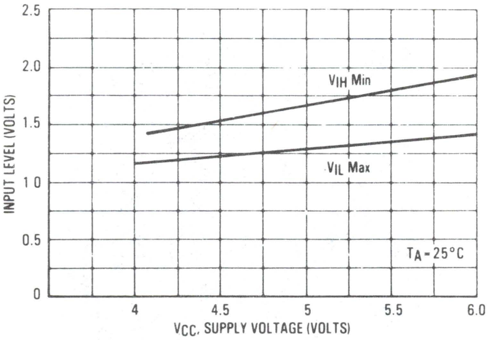
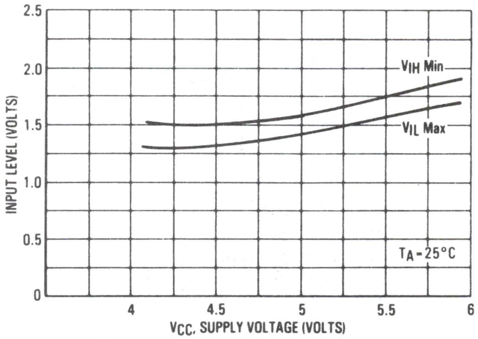


FIGURE 17 — DATA INPUT LEVEL versus SUPPLY VOLTAGE



SOFT ERROR TESTING

The storage cell depletion regions as well as the sense amplifier and its associated bit lines are susceptible to charge collection of electrons from an alpha "hit." However, the susceptibility of these vulnerable regions varies. Depleted storage cells are vulnerable at all times, whereas the sense amplifiers and associated bit lines are susceptible only during the small portion of the memory cycle just prior to sensing. Hence, an increase in the frequency of dynamic RAM access will cause a corresponding increase in the soft error rate.

To take this memory access dependency into account, the total soft error rate profile includes a cycle time component. The soft error rate due to bit line hits at the system's memory cycle rate is added to the soft error rate due to storage cell hits which are not frequency dependent. Figure 18 illustrates the impact that frequency of access has on the MCM6664A/MCM6665A overall soft error rate.

Under normal operating conditions, the die will be exposed to radiation levels of less than 0.01 alpha/cm^2/hr. Accelerated soft error testing data is generated from at least three high-intensity sources having an Alpha Flux Density range of 1×10^5 to 6×10^5 (alpha/cm^{2}hr) placed over uncoated die. Figure 19 shows the soft error rate for a given alpha flux density at a cycle rate of 100 kHz. The accelerated data of Figures 18 and 19 project that the soft error rate for package level radiation will be less than 0.1%/1000 hours.

SYSTEM LIFE OPERATING TEST CONDITIONS

1) Cycle time: 1 microsecond for read, write and refresh cycles
2) Refresh Rate: 1 millisecond
3) Voltage: 5.0 V
4) Temperature: 30° C ± 2° C (ambient temperature inside enclosure)
5) Elevation: Approximately 620 feet above mean sea level
6) Data Patterns: Write the entire memory space sequentially with all "1"s and then perform continuous sequential reads for 6 hours. Next, write the entire memory space with all "0"s sequentially and then perform continuous sequential reads for 6 hours. Next, go back to the all "1"s pattern and repeat the sequences all over again.

FIGURE 18 — ACCELERATED SOFT ERROR versus CYCLE TIME

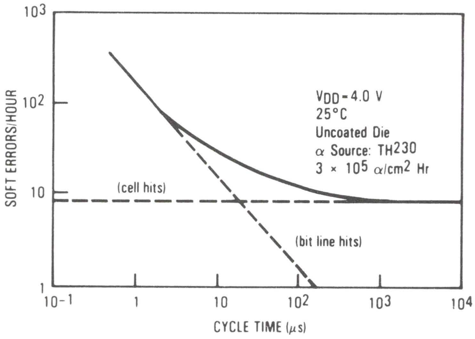
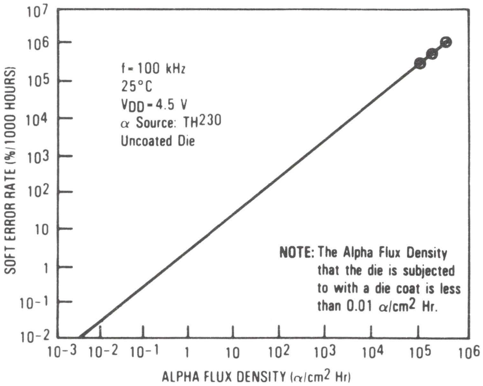


FIGURE 19 — SOFT ERROR RATE versus ALPHA FLUX DENSITY



CURRENT WAVEFORMS

FIGURE 20 — $\overline{\text{RAS}}/\overline{\text{CAS}}$ CYCLE

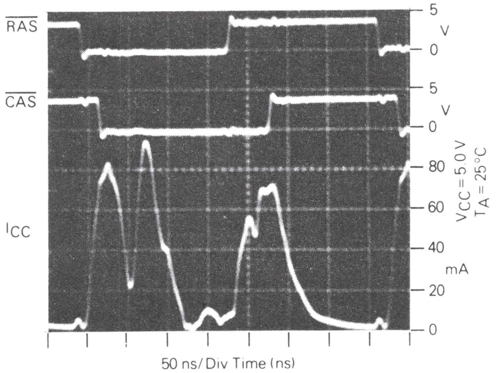


FIGURE 21 — LONG $\overline{\text{RAS}}/\overline{\text{CAS}}$ CYCLE

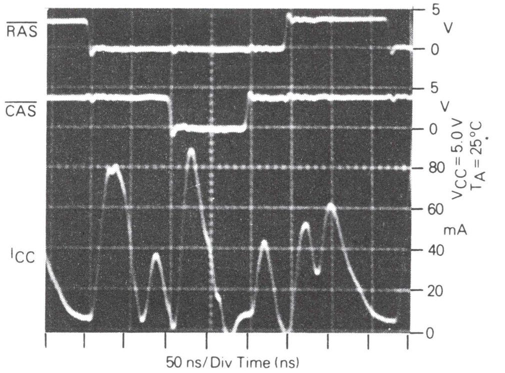


FIGURE 22 — $\overline{\text{RAS}}$ ONLY CYCLE

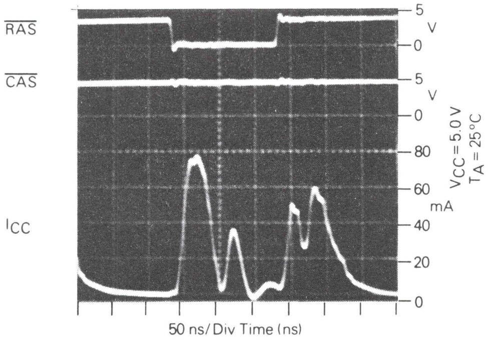


FIGURE 23 — PAGE MODE CYCLE

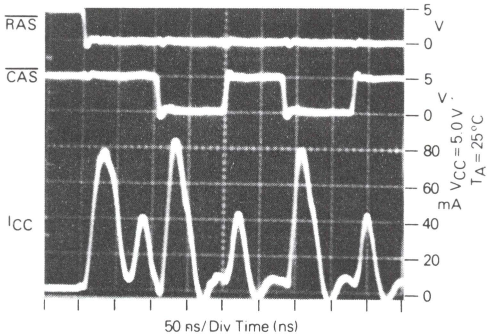
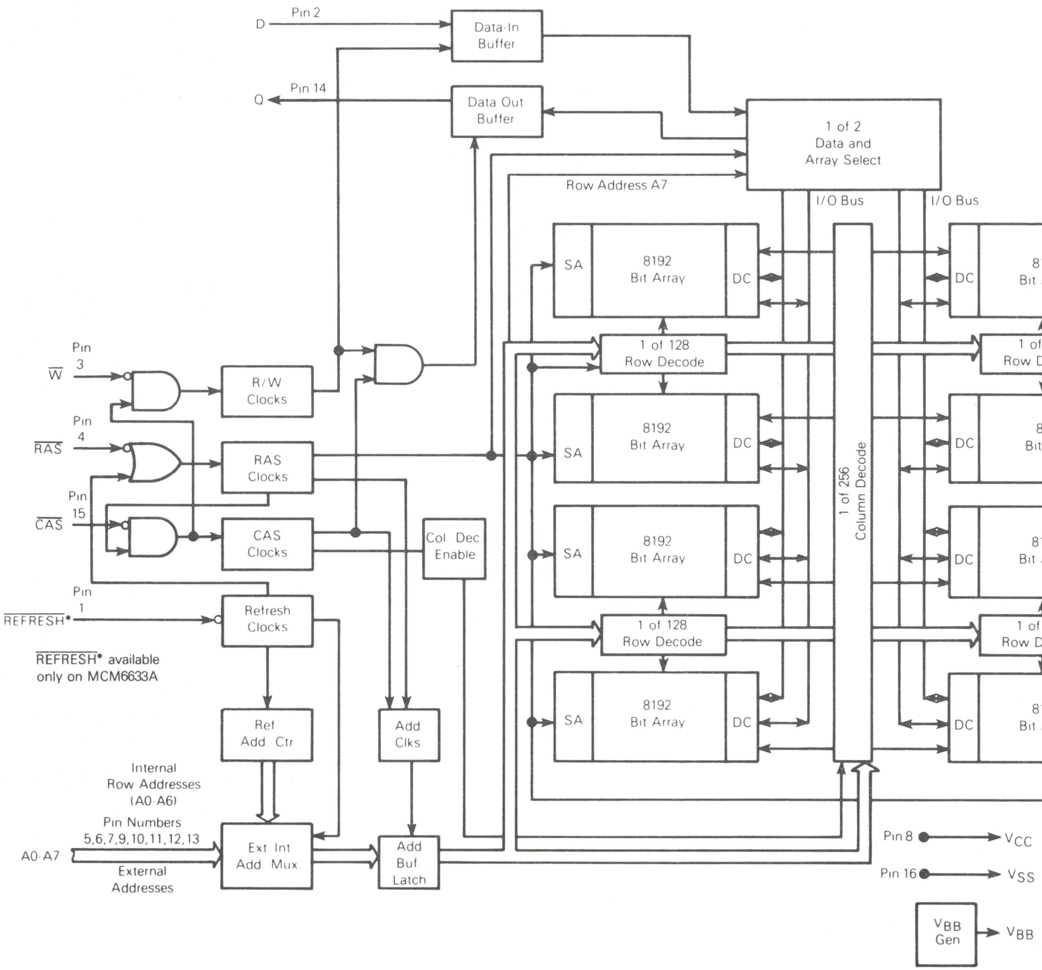


FIGURE 24 — FUNCTIONAL BLOCK DIAGRAM


D
Pin 2
Data-In Buffer
Q
Pin 14
Data Out Buffer
1 of 2 Data and Array Select
Row Address A7
I/O Bus
I/O Bus
SA
8192 Bit Array
DC
1 of 128 Row Decode
1 of 256 Column Decode
Pin 3
$\overline{W}$
Pin 4
$\overline{RAS}$
Pin 15
$\overline{CAS}$
Pin 1
$\overline{REFRESH}$*
R/W Clocks
RAS Clocks
CAS Clocks
Col Dec Enable
Refresh Clocks
$\overline{REFRESH}$* available only on MCM6633A
Ref Add Ctr
Add Clks
Internal Row Addresses (A0-A6)
Pin Numbers 5,6,7,9,10,11,12,13
A0-A7
External Addresses
Ext Int Add Mux
Add Buf Latch
Pin 8
V_{CC}
Pin 16
V_{SS}
V_{BB} Gen
V_{BB}

DEVICE INITIALIZATION

Since the 32K dynamic RAM is a single supply 5 V only device, the need for power supply sequencing is no longer required as was the case in older generation dynamic RAMs. On power-up an initial pause of 100 microseconds is required for the internal substrate generator pump to establish the correct bias voltage. This is to be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize the various dynamic nodes internal to the device. During an extended inactive state of the device (greater than 2 ms with device powered up) the wake up sequence (8 active cycles) will be necessary to assure proper device operation. See Figures 25 and 26 for power on characteristics of the RAM for two conditions (clocks active, clocks inactive).

The row address strobe is the primary "clock" that activates the device and maintains the data when the RAM is in the standby mode. This is the main feature that distinquishes it as a dynamic RAM as opposed to a static RAM. A dynamic RAM is placed in a low power standby mode when the device receives a positive-going row address strobe. The variation in the power dissipation of a dynamic RAM from the active to the standby state is an order of magnitude or more for NMOS devices. This feature is used to its fullest advantage with high density mainframe memory systems, where only a very small percentage of the devices are in the active mode at any one time and the rest of the devices are in the standby mode. Thus, large memory systems can be assembled that dissipate very low power per bit compared to a system where all devices are active continuously.

ADDRESSING THE RAM

The eight address pins on the device are time multiplexed with two separate 8-bit address fields that are strobed at the beginning of the memory cycle by two clocks (active negative) called the row address strobe and the column address strobe. A total of fifteen address bits will decode one of the 32,768 cell locations in the device. The column address strobe follows the row address strobe by a specified minimum and maximum time called "t_{RCD}," which is the row to column strobe delay. This time interval is also referred to as the multiplex window which gives flexibility to a system designer to set up his external addresses into the RAM. These conditions have to be met for normal read or write cycles. This initial portion of the cycle accomplishes the normal addressing of the device. There are, however, two other variations in addressing the 32K RAM, one is called the page mode cycle (described later) where an 8-bit column address field is presented on the input pins and latched by the $\overline{CAS}$ clock; and the other is the $\overline{RAS}$ only refresh cycle (described later) where a 7-bit row address field is presented on the input pins and latched by the $\overline{RAS}$ clock. In the latter case, the most significant bit on Row Address A7 (pin 9) is not required for refresh. See bit address map for the topology of the cells and their address selection.

NORMAL READ CYCLE

A read cycle is referred to as normal read cycle to differentiate it from a page-mode-read cycle, a read-while-write cycle, and read-modify-write cycle which are covered in a later section.

The memory read cycle begins with the row addresses valid and the $\overline{RAS}$ clock transitioning from V_{IH} to the V_{IL} level. The $\overline{CAS}$ clock must also make a transition from V_{IH} to the V_{IL} level at the specified t_{RCD} timing limits when the column addresses are latched. Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. Also, these clocks are linked in such a manner that the access time of the device is independent of the address multiplex window. The only stipulation is that the $\overline{CAS}$ clock must be active before or at

CURRENT WAVEFORMS

FIGURE 25 — SUPPLY CURRENT versus SUPPLY VOLTAGE DURING POWER UP, $\overline{RAS}$, $\overline{CAS} = V_{CC}$

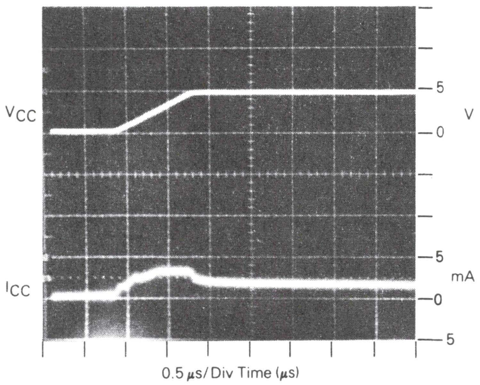
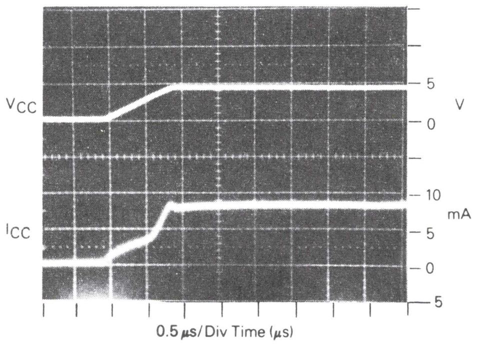


FIGURE 26 — SUPPLY CURRENT versus SUPPLY VOLTAGE DURING POWER UP, $\overline{RAS}$, $\overline{CAS} = V_{SS}$



the t_{RCD} maximum specification for an access (data valid) from the $\overline{\text{RAS}}$ clock edge to be guaranteed (t_{RAC}). If the t_{RCD} maximum condition is not met, the access (t_{CAC}) from the $\overline{\text{CAS}}$ clock active transition will determine read access time. The external $\overline{\text{CAS}}$ signal is ignored until an internal $\overline{\text{RAS}}$ signal is available, as noted in the functional block diagram, Figure 24. This gating feature on the $\overline{\text{CAS}}$ clock will allow the external $\overline{\text{CAS}}$ signal to become active as soon as the row address hold time (t_{RAH}) specification has been met and defines the t_{RCD} minimum specification. The time difference between t_{RCD} minimum and t_{RCD} maximum can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{\text{CAS}}$ clock.

Once the clocks have become active, they must stay active for the minimum (t_{RAS}) period for the $\overline{\text{RAS}}$ clock and the minimum (t_{CAS}) period for the $\overline{\text{CAS}}$ clock. The $\overline{\text{RAS}}$ clock must stay inactive for the minimum (t_{RP}) time. The former is for the completion of the cycle in progress, and the latter is for the device internal circuitry to be precharged for the next active cycle.

Data out is not latched and is valid as long as the $\overline{\text{CAS}}$ clock is active; the output will switch to the three-state mode when the $\overline{\text{CAS}}$ clock goes inactive. The $\overline{\text{CAS}}$ clock can remain active for a maximum of 10 ns (t_{CRP}) into the next cycle. To perform a read cycle, the write ($\overline{\text{W}}$) input must be held at the V_{IH} level from the time the $\overline{\text{CAS}}$ clock makes its active transition (t_{RCS}) to the time when it transitions into the inactive (t_{RCH}) mode.

WRITE CYCLE

A write cycle is similar to a read cycle except that the Write ($\overline{\text{W}}$) clock must go active (V_{IL} level) at or before the $\overline{\text{CAS}}$ clock goes active at a minimum t_{WCS} time. If the above condition is met, then the cycle in progress is referred to as a early write cycle. In an early write cycle, the write clock and the data in is referenced to the active transition of the $\overline{\text{CAS}}$ clock edge. There are two important parameters with respect to the write cycle: the column strobe to write lead time (t_{CWL}) and the row strobe to write lead time (t_{RWL}). These define the minimum time that $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks need to be active after the write operation has started (($\overline{\text{W}}$) clock at V_{IL} level).

It is also possible to perform a late write cycle. For this cycle the write clock is activated after the $\overline{\text{CAS}}$ goes low which is beyond t_{WCS} minimum time. Thus the parameters t_{CWL} and t_{RWL} must be satisfied before terminating this cycle. The difference between an early write cycle and a late write cycle is that in a late write cycle the write ($\overline{\text{W}}$) clock can occur much later in time with respect to the active transition of the $\overline{\text{CAS}}$ clock. This time could be as long as 10 microseconds $- [t_{RWL} + t_{RP} + 2T_t]$.

At the start of a write cycle, the data out is in a three-state condition and remains inactive throughout the cycle. The data out remains three-state because of the active transition of the write ($\overline{\text{W}}$) clock prevents the $\overline{\text{CAS}}$ clock from enabling the data-out buffers as noted in Functional Block Diagram. The three-state condition (high impedence) of the Data Out Pin during a write cycle can be effectively utilized in a systems that has a common input/output bus. The only stipulation is that the system use only early write mode operations for all write cycles to avoid bus contention.

READ-MODIFY-WRITE AND READ-WHILE-WRITE CYLES

As the name implies, both a read and a write cycle is accomplished at a selected bit during a single access. The read-modify-write cycle is similar to the late write cycle discussed above.

For the read-modify-write cycle a normal read cycle is initiated with the write ($\overline{\text{W}}$) clock at the V_{IH} level until the read data occurs at the device access time (t_{RAC}). At this time the write ($\overline{\text{W}}$) clock is asserted. The data in is setup and held with respect to the active edge of the write clock. The cycle described assumes a zero modify time between read and write.

Another variation of the read-modify-write cycle is the read-while-write cycle. For this cycle, the following parameters (t_{RWD}, t_{CWD}) play an important role. A read-while-write cycle starts as a normal read cycle with the write ($\overline{\text{W}}$) clock being asserted at minimum t_{RWD} or minimum t_{CWD} time, depending upon the application. This results in starting a write operation to the selected cell even before data out occurs. The minimum specification on t_{RWD} and t_{CWD} assure that data out does occur. In this case, the data in is set up with respect to write ($\overline{\text{W}}$) clock active edge.

PAGE-MODE CYCLES

Page mode operation allows faster successive data operations at the 128 column locations. Page access (t_{CAC}) is typically half the regular $\overline{\text{RAS}}$ clock access (t_{RAC}) on the Motorola 64K dynamic RAM. Page mode operation consists of holding the $\overline{\text{RAS}}$ clock active while cycling the $\overline{\text{CAS}}$ clock to access the column locations determined by the 8-bit column address field. There are two controlling factors that limit the access to all 128 column locations in one $\overline{\text{RAS}}$ clock active operation. These are the refresh interval of the device (2 ms/128 = 15.6 microseconds) and the maximum active time specification for the $\overline{\text{RAS}}$ clock (10 microseconds). Since 10 microseconds is the smaller value, the maximum specification of the $\overline{\text{RAS}}$ clock on time is the limiting factor of the number of sequential page accesses possible. Ten microseconds will provide approximately 50 successive page accesses (10 microseconds ÷ page mode cycle time) for each row address selected before the $\overline{\text{RAS}}$ clock is reset.

The page cycle is always initiated with a row address being provided and latched by the $\overline{\text{RAS}}$ clock, followed by the column address and $\overline{\text{CAS}}$ clock. From the timing illustrated, the initial cycle is a normal read or write cycle, that has been previously described, followed by the shorter $\overline{\text{CAS}}$ cycles (t_{PC}). The $\overline{\text{CAS}}$ cycle time (t_{PC}) consists of the $\overline{\text{CAS}}$ clock active time (t_{CAS}), and $\overline{\text{CAS}}$ clock precharge time (t_{CP}) and two transitions. In addition to read and write cycles, a read-modify-write cycle can also be performed in a page mode operation. For a read-modify-write or read-while-write type cycle, the conditions normal to that mode of operation will apply in the page mode also. The page mode cycle illustrated show a series of sequential reads separated by a series of sequential writes. This is just one mode of operation. In practice, any combination of read, write and read-modify-write cycles can be performed to suit a particular application.

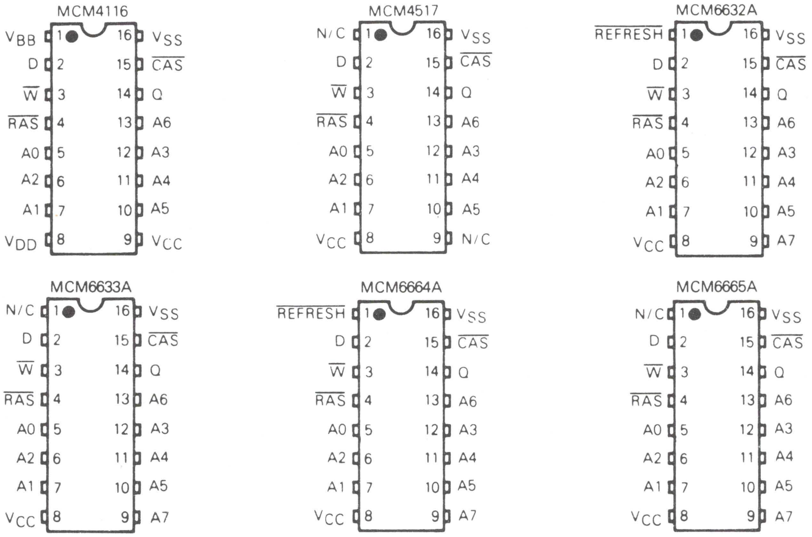
REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to

degrade with time and temperature. Therefore, to retain the correct information, the bits need to be refreshed at least once every 2 ms. This is accomplished by sequentially cycling through the 128 row address locations every 2 ms, or at least one row every 15.6 microseconds. A normal read or write operation to the RAM will serve to refresh all the bits (256) associated with that particular row decoded.

$\overline{\text{RAS}}$ Only Refresh — When the memory component is in standby the $\overline{\text{RAS}}$ only refresh scheme is employed. This refresh method performs a $\overline{\text{RAS}}$ only cycle on all 128 row addresses every 2 ms. The row addresses are latched in with the $\overline{\text{RAS}}$ clock, and the associated internal row locations are refreshed. As the heading implies, the $\overline{\text{CAS}}$ clock is not required and should be inactive or at a V_{IH} level to conserve power.

PIN ASSIGNMENT COMPARISON


MCM4116
VBB 1 16 VSS
D 2 15 CAS
W 3 14 Q
RAS 4 13 A6
A0 5 12 A3
A2 6 11 A4
A1 7 10 A5
VDD 8 9 VCC
MCM4517
N/C 1 16 VSS
D 2 15 CAS
W 3 14 Q
RAS 4 13 A6
A0 5 12 A3
A2 6 11 A4
A1 7 10 A5
VCC 8 9 N/C
MCM6632A
REFRESH 1 16 VSS
D 2 15 CAS
W 3 14 Q
RAS 4 13 A6
A0 5 12 A3
A2 6 11 A4
A1 7 10 A5
VCC 8 9 A7
MCM6633A
N/C 1 16 VSS
D 2 15 CAS
W 3 14 Q
RAS 4 13 A6
A0 5 12 A3
A2 6 11 A4
A1 7 10 A5
VCC 8 9 A7
MCM6664A
REFRESH 1 16 VSS
D 2 15 CAS
W 3 14 Q
RAS 4 13 A6
A0 5 12 A3
A2 6 11 A4
A1 7 10 A5
VCC 8 9 A7
MCM6665A
N/C 1 16 VSS
D 2 15 CAS
W 3 14 Q
RAS 4 13 A6
A0 5 12 A3
A2 6 11 A4
A1 7 10 A5
VCC 8 9 A7

PIN VARIATIONS

PIN NUMBER	MCM4116	MCM4517	MCM6632A	MCM6663A	MCM6664A	MCM6665A
1	V_{BB}(−5 V)	N/C	REFRESH	N/C	REFRESH	N/C
8	V_{DD}(+12 V)	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
9	V_{CC}(+5 V)	N/C	A7	A7	A7	A7

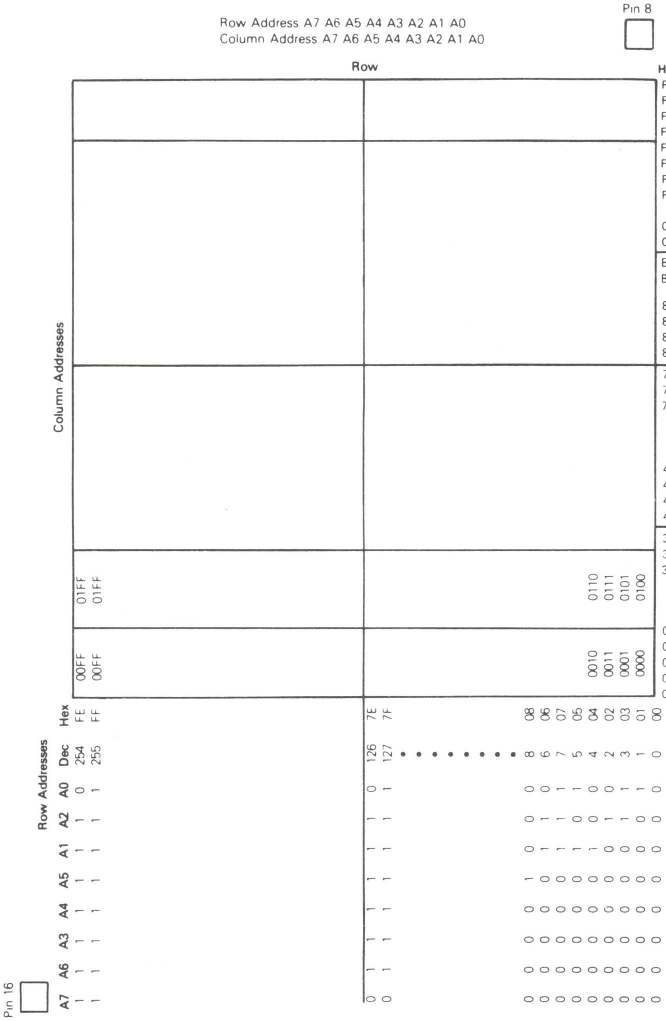
ORDERING INFORMATION

Part Number	Description	Speed	Marking*
MCM6633AL15	32K Dynamic	150	MCM66330A15/MCM66331AL15
MCM66330AL15	Random Access	150	MCM66330AL15
MCM66331AL15	Memory	150	MCM66331AL15
MCM6633AL20	Sidebraze	200	MCM66330AL20/MCM66331AL20
MCM66330AL20	Package "L"	200	MCM66330AL20
MCM66331AL20		200	MCM66331AL20

*MCM6633A = Tie A7 CAS (A15) Low "0"
MCM66331A = Tie A7 CAS (A15) High "1"

MCM6665A BIT ADDRESS MAP

Row Address A7 A6 A5 A4 A3 A2 A1 A0
Column Address A7 A6 A5 A4 A3 A2 A1 A0


Pin 8
Row
Column Addresses
01FF
01FF
0110
0111
0101
0100
00FF
00FF
0010
0011
0001
0000
Row Addresses
Hex FE FF 7E 7F 08 06 07 05 04 02 03 01 00
Dec 254 255 126 127 8 6 7 5 4 2 3 1 0
A0 0 1 0 1 0 0 1 1 0 0 1 1 0
A2 1 1 1 1 0 1 1 0 0 1 1 0 0
A1 1 1 1 1 0 1 1 1 1 0 0 0 0
A5 1 1 1 1 1 0 0 0 0 0 0 0 0
A4 1 1 1 1 0 0 0 0 0 0 0 0 0
A3 1 1 1 1 0 0 0 0 0 0 0 0 0
A6 1 1 1 1 0 0 0 0 0 0 0 0 0
A7 1 1 0 0 0 0 0 0 0 0 0 0 0
Pin 16

Column Addresses

Hex	Dec	A7	A6	A3	A4	A5	A2	A0	A1
FE	254	1	1	1	1	1	1	1	0
FF	255	1	1	1	1	1	1	1	1
FC	252	1	1	1	1	1	1	0	0
FD	253	1	1	1	1	1	1	0	1
FA	250	1	1	1	1	1	0	1	0
FB	251	1	1	1	1	1	0	1	1
F8	248	1	1	1	1	1	0	0	0
F9	249	1	1	1	1	1	0	0	1
	•								
C0	192	1	1	0	0	0	0	0	0
C1	193	1	1	0	0	0	0	0	1
BF	191	1	0	1	1	1	1	1	1
BE	190	1	0	1	1	1	1	1	0
	•								
83	131	1	0	0	0	0	0	1	1
82	130	1	0	0	0	0	0	1	0
81	129	1	0	0	0	0	0	0	1
80	128	1	0	0	0	0	0	0	0
7E	126	0	1	1	1	1	1	1	0
7F	127	0	1	1	1	1	1	1	1
7C	124	0	1	1	1	1	1	0	0
	•								
	•								
	•								
42	66	0	1	0	0	0	0	1	0
43	67	0	1	0	0	0	0	1	1
40	64	0	1	0	0	0	0	0	0
41	65	0	1	0	0	0	0	0	1
3F	63	0	0	1	1	1	1	1	1
3E	62	0	0	1	1	1	1	1	0
3D	61	0	0	1	1	1	1	0	1
	•								
	•								
	•								
04	4	0	0	0	0	0	1	0	0
03	3	0	0	0	0	0	0	1	1
02	2	0	0	0	0	0	0	1	0
01	1	0	0	0	0	0	0	0	1
00	0	0	0	0	0	0	0	0	0

Data Stored = $D_{in} \oplus A_{0X} \oplus A_{1Y}$

Column Address A1	Row Address A0	Data Stored
0	0	True
0	1	Inverted
1	0	Inverted
1	1	True

MOTOROLA

MCM6664A

Advance Information

MOS

(N-CHANNEL, SILICON-GATE)

65,536-BIT DYNAMIC RANDOM ACCESS MEMORY

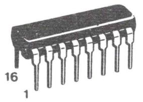
64K-BIT DYNAMIC RAM

The MCM6664A is a 65,536 bit, high-speed, dynamic Random-Access Memory. Organized as 65,536 one-bit words and fabricated using HMOS high-performance N-channel silicon-gate technology, this new breed of 5-volt only dynamic RAM combines high performance with low cost and improved reliability.

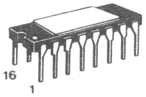
By multiplexing row- and column-address inputs, the MCM6664A requires only eight address lines and permits packaging in standard 16-pin dual-in-line packages. Complete address decoding is done on chip with address latches incorporated. Data out is controlled by $\overline{\text{CAS}}$ allowing for greater system flexibility.

All inputs and outputs, including clocks, are fully TTL compatible. The MCM6664A incorporates a one-transistor cell design and dynamic storage techniques. In addition to the $\overline{\text{RAS}}$-only refresh mode, the refresh control function available on pin 1 provides two additional modes of refresh, automatic and self refresh.

- Organized as 65,536 Words of 1 Bit
- Single 5 Volt Operation (±10%)
- Maximum Access Time: MCM6664A-12 = 120 ns
  MCM6664A-15 = 150 ns
  MCM6664A-20 = 200 ns
- Low Power Dissipation
  302.5 mW Maximum (Active) (MCM6664A-15)
  22 mW Maximum (Standby)
- Three-State Data Output
- Early-Write Common I/O Capability
- 16K Compatible 128-Cycle, 2 ms Refresh
- Control on Pin 1 for Automatic or Self Refresh
- $\overline{\text{RAS}}$-only Refresh Mode
- $\overline{\text{CAS}}$ Controlled Output
- Fast Page Mode Cycle Time
- Low Soft Error Rate <0.1% per 1000 Hours (See Soft Error Testing)

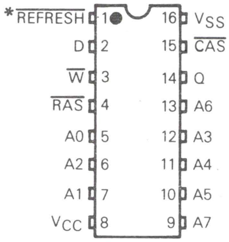


P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 690

PIN ASSIGNMENT

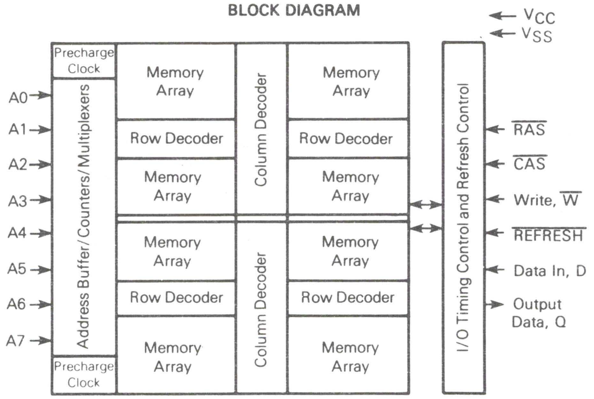

*REFRESH 1
D 2
W 3
RAS 4
A0 5
A2 6
A1 7
VCC 8
16 VSS
15 CAS
14 Q
13 A6
12 A3
11 A4
10 A5
9 A7

* If pin is not used, it should be connected to V_{CC} through a 10 k resistor.

PIN NAMES

$\overline{\text{REFRESH}}$	Refresh
A0-A7	Address Input
D	Data In
Q	Data Out
$\overline{\text{W}}$	Read/Write Input
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
V_{CC}	Power (+5 V)
V_{SS}	Ground

BLOCK DIAGRAM


VCC
VSS
Precharge Clock
A0
A1
A2
A3
A4
A5
A6
A7
Address Buffer/Counters/Multiplexers
Precharge Clock
Memory Array
Row Decoder
Memory Array
Memory Array
Row Decoder
Memory Array
Column Decoder
Column Decoder
Memory Array
Row Decoder
Memory Array
Memory Array
Row Decoder
Memory Array
I/O Timing Control and Refresh Control
RAS
CAS
Write, W
REFRESH
Data In, D
Output Data, Q

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

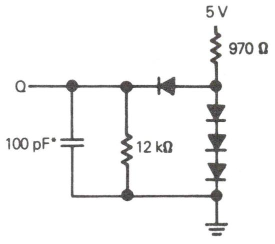
ADI-875R1/3-82

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS} (except V_{CC})	V_{in}, V_{out}	−2 to +7	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Power Dissipation	P_D	1.0	W
Data Out Current (Short Circuit)	I_{out}	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

FIGURE 1 — OUTPUT LOAD



*Includes Jig Capacitance

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	MCM6664A-12, -15, -20	V_{CC}	4.5	5.0	5.5	V	1
		V_{SS}	0	0	0	V	1
Logic 1 Voltage, All Inputs		V_{IH}	2.4	—	$V_{CC}+1$	V	1
Logic 0 Voltage, All Inputs		V_{IL}	−1.0	—	0.8	V	1, 19

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Units	Notes
V_{CC} Power Supply Current (Standby)	I_{CC2}	—	4.0	mA	5
V_{CC}Power Supply Current 6664A-12, $t_{RC}=250$ ns 6664A-15, $t_{RC}=270$ ns 6664A-20, $t_{RC}=330$ ns	I_{CC1}	 — — —	 60 55 45	mA	4
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles 6664A-12, $t_{RC}=250$ ns 6664A-15, $t_{RC}=270$ ns 6664A-20, $t_{RC}=330$ ns	I_{CC3}	 — — —	 50 45 35	mA	4
V_{CC} Power Supply Current During Page Mode Cycle for $t_{RAS}=10$ μsec 6664A-12, $t_{PC}=t_{RP}=120$ ns 6664A-15, $t_{PC}=t_{RP}=145$ ns 6664A-20, $t_{PC}=t_{RP}=200$ ns	I_{CC4}	 — — —	 45 40 35	mA	4
Input Leakage Current ($V_{SS} \leq V_{in} \leq V_{CC}$) (Any Input Except $\overline{REFRESH}$)	$I_{I(L)}$	—	10	μA	—
$\overline{REFRESH}$ Input Current ($V_{SS} \leq V_{in} \leq V_{CC}$)	I_F	—	20	μA	—
Output Leakage Current ($\overline{CAS}$ at logic 1, $V_{SS} \leq V_{out} \leq V_{CC}$)	$I_{O(L)}$	—	10	μA	—
Output Logic 1 Voltage @ $I_{out}=-4$ mA	V_{OH}	2.4	—	V	—
Output Logic 0 Voltage @ $I_{out}=4$ mA	V_{OL}	—	0.4	V	—

CAPACITANCE ($f=1.0$ MHz, $T_A=25°C$, $V_{CC}=5$ V Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit	Notes
Input Capacitance (A0-A7), D	C_{I1}	3	5	pF	7
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{REFRESH}$	C_{I2}	6	8	pF	7
Output Capacitance (Q), ($\overline{CAS}=V_{IH}$ to disable output)	C_O	5	7	pF	7

NOTES:

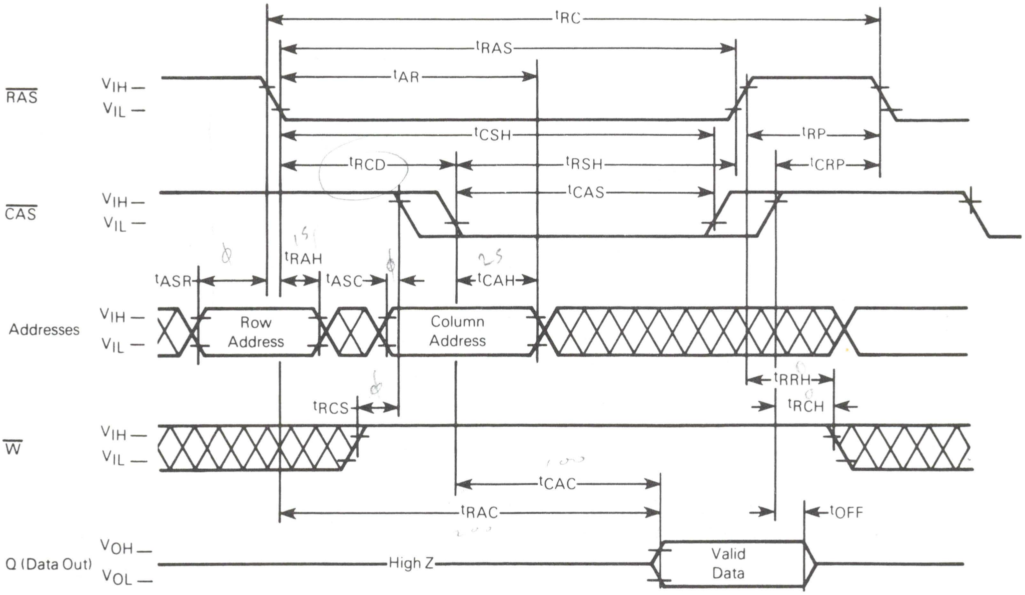
1. All voltages referenced to V_{SS}.
2. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
3. An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation guaranteed.
4. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
5. Output is disabled (open-circuit) and $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1.
6. The transition time specification applies for all inputs signals. In addition to meeting the transition rate specification, all input signals must transmit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
7. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C=I\Delta t/\Delta V$
8. The specifications for t_{RC} (min), and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
9. AC measurements $t_T=5.0$ ns.
10. Assumes that $t_{RCD} \leq t_{RCD}$ (Max).
11. Assumes that $t_{RCD} \geq t_{RCD}$ (Max)
12. Measured with a current load equivalent to 2 TTL (−200 μA, +4 mA) loads and 100 pF with the data output trip points set at $V_{OH}=2.0$ V and $V_{OL}=0.8$ V.
13. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

AC OPERATING CONDITIONS AND CHARACTERISTICS (Read, Write, and Read-Modify-Write Cycles)
(Full Operating Voltage and Temperature Range Unless Otherwise Noted . See Notes 2, 3, 6, and Figure 1)

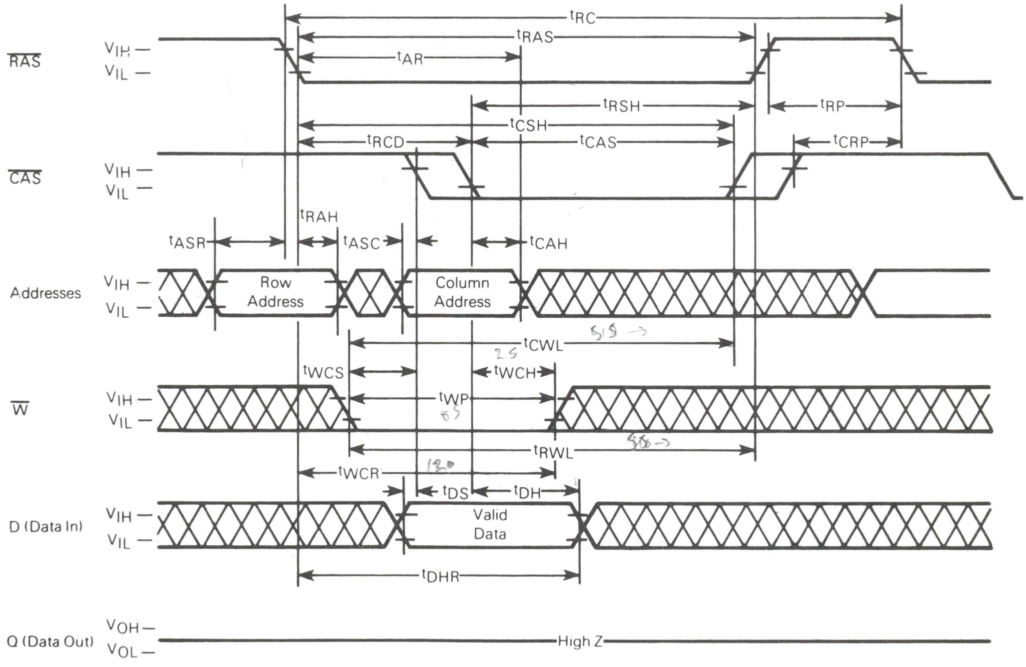
Parameter	Symbol	6664A-12		6664A-15		6664A-20		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	250	–	270	–	330	–	ns	8, 9
Read Write Cycle Time	t_{RWC}	255	–	280	–	345	–	ns	8, 9
Access Time from Row Address Strobe	t_{RAC}	–	120	–	150	–	200	ns	10, 12
Access Time from Column Address Strobe	t_{CAC}	–	60	–	75	–	100	ns	11, 12
Output Buffer and Turn-Off Delay	t_{OFF}	0	30	0	30	0	40	ns	18
Row Address Strobe Precharge Time	t_{RP}	100	–	100	–	120	–	ns	–
Row Address Strobe Pulse Width	t_{RAS}	120	10000	150	10000	200	10000	ns	–
Column Address Strobe Pulse Width	t_{CAS}	60	10000	75	10000	100	10000	ns	–
Row to Column Strobe Lead Time	t_{RCD}	20	60	25	75	30	100	ns	13
Row Address Setup Time	t_{ASR}	0	–	0	–	0	–	ns	–
Row Address Hold Time	t_{RAH}	15	–	20	–	25	–	ns	–
Column Address Setup Time	t_{ASC}	0	–	0	–	0	–	ns	–
Column Address Hold Time	t_{CAH}	25	–	35	–	45	–	ns	–
Column Address Hold Time Referenced to $\overline{\text{RAS}}$	t_{AR}	85	–	95	–	120	–	ns	17
Transition Time (Rise and Fall)	t_{T}	3	50	3	50	3	50	ns	6
Read Command Setup Time	t_{RCS}	0	–	0	–	0	–	ns	–
Read Command Hold Time	t_{RCH}	0	–	0	–	0	–	ns	14
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{RRH}	0	–	0	–	0	–	ns	14
Write Command Hold Time	t_{WCH}	25	–	35	–	45	–	ns	–
Write Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{WCR}	85	–	95	–	120	–	ns	17
Write Command Pulse Width	t_{WP}	25	–	35	–	45	–	ns	–
Write Command to Row Strobe Lead Time	t_{RWL}	40	–	45	–	55	–	ns	–
Write Command to Column Strobe Lead Time	t_{CWL}	40	–	45	–	55	–	ns	–
Data in Setup Time	t_{DS}	0	–	0	–	0	–	ns	15
Data in Hold Time	t_{DH}	25	–	35	–	45	–	ns	15
Data in Hold Time Referenced to $\overline{\text{RAS}}$	t_{DHR}	85	–	95	–	120	–	ns	17
Column to Row Strobe Precharge Time	t_{CRP}	−10	–	−10	–	−10	–	ns	–
$\overline{\text{RAS}}$ Hold Time	t_{RSH}	60	–	75	–	100	–	ns	–
Refresh Period	t_{RFSH}	–	2.0	–	2.0	–	2.0	ms	–
$\overline{\text{WRITE}}$ Command Setup Time	t_{WCS}	−10	–	−10	–	−10	–	ns	16
$\overline{\text{CAS}}$ to $\overline{\text{WRITE}}$ Delay	t_{CWD}	40	–	45	–	55	–	ns	16
$\overline{\text{RAS}}$ to $\overline{\text{WRITE}}$ Delay	t_{RWD}	100	–	120	–	155	–	ns	16
$\overline{\text{CAS}}$ Hold Time	t_{CSH}	120	–	150	–	200	–	ns	–
$\overline{\text{CAS}}$ Precharge Time (Page Mode Cycle Only)	t_{CP}	50	–	60	–	80	–	ns	–
Page Mode Cycle Time	t_{PC}	120	–	145	–	200	–	ns	–
$\overline{\text{RAS}}$ to $\overline{\text{REFRESH}}$ Delay	t_{RFD}	−10	–	−10	–	−10	–	ns	–
$\overline{\text{REFRESH}}$ Period (Battery Backup Mode)	t_{FBP}	2000	–	2000	–	2000	–	ns	–
$\overline{\text{REFRESH}}$ to $\overline{\text{RAS}}$ Precharge Time (Battery Backup Mode)	t_{FBR}	290	–	320	–	400	–	ns	–
$\overline{\text{REFRESH}}$ Cycle Time (Auto Pulse Mode)	t_{FC}	250	–	270	–	330	–	ns	–
$\overline{\text{REFRESH}}$ Pulse Period (Auto Period Mode)	t_{FP}	60	2000	60	2000	60	2000	ns	–
$\overline{\text{REFRESH}}$ to $\overline{\text{RAS}}$ Setup Time (Auto Pulse Mode)	t_{FSR}	−30	–	−30	–	−30	–	ns	–
$\overline{\text{REFRESH}}$ to $\overline{\text{RAS}}$ Delay Time (Auto Pulse Mode)	t_{FRD}	290	–	320	–	400	–	ns	–
$\overline{\text{REFRESH}}$ Inactive Time	t_{FI}	60	–	60	–	60	–	ns	–
$\overline{\text{RAS}}$ to $\overline{\text{REFRESH}}$ Lead Time	t_{FRL}	350	–	370	–	450	–	ns	–
$\overline{\text{RAS}}$ Inactive Time During $\overline{\text{REFRESH}}$	t_{FRI}	350	–	370	–	450	–	ns	–

14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in random write cycles and to $\overline{\text{WRITE}}$ leading edge in delayed write or read-modify-write cycles.
16. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
17. Addresses, data-in and WRITE are don't care. Data-out depends on the state of CAS. If CAS remains low, the previous output will remain valid. CAS is allowed to make an active to inactive transition during the pin #1 refresh cycle. When CAS is brought high, the output will assume a high-impedance state.
18. t_{off} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
19. The device will withstand undershoots to the −2 volt level with a maximum pulse width of 20 ns at the −1.5 volt level. This is periodically sampled rather than 100% tested.

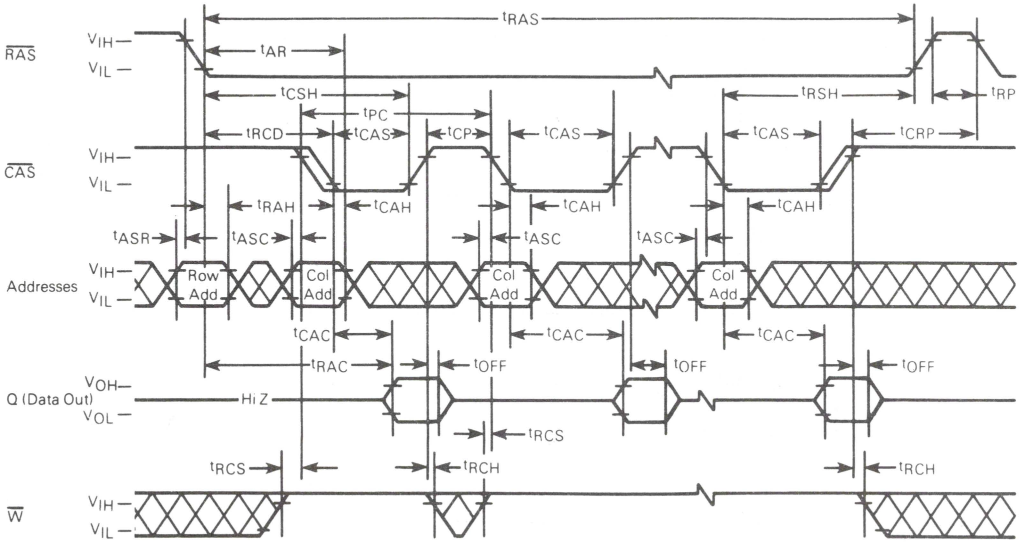
READ CYCLE TIMING


tRC
tRAS
tAR
RAS
VIH
VIL
tCSH
tRP
tRCD
tRSH
tCRP
tCAS
CAS
VIH
VIL
0
15
tRAH
0
25
tASR
tASC
tCAH
Addresses
VIH
VIL
Row Address
Column Address
0
tRRH
0
tRCH
0
tRCS
W
VIH
VIL
100
tCAC
tRAC
tOFF
Q (Data Out)
VOH
VOL
High Z
Valid Data

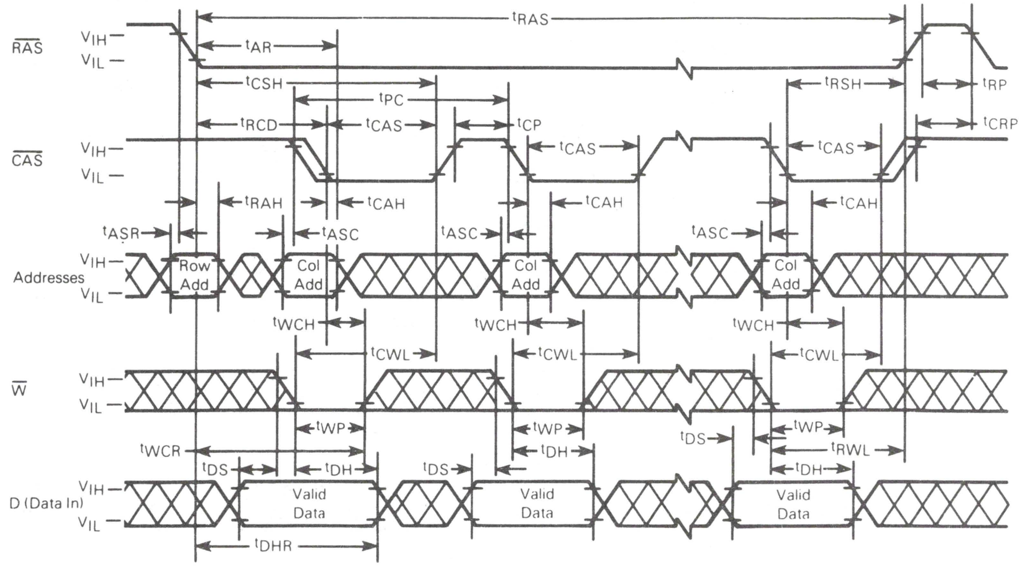
WRITE CYCLE TIMING


tRC
tRAS
tAR
RAS
VIH
VIL
tRSH
tRP
tCSH
tRCD
tCAS
tCRP
CAS
VIH
VIL
tRAH
tASR
tASC
tCAH
Addresses
VIH
VIL
Row Address
Column Address
tCWL
515 →
25
tWCS
tWCH
W
VIH
VIL
tWP
85
tRWL
515 →
tWCR
120
tDS
tDH
D (Data In)
VIH
VIL
Valid Data
tDHR
Q (Data Out)
VOH
VOL
High Z

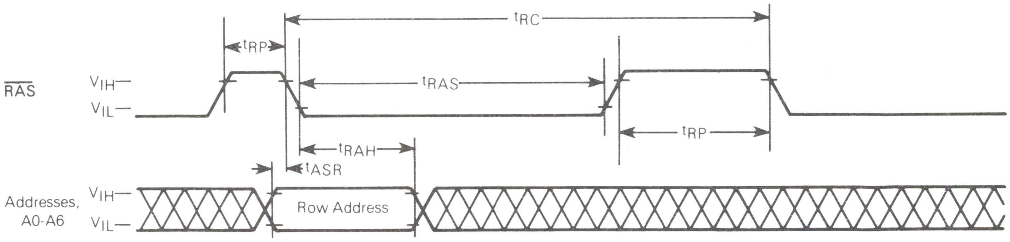
PAGE MODE READ CYCLE


tRAS
RAS
VIH—
VIL—
tAR
tRP
tCSH
tRSH
tPC
tRCD
tCAS
tCP
tCAS
tCAS
tCRP
CAS
VIH—
VIL—
tRAH
tCAH
tCAH
tCAH
tASR
tASC
tASC
tASC
Addresses
VIH—
VIL—
Row Add
Col Add
Col Add
Col Add
tCAC
tCAC
tCAC
tRAC
tOFF
tOFF
tOFF
Q (Data Out)
VOH—
VOL—
Hi Z
tRCS
tRCS
tRCH
tRCH
W
VIH—
VIL—

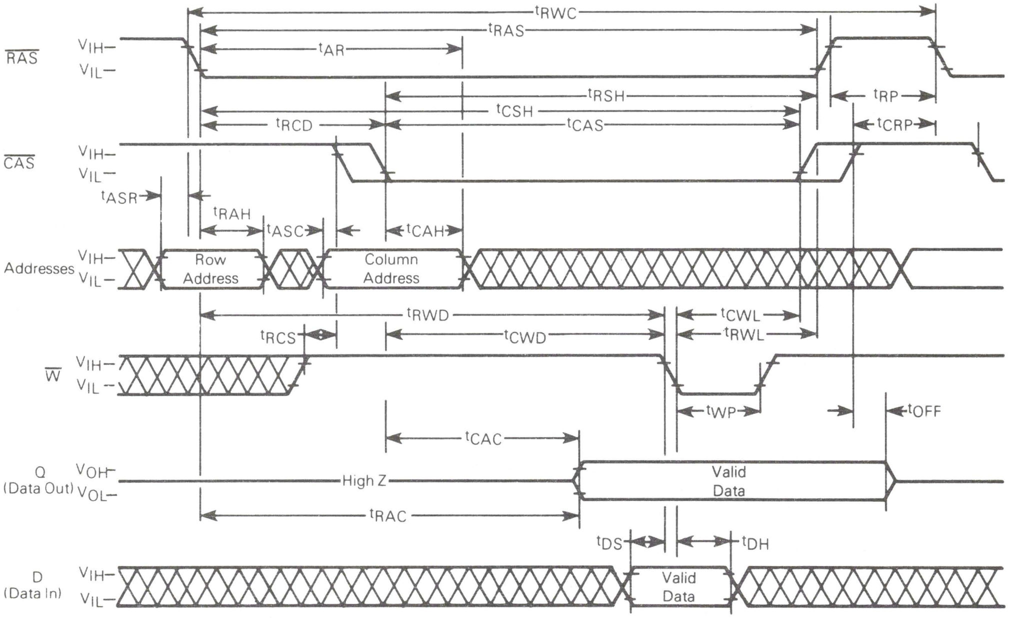
PAGE MODE WRITE CYCLE


tRAS
RAS
VIH—
VIL—
tAR
tRP
tCSH
tRSH
tPC
tRCD
tCAS
tCP
tCRP
CAS
VIH—
VIL—
tCAS
tCAS
tRAH
tCAH
tCAH
tCAH
tASR
tASC
tASC
tASC
Addresses
VIH—
VIL—
Row Add
Col Add
Col Add
Col Add
tWCH
tWCH
tWCH
tCWL
tCWL
tCWL
W
VIH—
VIL—
tWP
tWP
tWP
tWCR
tDS
tDH
tDS
tDH
tDS
tDH
tRWL
D (Data In)
VIH—
VIL—
Valid Data
Valid Data
Valid Data
tDHR

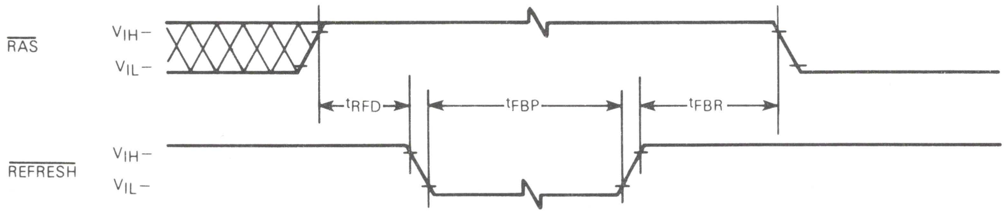
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE
(Data-in and $\overline{\text{WRITE}}$ are Don't Care, $\overline{\text{CAS}}$ is HIGH)


tRC
tRP
RAS
VIH
VIL
tRAS
tRP
tRAH
tASR
Addresses, A0-A6
VIH
VIL
Row Address

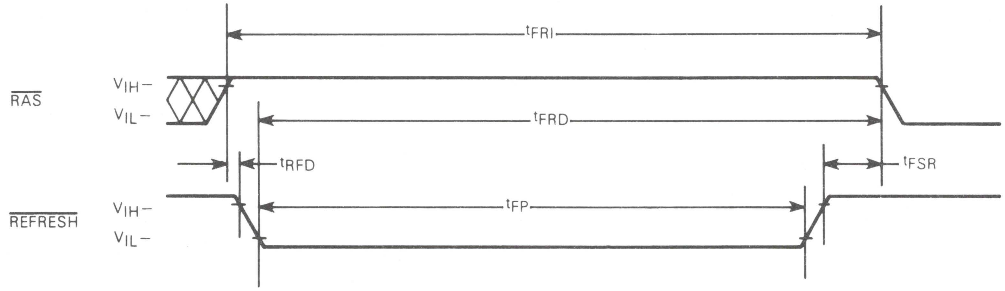
READ-WRITE/READ-MODIFY-WRITE CYCLE


tRWC
tRAS
tAR
RAS
VIH
VIL
tRSH
tRP
tCSH
tRCD
tCAS
tCRP
CAS
VIH
VIL
tASR
tRAH
tASC
tCAH
Addresses
VIH
VIL
Row Address
Column Address
tRWD
tCWL
tRCS
tCWD
tRWL
W
VIH
VIL
tWP
tOFF
tCAC
Q (Data Out)
VOH
VOL
High Z
Valid Data
tRAC
tDS
tDH
D (Data In)
VIH
VIL
Valid Data

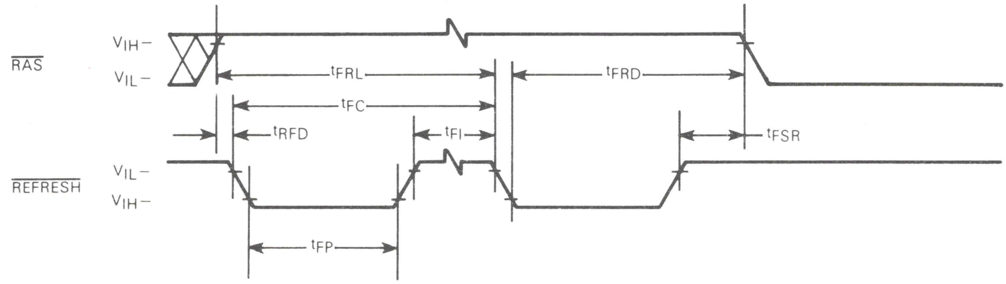
SELF REFRESH MODE (Battery Backup)*


$\overline{RAS}$
V_{IH} –
V_{IL} –
t_{RFD}
t_{FBP}
t_{FBR}
$\overline{REFRESH}$
V_{IH} –
V_{IL} –

AUTOMATIC PULSE REFRESH CYCLE — SINGLE PULSE*


t_{FRI}
$\overline{RAS}$
V_{IH} –
V_{IL} –
t_{FRD}
t_{RFD}
t_{FSR}
$\overline{REFRESH}$
V_{IH} –
V_{IL} –
t_{FP}

AUTOMATIC PULSE REFRESH CYCLE — MULTIPLE PULSE*


$\overline{RAS}$
V_{IH} –
V_{IL} –
t_{FRL}
t_{FRD}
t_{FC}
t_{RFD}
t_{FI}
t_{FSR}
$\overline{REFRESH}$
V_{IL} –
V_{IH} –
t_{FP}

*Addresses, data-in and $\overline{WRITE}$ are don't care, $\overline{CAS}$ is high.

TYPICAL CHARACTERISTICS

FIGURE 2 — $\overline{\text{RAS}}$ ACCESS TIME versus SUPPLY VOLTAGE

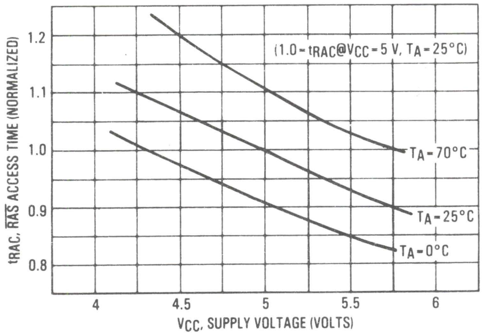


FIGURE 3 — $\overline{\text{CAS}}$ ACCESS TIME versus SUPPLY VOLTAGE

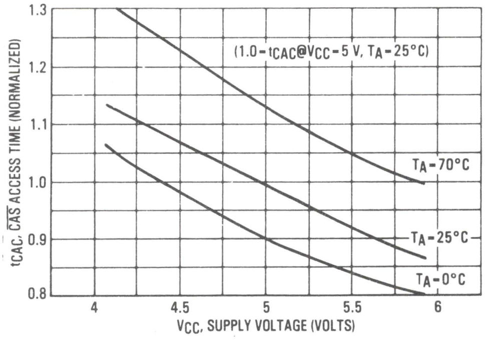


FIGURE 4 — $\overline{\text{RAS}}$ ACCESS TIME versus AMBIENT TEMPERATURE

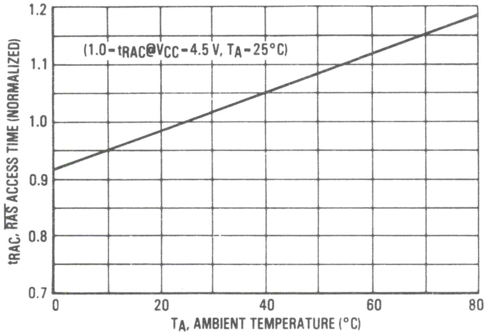


FIGURE 5 — $\overline{\text{CAS}}$ ACCESS TIME versus AMBIENT TEMPERATURE

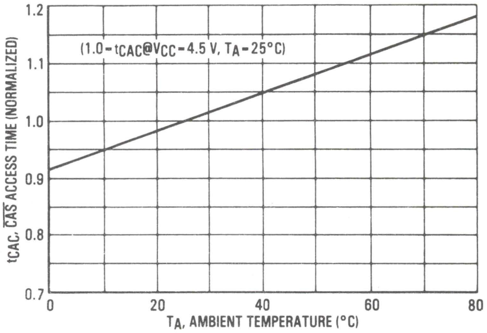


FIGURE 6 — $\overline{\text{RAS}}$, $\overline{\text{W}}$ INPUT LEVEL versus SUPPLY VOLTAGE

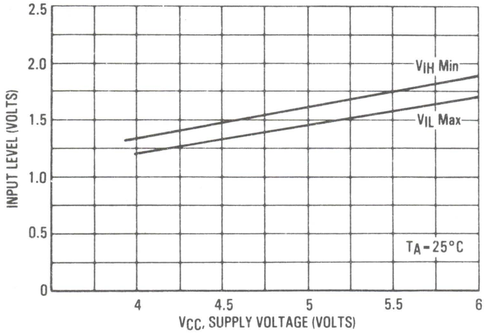
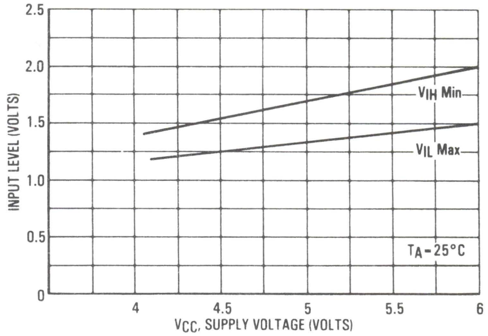


FIGURE 7 — $\overline{\text{CAS}}$, $\overline{\text{W}}$ INPUT LEVEL versus SUPPLY VOLTAGE



TYPICAL CHARACTERISTICS (continued)

FIGURE 8 — I_{CC1} SUPPLY CURRENT versus CYCLE RATE

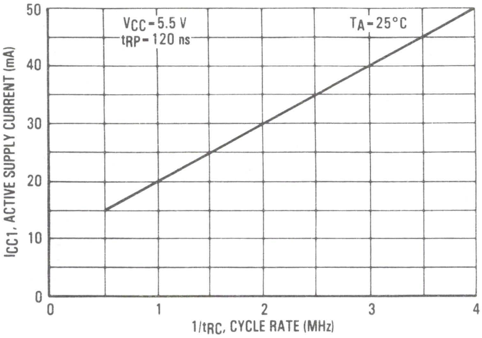


FIGURE 9 — I_{CC1} SUPPLY CURRENT versus SUPPLY VOLTAGE

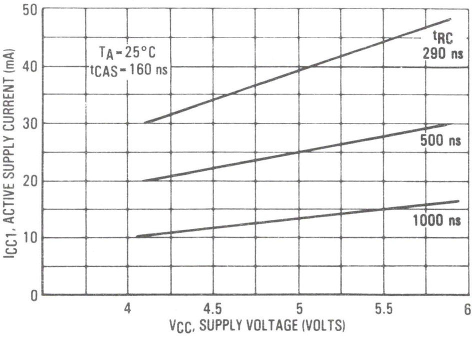


FIGURE 10 — I_{CC1} SUPPLY CURRENT versus SUPPLY VOLTAGE

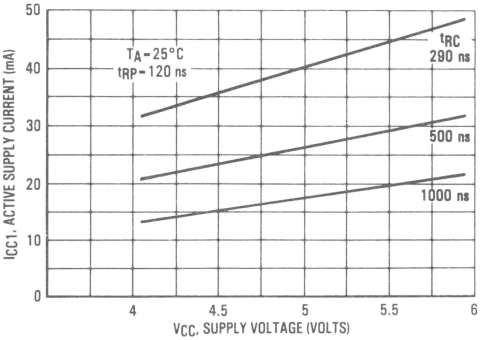


FIGURE 11 — I_{CC1} SUPPLY CURRENT versus AMBIENT TEMPERATURE (min t_{RP})

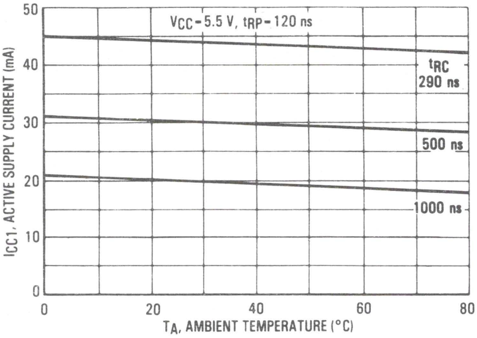


FIGURE 12 — I_{CC1} SUPPLY CURRENT versus AMBIENT TEMPERATURE (min $\overline{RAS}$)

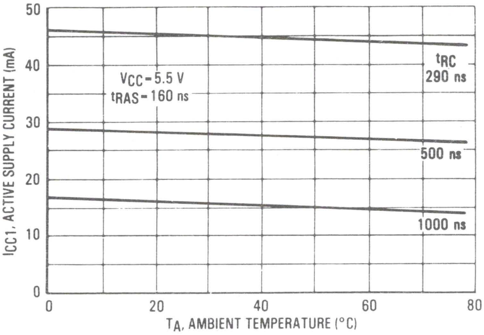
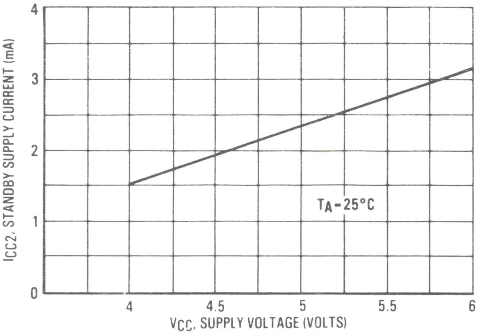


FIGURE 13 — I_{CC2} SUPPLY CURRENT versus SUPPLY VOLTAGE



TYPICAL CHARACTERISTICS (continued)

FIGURE 14 — I_{CC2} STANDBY CURRENT versus AMBIENT TEMPERATURE

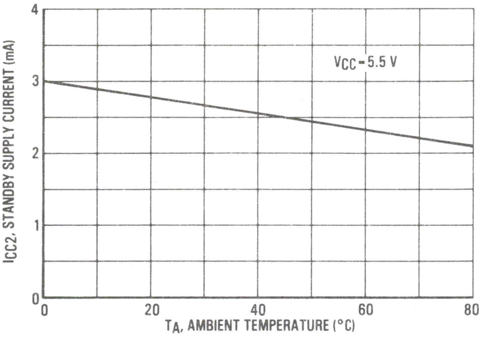


FIGURE 15 — I_{CC3} SUPPLY CURRENT versus CYCLE RATE

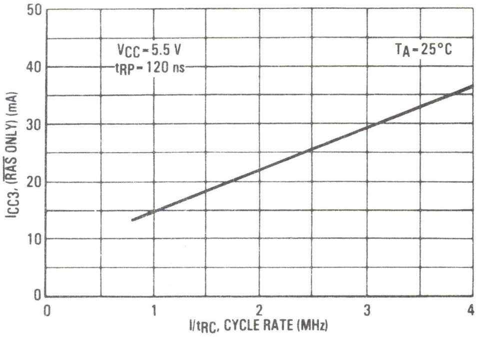


FIGURE 16 — ADDRESS INPUT LEVEL versus SUPPLY VOLTAGE

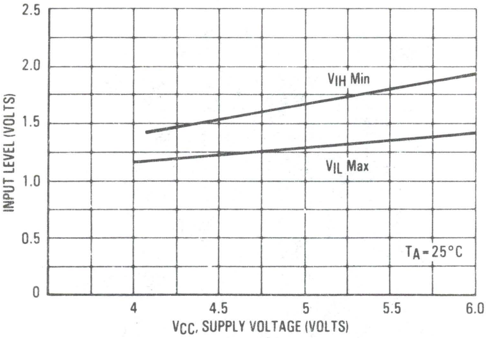
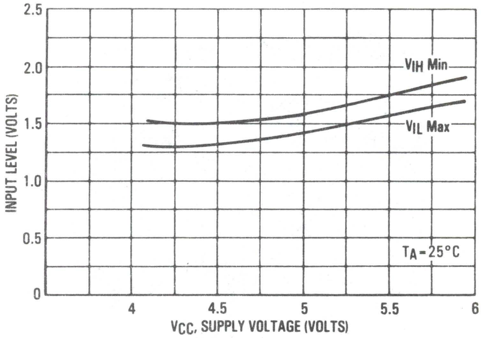


FIGURE 17 — DATA INPUT LEVEL versus SUPPLY VOLTAGE



SOFT ERROR TESTING

The storage cell depletion regions as well as the sense amplifier and its associated bit lines are susceptible to charge collection of electrons from an alpha "hit." However, the susceptibility of these vulnerable regions varies. Depleted storage cells are vulnerable at all times, whereas the sense amplifiers and associated bit lines are susceptible only during the small portion of the memory cycle just prior to sensing. Hence, an increase in the frequency of dynamic RAM access will cause a corresponding increase in the soft error rate.

To take this memory access dependency into account, the total soft error rate profile includes a cycle time component. The soft error rate due to bit line hits at the system's memory cycle rate is added to the soft error rate due to storage cell hits which are not frequency dependent. Figure 18 illustrates the impact that frequency of access has on the MCM6664A/MCM6665A overall soft error rate.

Under normal operating conditions, the die will be exposed to radiation levels of less than 0.01 alpha/cm^2/hr. Accelerated soft error testing data is generated from at least three high-intensity sources having an Alpha Flux Density range of 1×10^5 to 6×10^5 (alpha/cm^{2}hr) placed over uncoated die. Figure 19 shows the soft error rate for a given alpha flux density at a cycle rate of 100 kHz. The accelerated data of Figures 18 and 19 project that the soft error rate for package level radiation will be less than 0.1%/1000 hours.

SYSTEM LIFE OPERATING TEST CONDITIONS

1) Cycle time: 1 microsecond for read, write and refresh cycles
2) Refresh Rate: 1 millisecond
3) Voltage: 5.0 V
4) Temperature: 30° C ±2° C (ambient temperature inside enclosure)
5) Elevation: Approximately 620 feet above mean sea level
6) Data Patterns: Write the entire memory space sequentially with all "1"s and then perform continuous sequential reads for 6 hours. Next, write the entire memory space with all "0"s sequentially and then perform continuous sequential reads for 6 hours. Next, go back to the all "1"s pattern and repeat the sequences all over again.

FIGURE 18 — ACCELERATED SOFT ERROR versus CYCLE TIME

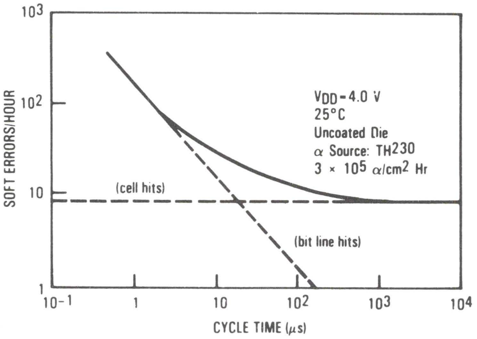
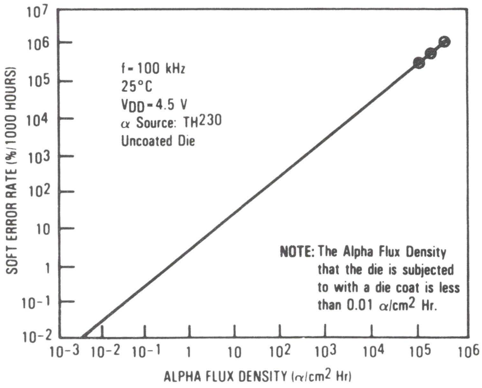
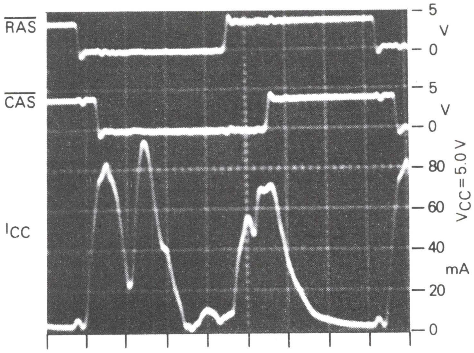


FIGURE 19 — SOFT ERROR RATE versus ALPHA FLUX DENSITY



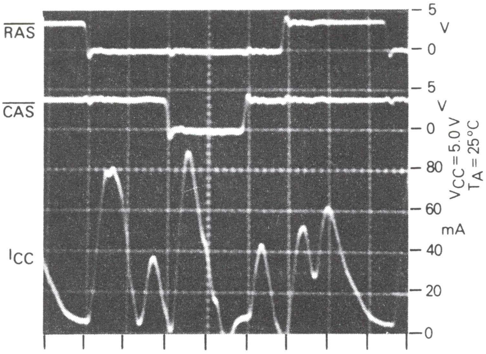
CURRENT WAVEFORMS

FIGURE 20 — $\overline{RAS}/\overline{CAS}$ CYCLE



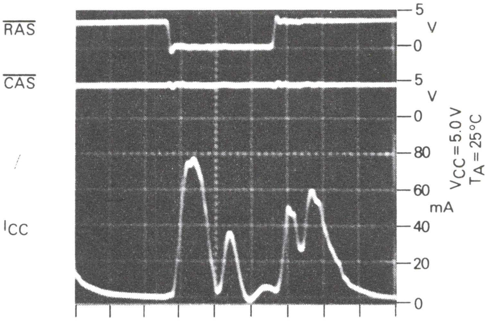
50 ns/Div Time (ns)

FIGURE 21 — LONG $\overline{RAS}/\overline{CAS}$ CYCLE



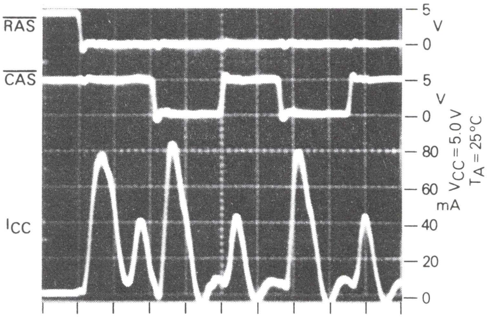
50 ns/Div Time (ns)

FIGURE 22 — $\overline{RAS}$ ONLY CYCLE



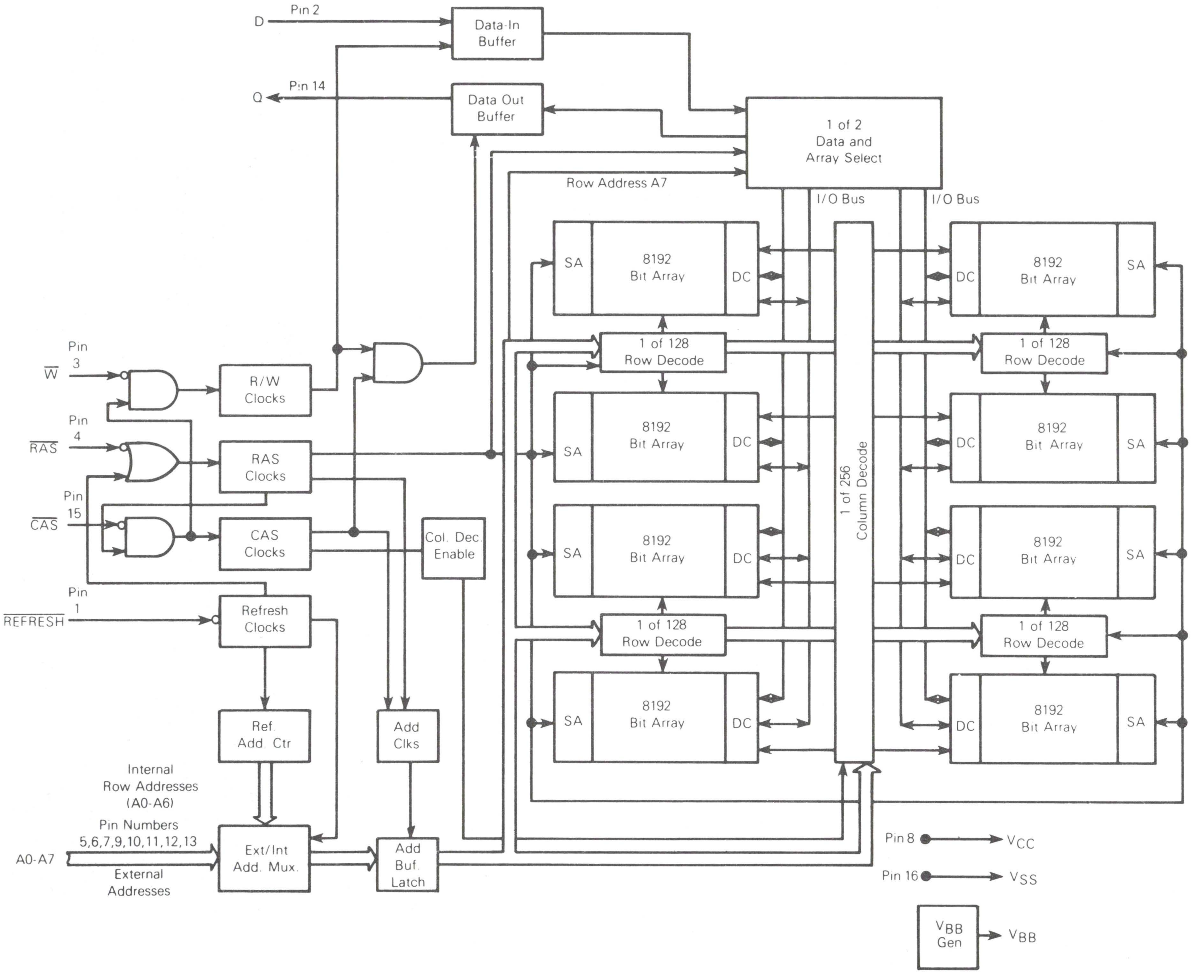
50 ns/Div Time (ns)

FIGURE 23 — PAGE MODE CYCLE



50 ns/Div Time (ns)

FIGURE 24 — FUNCTIONAL BLOCK DIAGRAM


D
Pin 2
Data-In Buffer
Q
Pin 14
Data Out Buffer
1 of 2 Data and Array Select
Row Address A7
I/O Bus
I/O Bus
SA
8192 Bit Array
DC
1 of 128 Row Decode
1 of 256 Column Decode
Pin 3
W̄
Pin 4
R̄ĀS̄
Pin 15
C̄ĀS̄
Pin 1
R̄ĒF̄R̄ĒS̄H̄
R/W Clocks
RAS Clocks
CAS Clocks
Refresh Clocks
Col. Dec. Enable
Ref. Add. Ctr
Add Clks
Internal Row Addresses (A0-A6)
Pin Numbers 5,6,7,9,10,11,12,13
A0-A7
External Addresses
Ext/Int Add. Mux.
Add Buf. Latch
Pin 8
VCC
Pin 16
VSS
VBB Gen
VBB

DEVICE INITIALIZATION

Since the 64K dynamic RAM is a single supply 5 V only device, the need for power supply sequencing is no longer required as was the case in older generation dynamic RAMs. On power-up an initial pause of 100 microseconds is required for the internal substrate generator pump to establish the correct bias voltage. This is to be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize the various dynamic nodes internal to the device. During an extended inactive state of the device (greater than 2 ms with device powered up) the wake up sequence (8 active cycles) will be necessary to assure proper device operation. See Figures 25 and 26 for power on characteristics of the RAM for two conditions (clocks active, clocks inactive).

The row address strobe is the primary "clock" that activates the device and maintains the data when the RAM is in the standby mode. This is the main feature that distinquishes it as a dynamic RAM as opposed to a static RAM. A dynamic RAM is placed in a low power standby mode when the device receives a positive-going row address strobe. The variation in the power dissipation of a dynamic RAM from the active to the standby state is an order of magnitude or more for NMOS devices. This feature is used to its fullest advantage with high density mainframe memory systems, where only a very small percentage of the devices are in the active mode at any one time and the rest of the devices are in the standby mode. Thus, large memory systems can be assembled that dissipate very low power per bit compared to a system where all devices are active continuously.

ADDRESSING THE RAM

The eight address pins on the device are time multiplexed with two separate 8-bit address fields that are strobed at the beginning of the memory cycle by two clocks (active negative) called the row address strobe and the column address strobe. A total of sixteen address bits will decode one of the 65,536 cell locations in the device. The column address strobe follows the row address strobe by a specified minimum and maximum time called "t_{RCD}," which is the row to column strobe delay. This time interval is also referred to as the multiplex window which gives flexibility to a system designer to set up his external addresses into the RAM. These conditions have to be met for normal read or write cycles. This initial portion of the cycle accomplishes the normal addressing of the device. There are, however, two other variations in addressing the 64K RAM, one is called the page mode cycle (described later) where an 8-bit column address field is presented on the input pins and latched by the $\overline{CAS}$ clock; and the other is the $\overline{RAS}$ only refresh cycle (described later) where a 7-bit row address field is presented on the input pins and latched by the $\overline{RAS}$ clock. In the latter case, the most significant bit on Row Address A7 (pin 9) is not required for refresh. See bit address map for the topology of the cells and their address selection.

NORMAL READ CYCLE

A read cycle is referred to as normal read cycle to differentiate if from a page-mode-read cycle, a read-while-write cycle, and read-modify-write cycle which are covered in a later section.

The memory read cycle begins with the row addresses valid and the $\overline{RAS}$ clock transitioning from V_{IH} to the V_{IL} level. The $\overline{CAS}$ clock must also make a transition from V_{IH} to the V_{IL} level at the specified t_{RCD} timing limits when the column addresses are latched. Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. Also, these clocks are linked in such a manner that the access time of the device is independent of the address multiplex window. The only stipulation is that the $\overline{CAS}$ clock must be active before or at

CURRENT WAVEFORMS

FIGURE 25 — SUPPLY CURRENT versus SUPPLY VOLTAGE DURING POWER UP, $\overline{RAS}$, $\overline{CAS}$ = V_{CC}

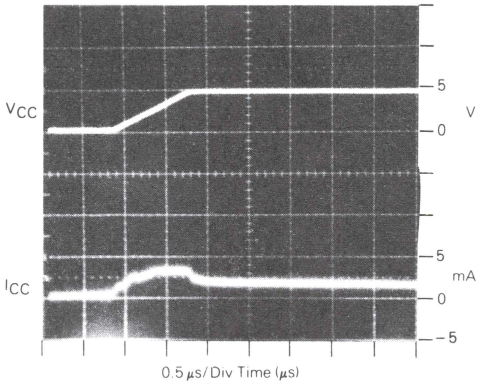
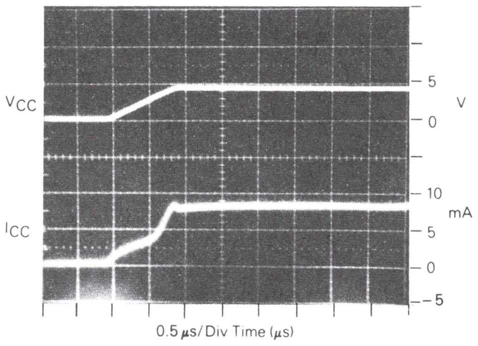


FIGURE 26 — SUPPLY CURRENT versus SUPPLY VOLTAGE DURING POWER UP, $\overline{RAS}$, $\overline{CAS}$ = V_{SS}



the t_{RCD} maximum specification for an access (data valid) from the $\overline{RAS}$ clock edge to be guaranteed (t_{RAC}). If the t_{RCD} maximum condition is not met, the access (t_{CAC}) from the $\overline{CAS}$ clock active transition will determine read access time. The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available, as noted in the functional block diagram, Figure 24. This gating feature on the $\overline{CAS}$ clock will allow the external $\overline{CAS}$ signal to become active as soon as the row address hold time (t_{RAH}) specification has been met and defines the t_{RCD} minimum specification. The time difference between t_{RCD} minimum and t_{RCD} maximum can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

Once the clocks have become active, they must stay active for the minimum (t_{RAS}) period for the $\overline{RAS}$ clock and the minimum (t_{CAS}) period for the $\overline{CAS}$ clock. The $\overline{RAS}$ clock must stay inactive for the minimum (t_{RP}) time. The former is for the completion of the cycle in progress, and the latter is for the device internal circuitry to be precharged for the next active cycle.

Data out is not latched and is valid as long as the $\overline{CAS}$ clock is active; the output will switch to the three-state mode when the $\overline{CAS}$ clock goes inactive. The $\overline{CAS}$ clock can remain active for a maximum of 10 ns (t_{CRP}) into the next cycle. To perform a read cycle, the write ($\overline{W}$) input must be held at the V_{IH} level from the time the $\overline{CAS}$ clock makes its active transition (t_{RCS}) to the time when it transitions into the inactive (t_{RCH}) mode.

WRITE CYCLE

A write cycle is similar to a read cycle except that the Write ($\overline{W}$) clock must go active (V_{IL} level) at or before the $\overline{CAS}$ clock goes active at a minimum t_{WCS} time. If the above condition is met, then the cycle in progress is referred to as a early write cycle. In an early write cycle, the write clock and the data in is referenced to the active transition of the $\overline{CAS}$ clock edge. There are two important parameters with respect to the write cycle: the column strobe to write lead time (t_{CWL}) and the row strobe to write lead time (t_{RWL}). These define the minimum time that $\overline{RAS}$ and $\overline{CAS}$ clocks need to be active after the write operation has started (($\overline{W}$) clock at V_{IL} level).

It is also possible to perform a late write cycle. For this cycle the write clock is activated after the $\overline{CAS}$ goes low which is beyond t_{WCS} minimum time. Thus the parameters t_{CWL} and t_{RWL} must be satisfied before terminating this cycle. The difference between an early write cycle and a late write cycle is that in a late write cycle the write (W) clock can occur much later in time with respect to the active transition of the $\overline{CAS}$ clock. This time could be as long as 10 microseconds − [t_{RWL} + t_{RP} + $2T_t$].

At the start of a write cycle, the data out is in a three-state condition and remains inactive throughout the cycle. The data out remains three-state because of the active transition of the write ($\overline{W}$) clock prevents the $\overline{CAS}$ clock from enabling the data-out buffers as noted in Functional Block Diagram. The three-state condition (high impedence) of the Data Out Pin during a write cycle can be effectively utilized in systems that have a common input/output bus. The only stipulation is that the system use only early write mode operations for all write cycles to avoid bus contention.

READ-MODIFY-WRITE AND READ-WHILE-WRITE CYLES

As the name implies, both a read and a write cycle is accomplished at a selected bit during a single access. The read-modify-write cycle is similar to the late write cycle discussed above.

For the read-modify-write cycle a normal read cycle is initiated with the write ($\overline{W}$) clock at the V_{IH} level until the read data occurs at the device access time (t_{RAC}). At this time the write ($\overline{W}$) clock is asserted. The data in is setup and held with respect to the active edge of the write clock. The cycle described assumes a zero modify time between read and write.

Another variation of the read-modify-write cycle is the read-while-write cycle. For this cycle, the following parameters (t_{RWD}, t_{CWD}) play an important role. A read-while-write cycle starts as a normal read cycle with the write ($\overline{W}$) clock being asserted at minimum t_{RWD} or minimum t_{CWD} time, depending upon the application. This results in starting a write operation to the selected cell even before data out occurs. The minimum specification on t_{RWD} and t_{CWD} assure that data out does occur. In this case, the data in is set up with respect to write ($\overline{W}$) clock active edge.

PAGE-MODE CYCLES

Page mode operation allows faster successive data operations at the 256 column locations. Page access (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access (t_{RAC}) on the Motorola 64K dynamic RAM. Page mode operation consists of holding the $\overline{RAS}$ clock active while cycling the $\overline{CAS}$ clock to access the column locations determined by the 8-bit column address field. There are two controlling factors that limit the access to all 256 column locations in one $\overline{RAS}$ clock active operation. These are the refresh interval of the device (2 ms/128 = 15.6 microseconds) and the maximum active time specification for the $\overline{RAS}$ clock (10 microseconds). Since 10 microseconds is the smaller value, the maximum specification of the $\overline{RAS}$ clock on time is the limiting factor of the number of sequential page accesses possible. Ten microseconds will provide approximately 50 successive page accesses (10 microseconds ÷ page mode cycle time) for each row address selected before the $\overline{RAS}$ clock is reset.

The page cycle is always initiated with a row address being provided and latched by the $\overline{RAS}$ clock, followed by the column address and $\overline{CAS}$ clock. From the timing illustrated, the initial cycle is a normal read or write cycle, that has been previously described, followed by the shorter $\overline{CAS}$ cycles (t_{PC}). The $\overline{CAS}$ cycle time (t_{PC}) consists of the $\overline{CAS}$ clock active time (t_{CAS}), and $\overline{CAS}$ clock precharge time (t_{CP}) and two transitions. In addition to read and write cycles, a read-modify-write cycle can also be performed in a page mode operation. For a read-modify-write or read-while-write type cycle, the conditions normal to that mode of operation will apply in the page mode also. The page mode cycle illustrated show a series of sequential reads separated by a series of sequential writes. This is just one mode of operation. In practice, any combination of read, write and read-modify-write cycles can be performed to suit a particular application.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to

degrade with time and temperature. Therefore, to retain the correct information, the bits need to be refreshed at least once every 2 ms. This is accomplished by sequentially cycling through the 128 row address locations every 2 ms, or at least one row every 15.6 microseconds. A normal read or write operation to the RAM will serve to refresh all the bits (256) associated with that particular row decoded.

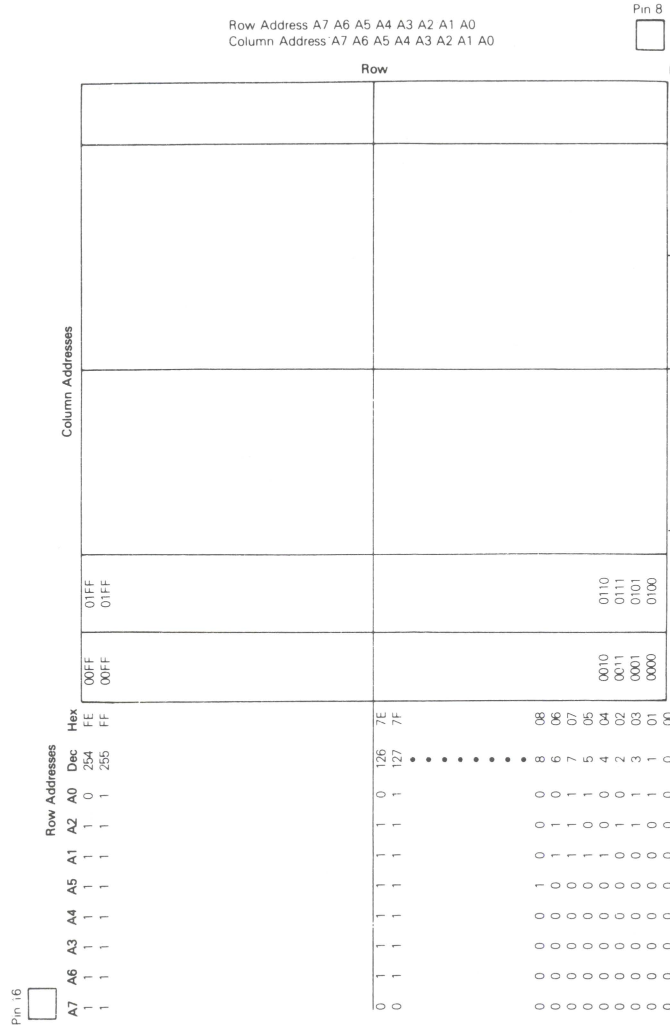
$\overline{\text{RAS}}$ Only Refresh — When the memory component is in standby the $\overline{\text{RAS}}$ only refresh scheme is employed. This refresh method performs a $\overline{\text{RAS}}$ only cycle on all 128 row addresses every 2 ms. The row addresses are latched in with the $\overline{\text{RAS}}$ clock, and the associated internal row locations are refreshed. As the heading implies, the $\overline{\text{CAS}}$ clock is not required and should be inactive or at a V_{IH} level to conserve power.

Auto Refresh Mode and Self Refresh mode (MCM6664A only) — With the MCM6664A, two additional refresh methods are available to the user. These special functions are incorporated on pin 1 of the device and have been approved by JEDEC as an alternative function for that pin on the 64K dynamic memory. The auto refresh mode is accomplished by asserting pin 1 active (V_{IL} level) during the time interval when there are no memory cycles. In the auto refresh mode, the $\overline{\text{REFRESH}}$ active pulse (t_{FP}) must be limited to 2 microseconds or less. The 2 microsecond time is specified to prevent the device from transitioning into the self refresh mode. Auto refresh can be performed in a distributed mode (refresh cycle every 15.6 microseconds) and in a burst mode where all 128 refresh cycles are done one after the other until complete. An onboard address counter generates the internal row address to refresh a particular row and increments itself at the end of each cycle.

Another variation of refresh is the self refresh mode. This mode is similar to the auto refresh method except that the active pulse width (t_{FBP}) must be greater than 2 microseconds or held down active indefinitely. With pin 1 in the self refresh mode, an internal row address is generated by the internal refresh counter approximately every 15.6 microseconds. This mode of refresh is used for systems requiring battery back-up, and saves additional system power by not requiring an external refresh address counter and address buffers. The power dissipation for either $\overline{\text{REFRESH}}$ mode is the same.

MCM6664A BIT ADDRESS MAP

Row Address A7 A6 A5 A4 A3 A2 A1 A0
Column Address A7 A6 A5 A4 A3 A2 A1 A0



Row Addresses

Hex	Dec	A0	A2	A1	A5	A4	A3	A6	A7
FE	254	0	1	1	1	1	1	1	1
FF	255	1	1	1	1	1	1	1	1
7E	126	0	1	1	1	1	1	1	0
7F	127	1	1	1	1	1	1	1	0
•	•								
08	8	0	0	0	1	0	0	0	0
06	6	0	1	1	0	0	0	0	0
07	7	1	1	1	0	0	0	0	0
05	5	1	0	1	0	0	0	0	0
04	4	0	0	1	0	0	0	0	0
02	2	0	1	0	0	0	0	0	0
03	3	1	1	0	0	0	0	0	0
01	1	1	0	0	0	0	0	0	0
00	0	0	0	0	0	0	0	0	0

Column Addresses

Hex	Dec	A7	A6	A3	A4	A5	A2	A0	A1
FE	254	1	1	1	1	1	1	1	0
FF	255	1	1	1	1	1	1	1	1
FC	252	1	1	1	1	1	1	0	0
FD	253	1	1	1	1	1	1	0	1
FA	250	1	1	1	1	1	0	1	0
FB	251	1	1	1	1	1	0	1	1
F8	248	1	1	1	1	1	0	0	0
F9	249	1	1	1	1	1	0	0	1
	•								
C0	192	1	1	0	0	0	0	0	0
C1	193	1	1	0	0	0	0	0	1
BF	191	1	0	1	1	1	1	1	1
BE	190	1	0	1	1	1	1	1	0
	•								
83	131	1	0	0	0	0	0	1	1
82	130	1	0	0	0	0	0	1	0
81	129	1	0	0	0	0	0	0	1
80	128	1	0	0	0	0	0	0	0
7E	126	0	1	1	1	1	1	1	0
7F	127	0	1	1	1	1	1	1	1
7C	124	0	1	1	1	1	1	0	0
	•								
	•								
	•								
42	66	0	1	0	0	0	0	1	0
43	67	0	1	0	0	0	0	1	1
40	64	0	1	0	0	0	0	0	0
41	65	0	1	0	0	0	0	0	1
3F	63	0	0	1	1	1	1	1	1
3E	62	0	0	1	1	1	1	1	0
3D	61	0	0	1	1	1	1	0	1
	•								
	•								
	•								
04	4	0	0	0	0	0	1	0	0
03	3	0	0	0	0	0	0	1	1
02	2	0	0	0	0	0	0	1	0
01	1	0	0	0	0	0	0	0	1
00	0	0	0	0	0	0	0	0	0

Data Stored $= D_{in} \oplus A_{0X} \oplus A_{1Y}$

Column Address A1	Row Address A0	Data Stored
0	0	True
0	1	Inverted
1	0	Inverted
1	1	True

MOTOROLA

MCM6665A

MOS

(N-CHANNEL, SILICON-GATE)

65,536-BIT DYNAMIC RANDOM ACCESS MEMORY

64K BIT DYNAMIC RAM

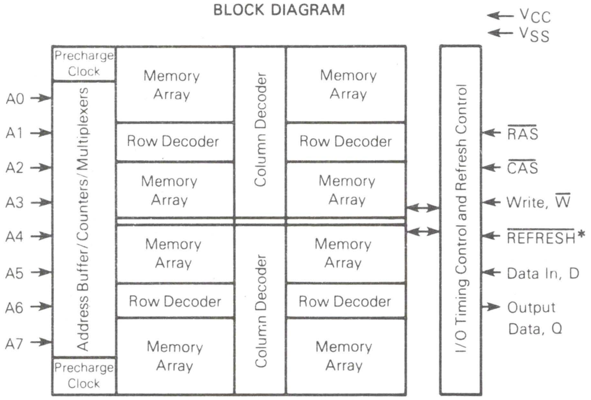
The MCM6665A is a 65,536 bit, high-speed, dynamic Random-Access Memory. Organized as 65,536 one-bit words and fabricated using HMOS high-performance N-channel silicon-gate technology, this new breed of 5-volt only dynamic RAM combines high performance with low cost and improved reliability.

By multiplexing row- and column-address inputs, the MCM6665A requires only eight address lines and permits packaging in standard 16-pin dual-in-line packages. Complete address decoding is done on chip with address latches incorporated. Data out is controlled by $\overline{\text{CAS}}$ allowing for greater system flexibility.

All inputs and outputs, including clocks, are fully TTL compatible. The MCM6665A incorporates a one-transistor cell design and dynamic storage techniques.

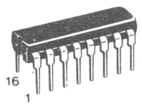
- Organized as 65,536 Words of 1 Bit
- Single +5 V Operation (±10%)
- Full Power Supply Range Capabilities
- Maximum Access Time
  MCM6665A-12 = 120 ns
  MCM6665A-15 = 150 ns
  MCM6665A-20 = 200 ns
- Low Power Dissipation
  302.5 mW Maximum (Active) (MCM6665A-15)
  22 mW Maximum (Standby)
- Three-State Data Output
- Internal Latches for Address and Data Input
- Early-Write Common I/O Capability
- 16K Compatible 128-Cycle, 2 ms Refresh
- $\overline{\text{RAS}}$-only Refresh Mode
- $\overline{\text{CAS}}$ Controlled Output
- Upward Pin Compatible from the 16K RAM (MCM4116, MCM4517)
- Fast Page Mode Cycle Time
- Low Soft Error Rate <0.1% per 1000 Hours (See Soft Error Testing)

BLOCK DIAGRAM

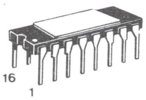


VCC
VSS
Precharge Clock
Memory Array
Column Decoder
Memory Array
A0
A1
A2
A3
A4
A5
A6
A7
Address Buffer/Counters/Multiplexers
Row Decoder
Row Decoder
Memory Array
Memory Array
Memory Array
Memory Array
Row Decoder
Row Decoder
Column Decoder
Memory Array
Memory Array
Precharge Clock
I/O Timing Control and Refresh Control
RAS
CAS
Write, W
REFRESH*
Data In, D
Output Data, Q

*Refresh Function Available on MCM6664A



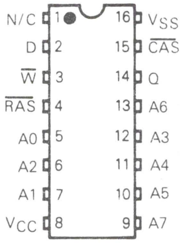
P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 690

Z SUFFIX, CERAMIC PACKAGE
ALSO AVAILABLE — CASE 752A

PIN ASSIGNMENT



N/C 1
D 2
W 3
RAS 4
A0 5
A2 6
A1 7
VCC 8
16 VSS
15 CAS
14 Q
13 A6
12 A3
11 A4
10 A5
9 A7

PIN NAMES

Pin	Name
A0-A7	Address Input
D	Data In
Q	Data Out
$\overline{\text{W}}$	Read/Write Input
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
V_{CC}	Power (+5 V)
V_{SS}	Ground

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

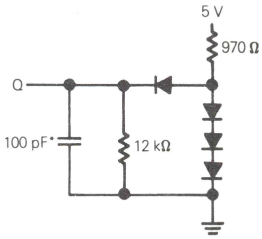
DS-9863/4-82

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS} (except V_{CC})	V_{in}, V_{out}	−2 to +7	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Power Dissipation	P_D	1.0	W
Data Out Current	I_{out}	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

FIGURE 1 — OUTPUT LOAD



*Includes Jig Capacitance

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	MCM6665A-12, -15, -20	V_{CC}	4.5	5.0	5.5	V	1
		V_{SS}	0	0	0	V	1
Logic 1 Voltage, All Inputs		V_{IH}	2.4	—	$V_{CC}+1$	V	1
Logic 0 Voltage, All Inputs		V_{IL}	−1.0*	—	0.8	V	1

*The device will withstand undershoots to the −2 volt level with a maximum pulse width of 20 ns at the −1.5 volt level. This is periodically sampled rather than 100% tested.

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Units	Notes
V_{CC} Power Supply Current (Standby)	I_{CC2}	—	4.0	mA	5
V_{CC} Power Supply Current 6665A-12, $t_{RC}=250$ ns 6665A-15, $t_{RC}=270$ ns 6665A-20, $t_{RC}=330$ ns	I_{CC1}	— — —	60 55 50	mA	4
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles 6665A-12, $t_{RC}=250$ ns 6665A-15, $t_{RC}=270$ ns 6665A-20, $t_{RC}=330$ ns	I_{CC3}	— — —	50 45 40	mA	4
V_{CC} Power Supply Current During Page Mode Cycle for $t_{RAS}=10$ μsec 6665A-12, $t_{PC}=t_{RP}=120$ ns 6665A-15, $t_{PC}=t_{RP}=145$ ns 6665A-20, $t_{PC}=t_{RP}=200$ ns	I_{CC4}	— — —	45 40 35	mA	4
Input Leakage Current ($V_{SS} \le V_{in} \le V_{CC}$)	$I_{I(L)}$	—	10	μA	—
Output Leakage Current ($\overline{CAS}$ at logic 1, $V_{SS} \le V_{out} \le V_{CC}$)	$I_{O(L)}$	—	10	μA	—
Output Logic 1 Voltage @ $I_{out}=-4$ mA	V_{OH}	2.4	—	V	—
Output Logic 0 Voltage @ $I_{out}=4$ mA	V_{OL}	—	0.4	V	—

CAPACITANCE ($f=1.0$ MHz, $T_A=25°C$, $V_{CC}=5$ V Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit	Notes
Input Capacitance (A0-A7), D	C_{I1}	3	5	pF	7
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	C_{I2}	6	8	pF	7
Output Capacitance (Q), ($\overline{CAS}=V_{IH}$ to disable output)	C_O	5	7	pF	7

NOTES:
1. All voltages referenced to V_{SS}.
2. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
3. An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
4. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
5. $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1.
6. The transition time specification applies for all inputs signals. In addition to meeting the transition rate specification, all input signals must transmit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
7. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C=\frac{I\Delta t}{\Delta V}$

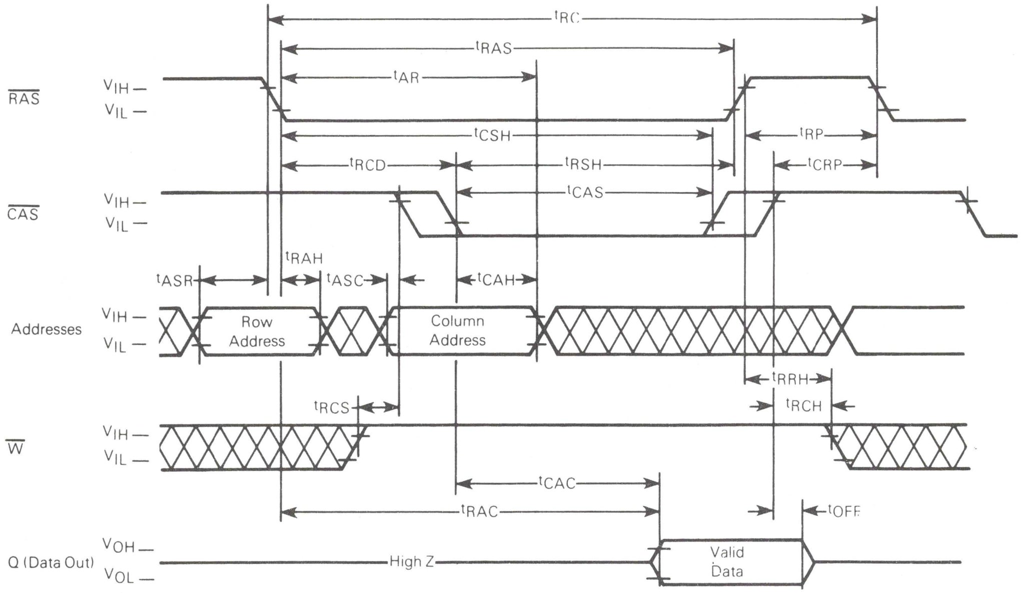
AC OPERATING CONDITIONS AND CHARACTERISTICS (Read, Write, and Read-Modify-Write Cycles)

(Full Operating Voltage and Temperature Range Unless Otherwise Noted; See Notes 2, 3, 6, and Figure 1)

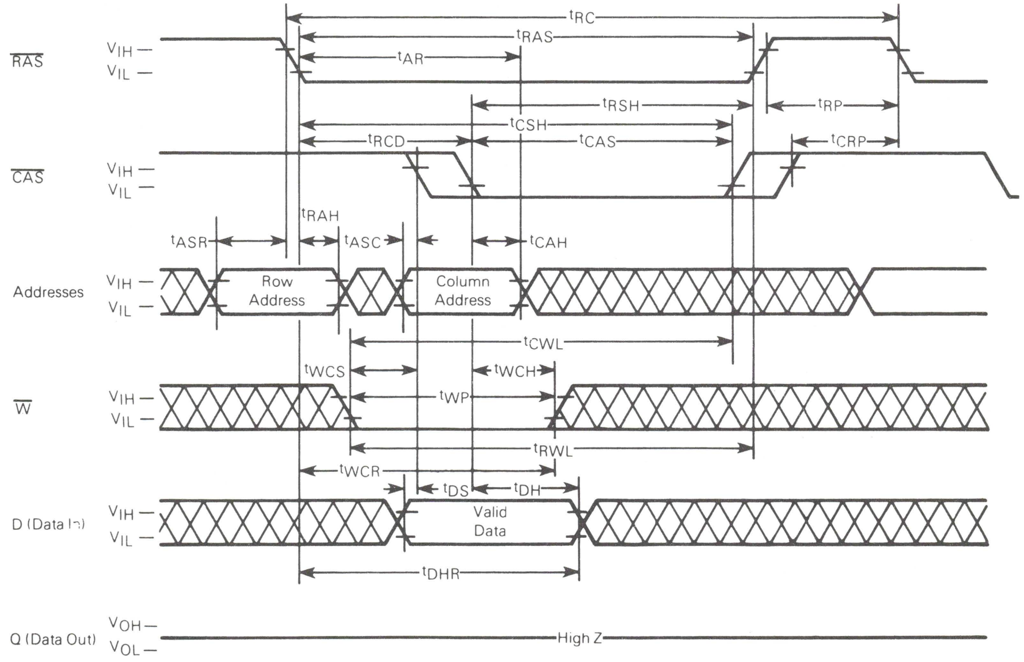
Parameter	Symbol	6665A-12		6665A-15		6665A-20		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	250	–	270	–	330	–	ns	8, 9
Read Write Cycle Time	t_{RWC}	255	–	280	–	345	–	ns	8, 9
Access Time from Row Address Strobe	t_{RAC}	–	120	–	150	–	200	ns	10, 12
Access Time from Column Address Strobe	t_{CAC}	–	60	–	75	–	100	ns	11, 12
Output Buffer and Turn-Off Delay	t_{OFF}	0	30	0	30	0	40	ns	18
Row Address Strobe Precharge Time	t_{RP}	100	–	100	–	120	–	ns	–
Row Address Strobe Pulse Width	t_{RAS}	120	10000	150	10000	200	10000	ns	–
Column Address Strobe Pulse Width	t_{CAS}	60	10000	75	10000	100	10000	ns	–
Row to Column Strobe Lead Time	t_{RCD}	25	60	30	75	35	100	ns	13
Row Address Setup Time	t_{ASR}	0	–	0	–	0	–	ns	–
Row Address Hold Time	t_{RAH}	15	–	20	–	25	–	ns	–
Column Address Setup Time	t_{ASC}	0	–	0	–	0	–	ns	–
Column Address Hold Time	t_{CAH}	25	–	35	–	45	–	ns	–
Column Address Hold Time Referenced to $\overline{\text{RAS}}$	t_{AR}	85	–	95	–	120	–	ns	17
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	6
Read Command Setup Time	t_{RCS}	0	–	0	–	0	–	ns	–
Read Command Hold Time	t_{RCH}	0	–	0	–	0	–	ns	14
Read Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{RRH}	0	–	0	–	0	–	ns	14
Write Command Hold Time	t_{WCH}	25	–	35	–	45	–	ns	–
Write Command Hold Time Referenced to $\overline{\text{RAS}}$	t_{WCR}	85	–	95	–	120	–	ns	17
Write Command Pulse Width	t_{WP}	25	–	35	–	45	–	ns	–
Write Command to Row Strobe Lead Time	t_{RWL}	40	–	45	–	55	–	ns	–
Write Command to Column Strobe Lead Time	t_{CWL}	40	–	45	–	55	–	ns	–
Data in Setup Time	t_{DS}	0	–	0	–	0	–	ns	15
Data in Hold Time	t_{DH}	25	–	35	–	45	–	ns	15
Data in Hold Time Referenced to $\overline{\text{RAS}}$	t_{DHR}	85	–	95	–	120	–	ns	17
Column to Row Strobe Precharge Time	t_{CRP}	– 10	–	– 10	–	– 10	–	ns	–
$\overline{\text{RAS}}$ Hold Time	t_{RSH}	60	–	75	–	100	–	ns	–
Refresh Period	t_{RFSH}	–	2.0	–	2.0	–	2.0	ms	–
$\overline{\text{WRITE}}$ Command Setup Time	t_{WCS}	– 10	–	– 10	–	– 10	–	ns	16
$\overline{\text{CAS}}$ to $\overline{\text{WRITE}}$ Delay	t_{CWD}	40	–	45	–	55	–	ns	16
$\overline{\text{RAS}}$ to $\overline{\text{WRITE}}$ Delay	t_{RWD}	100	–	120	–	155	–	ns	16
$\overline{\text{CAS}}$ Hold Time	t_{CSH}	120	–	150	–	200	–	ns	–
$\overline{\text{CAS}}$ Precharge Time (Page Mode Cycle Only)	t_{CP}	50	–	60	–	80	–	ns	–
Page Mode Cycle Time	t_{PC}	120	–	145	–	200	–	ns	–

8. The specifications for t_{RC} (min), and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
9. AC measurements $t_T = 5.0$ ns.
10. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
11. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
12. Measured with a current load equivalent to 2 TTL ($-200\ \mu A$, $+4$ mA) loads and 100 pF with the data output trip points set at $V_{OH} = 2.0$ V and $V_{OL} = 0.8$ V.
13. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in random write cycles and to $\overline{\text{WRITE}}$ leading edge in delayed write or read-modify-write cycles.
16. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
17. t_{AR} min $\leq t_{AR} = t_{RCD} + t_{CAH}$
    t_{DHR} min $\leq t_{DHR} = t_{RCD} + t_{DH}$
    t_{WCR} min $\leq t_{WCR} = t_{RCD} + t_{WCH}$
18. t_{off} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

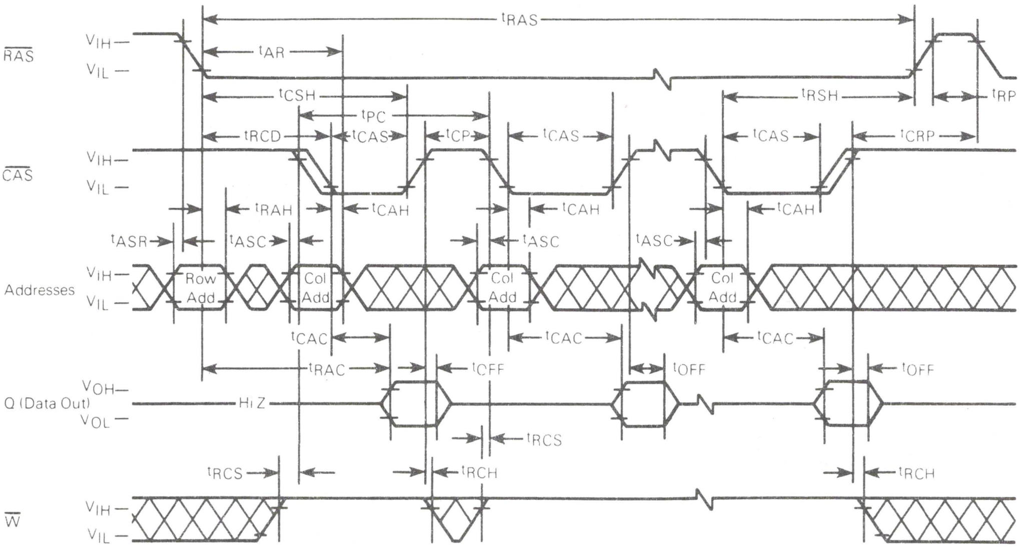
READ CYCLE TIMING


tRC
tRAS
tAR
RAS
VIH
VIL
tCSH
tRP
tRCD
tRSH
tCRP
tCAS
CAS
VIH
VIL
tRAH
tASR
tASC
tCAH
Addresses
VIH
VIL
Row Address
Column Address
tRRH
tRCS
tRCH
W
VIH
VIL
tCAC
tRAC
tOFF
Q (Data Out)
VOH
VOL
High Z
Valid Data

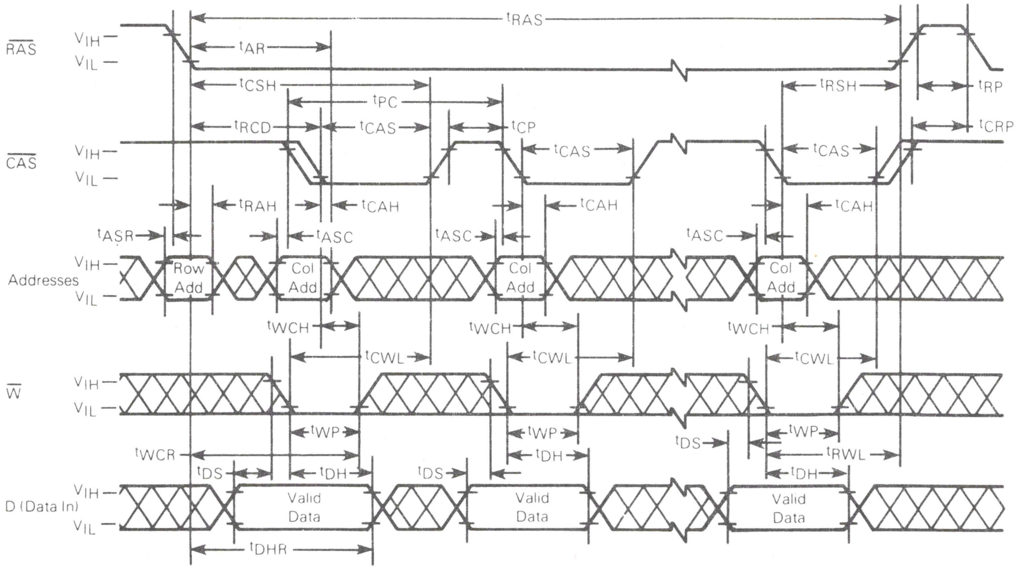
WRITE CYCLE TIMING


tRC
tRAS
tAR
RAS
VIH
VIL
tRSH
tRP
tCSH
tRCD
tCAS
tCRP
CAS
VIH
VIL
tRAH
tASR
tASC
tCAH
Addresses
VIH
VIL
Row Address
Column Address
tCWL
tWCS
tWCH
tWP
W
VIH
VIL
tRWL
tWCR
tDS
tDH
D (Data In)
VIH
VIL
Valid Data
tDHR
Q (Data Out)
VOH
VOL
High Z

PAGE MODE READ CYCLE

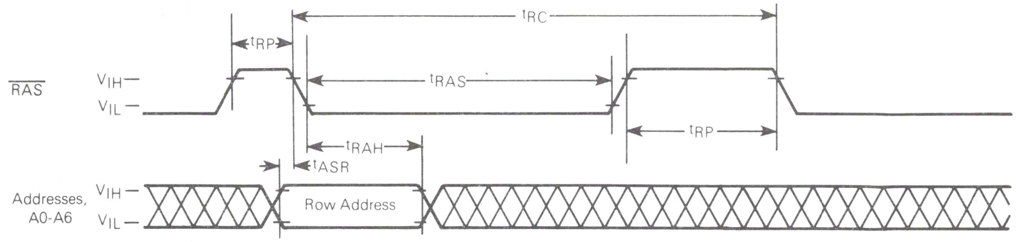

tRAS
RAS
VIH
VIL
tAR
tCSH
tRSH
tRP
tPC
tRCD
tCAS
tCP
tCAS
tCAS
tCRP
CAS
VIH
VIL
tRAH
tCAH
tCAH
tCAH
tASR
tASC
tASC
tASC
Addresses
VIH
VIL
Row Add
Col Add
Col Add
Col Add
tCAC
tCAC
tCAC
tRAC
tOFF
tOFF
tOFF
Q (Data Out)
VOH
VOL
Hi Z
tRCS
tRCS
tRCH
tRCH
W
VIH
VIL

PAGE MODE WRITE CYCLE

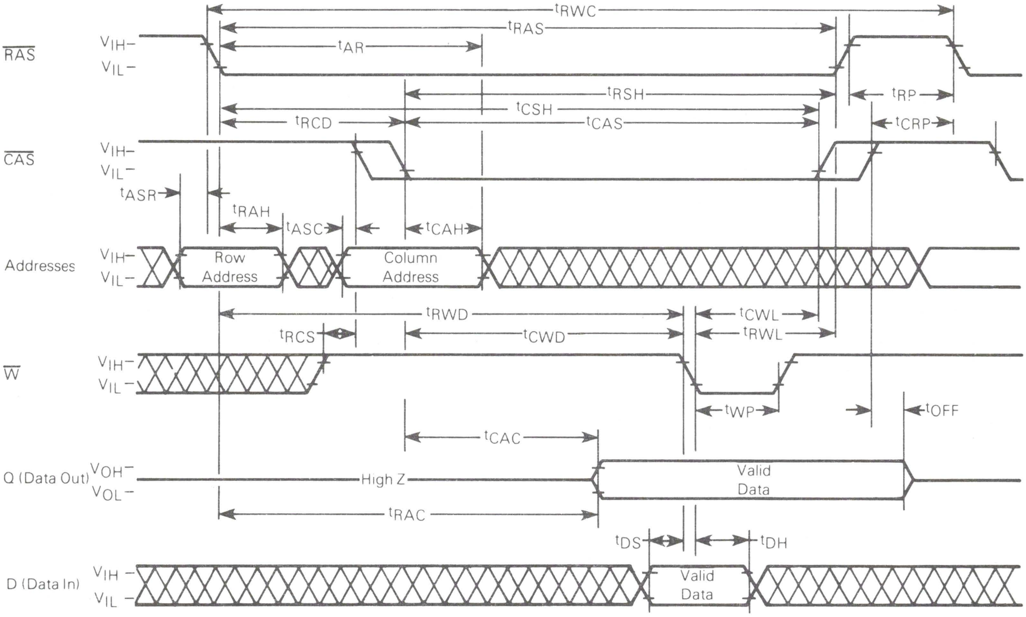

tRAS
RAS
VIH
VIL
tAR
tCSH
tRSH
tRP
tPC
tRCD
tCAS
tCP
tCRP
tCAS
tCAS
CAS
VIH
VIL
tRAH
tCAH
tCAH
tCAH
tASR
tASC
tASC
tASC
Addresses
VIH
VIL
Row Add
Col Add
Col Add
Col Add
tWCH
tWCH
tWCH
tCWL
tCWL
tCWL
W
VIH
VIL
tWP
tWP
tWP
tWCR
tDS
tDH
tDS
tDH
tDS
tDH
tRWL
D (Data In)
VIH
VIL
Valid Data
Valid Data
Valid Data
tDHR

$\overline{\text{RAS}}$-ONLY REFRESH CYCLE

(Data-in and $\overline{\text{Write}}$ are Don't Care, $\overline{\text{CAS}}$ is HIGH)


tRC
tRP
tRAS
tRP
tRAH
tASR
RAS
VIH
VIL
Addresses, A0-A6
VIH
VIL
Row Address

READ-WRITE/READ-MODIFY-WRITE CYCLE


tRWC
tRAS
tAR
tRSH
tRP
tCSH
tRCD
tCAS
tCRP
RAS
VIH
VIL
CAS
VIH
VIL
tASR
tRAH
tASC
tCAH
Addresses
VIH
VIL
Row Address
Column Address
tRWD
tCWL
tRCS
tCWD
tRWL
W
VIH
VIL
tWP
tOFF
tCAC
Q (Data Out)
VOH
VOL
High Z
Valid Data
tRAC
tDS
tDH
D (Data In)
VIH
VIL
Valid Data

TYPICAL CHARACTERISTICS

FIGURE 2 — $\overline{\text{RAS}}$ ACCESS TIME versus SUPPLY VOLTAGE

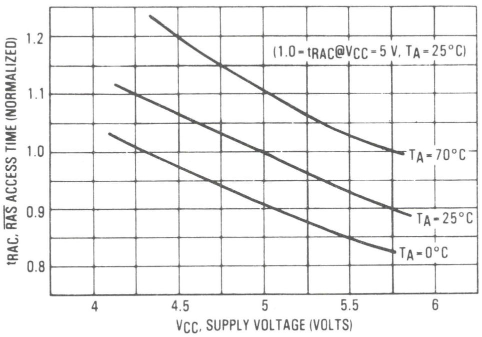


FIGURE 3 — $\overline{\text{CAS}}$ ACCESS TIME versus SUPPLY VOLTAGE

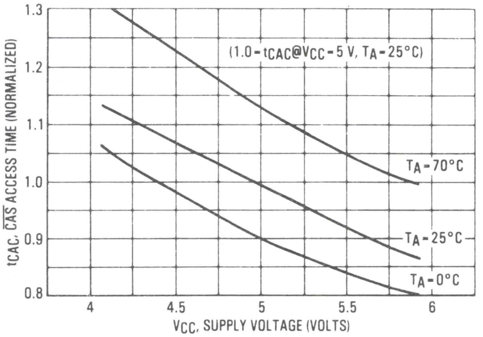


FIGURE 4 — $\overline{\text{RAS}}$ ACCESS TIME versus AMBIENT TEMPERATURE

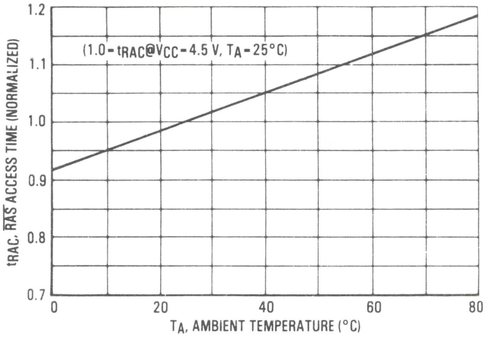


FIGURE 5 — $\overline{\text{CAS}}$ ACCESS TIME versus AMBIENT TEMPERATURE

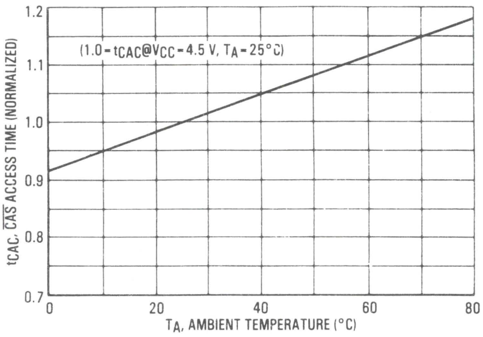


FIGURE 6 — $\overline{\text{RAS}}$, $\overline{\text{W}}$ INPUT LEVEL versus SUPPLY VOLTAGE

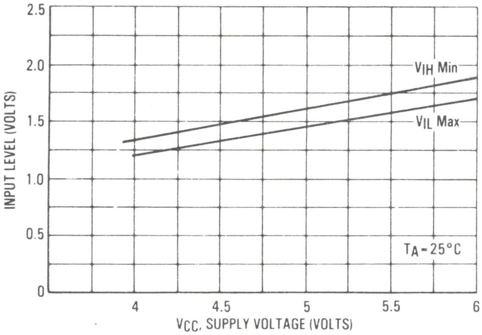
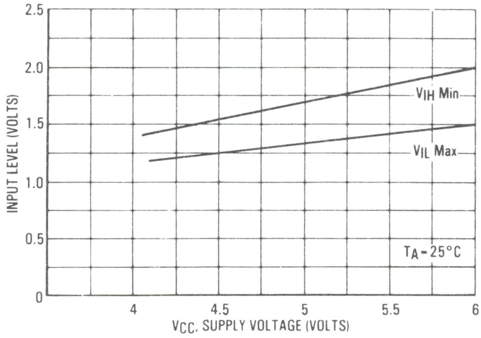


FIGURE 7 — $\overline{\text{CAS}}$, $\overline{\text{W}}$ INPUT LEVEL versus SUPPLY VOLTAGE



TYPICAL CHARACTERISTICS (continued)

FIGURE 8 — I_{CC1} SUPPLY CURRENT versus CYCLE RATE

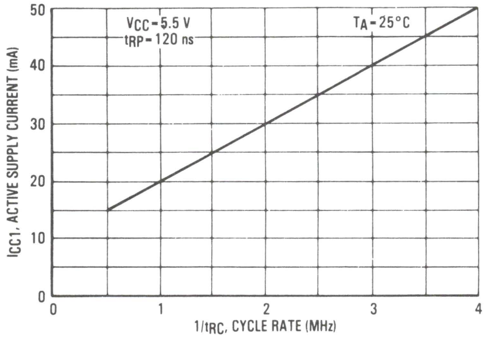


FIGURE 9 — I_{CC1} SUPPLY CURRENT versus SUPPLY VOLTAGE

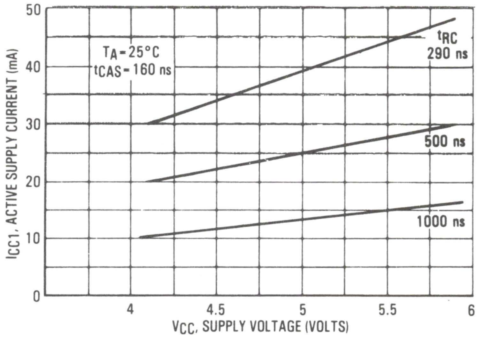


FIGURE 10 — I_{CC1} SUPPLY CURRENT versus SUPPLY VOLTAGE

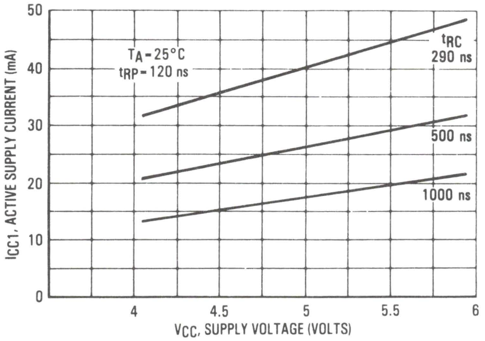


FIGURE 11 — I_{CC1} SUPPLY CURRENT versus AMBIENT TEMPERATURE (min t_{RP})

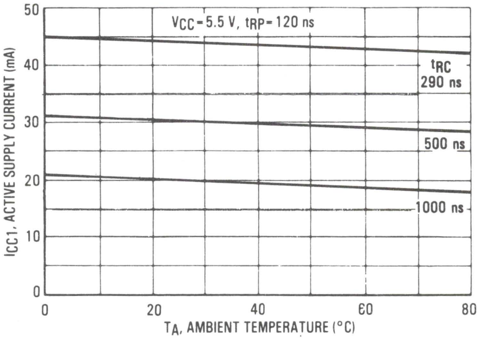


FIGURE 12 — I_{CC1} SUPPLY CURRENT versus AMBIENT TEMPERATURE (min $\overline{RAS}$)

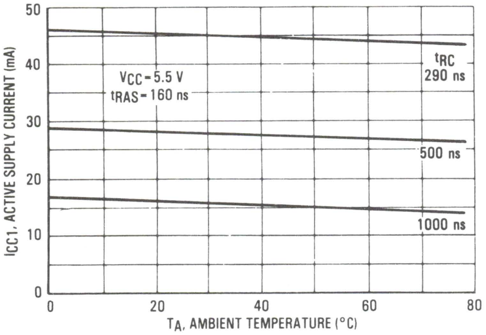
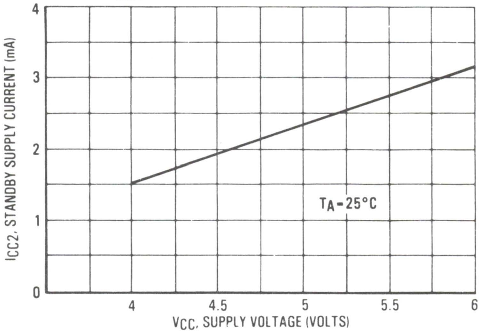


FIGURE 13 — I_{CC2} SUPPLY CURRENT versus SUPPLY VOLTAGE



TYPICAL CHARACTERISTICS (continued)

FIGURE 14 — I_{CC2} STANDBY CURRENT versus AMBIENT TEMPERATURE

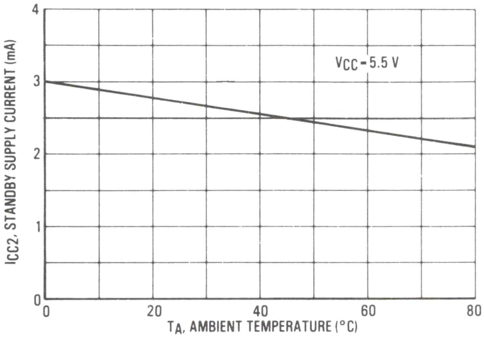


FIGURE 15 — I_{CC3} SUPPLY CURRENT versus CYCLE RATE

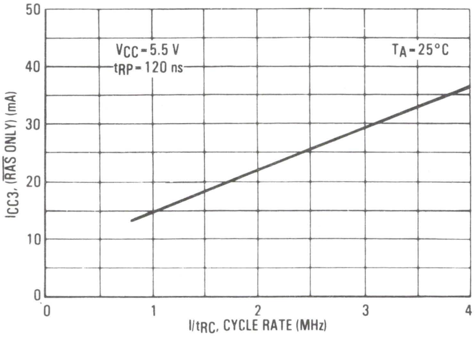


FIGURE 16 — ADDRESS INPUT LEVEL versus SUPPLY VOLTAGE

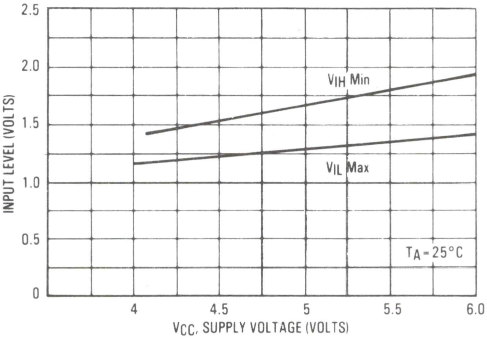
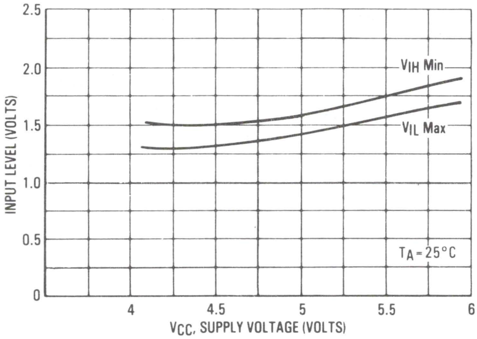


FIGURE 17 — DATA INPUT LEVEL versus SUPPLY VOLTAGE



SOFT ERROR TESTING

The storage cell depletion regions as well as the sense amplifier and its associated bit lines are susceptible to charge collection of electrons from an alpha "hit." However, the susceptibility of these vulnerable regions varies. Depleted storage cells are vulnerable at all times, whereas the sense amplifiers and associated bit lines are susceptible only during the small portion of the memory cycle just prior to sensing. Hence, an increase in the frequency of dynamic RAM access will cause a corresponding increase in the soft error rate.

To take this memory access dependency into account, the total soft error rate profile includes a cycle time component. The soft error rate due to bit line hits at the system's memory cycle rate is added to the soft error rate due to storage cell hits which are not frequency dependent. Figure 18 illustrates the impact that frequency of access has on the MCM6664A/MCM6665A overall soft error rate.

Under normal operating conditions, the die will be exposed to radiation levels of less than 0.01 alpha/cm^2/hr. Accelerated soft error testing data is generated from at least three high-intensity sources having an Alpha Flux Density range of 1×10^5 to 6×10^5 (alpha/cm^{2}hr) placed over uncoated die. Figure 19 shows the soft error rate for a given alpha flux density at a cycle rate of 100 kHz. The accelerated data of Figures 18 and 19 project that the soft error rate for package level radiation will be less than 0.1%/1000 hours.

SYSTEM LIFE OPERATING TEST CONDITIONS

1) Cycle time: 1 microsecond for read, write and refresh cycles
2) Refresh Rate: 1 millisecond
3) Voltage: 5.0 V
4) Temperature: 30° C ±2° C (ambient temperature inside enclosure)
5) Elevation: Approximately 620 feet above mean sea level
6) Data Patterns: Write the entire memory space sequentially with all "1"s and then perform continuous sequential reads for 6 hours. Next, write the entire memory space with all "0"s sequentially and then perform continuous sequential reads for 6 hours. Next, go back to the all "1"s pattern and repeat the sequences all over again.

FIGURE 18 — ACCELERATED SOFT ERROR versus CYCLE TIME

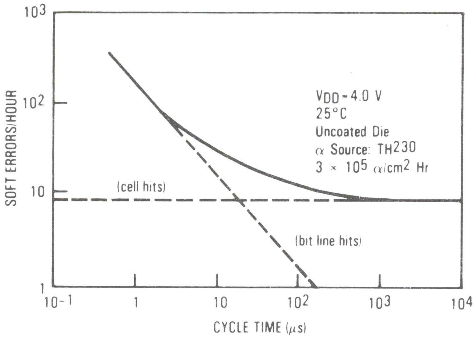
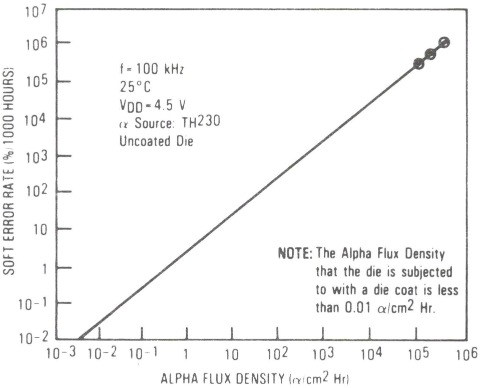


FIGURE 19 — SOFT ERROR RATE versus ALPHA FLUX DENSITY



CURRENT WAVEFORMS

FIGURE 20 — $\overline{RAS}/\overline{CAS}$ CYCLE

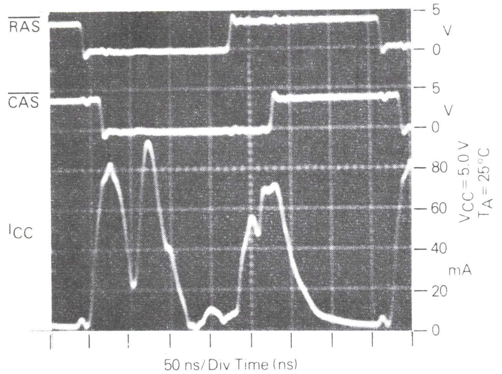


FIGURE 21 — LONG $\overline{RAS}/\overline{CAS}$ CYCLE

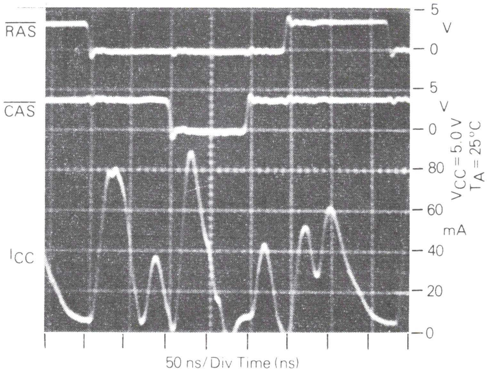


FIGURE 22 — $\overline{RAS}$ ONLY CYCLE

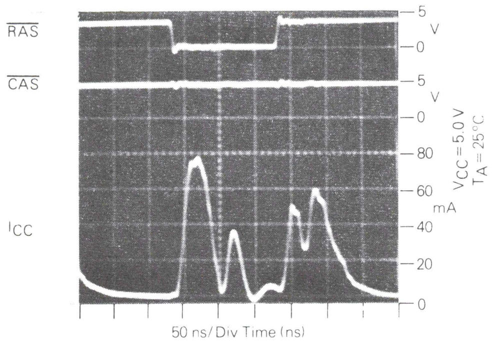


FIGURE 23 — PAGE MODE CYCLE

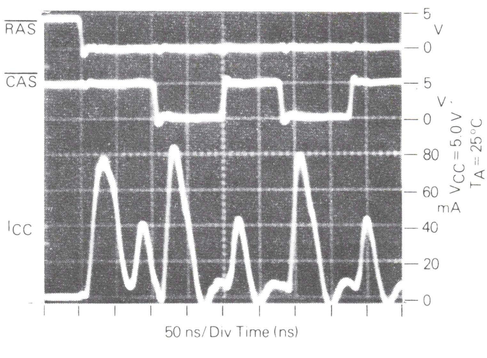
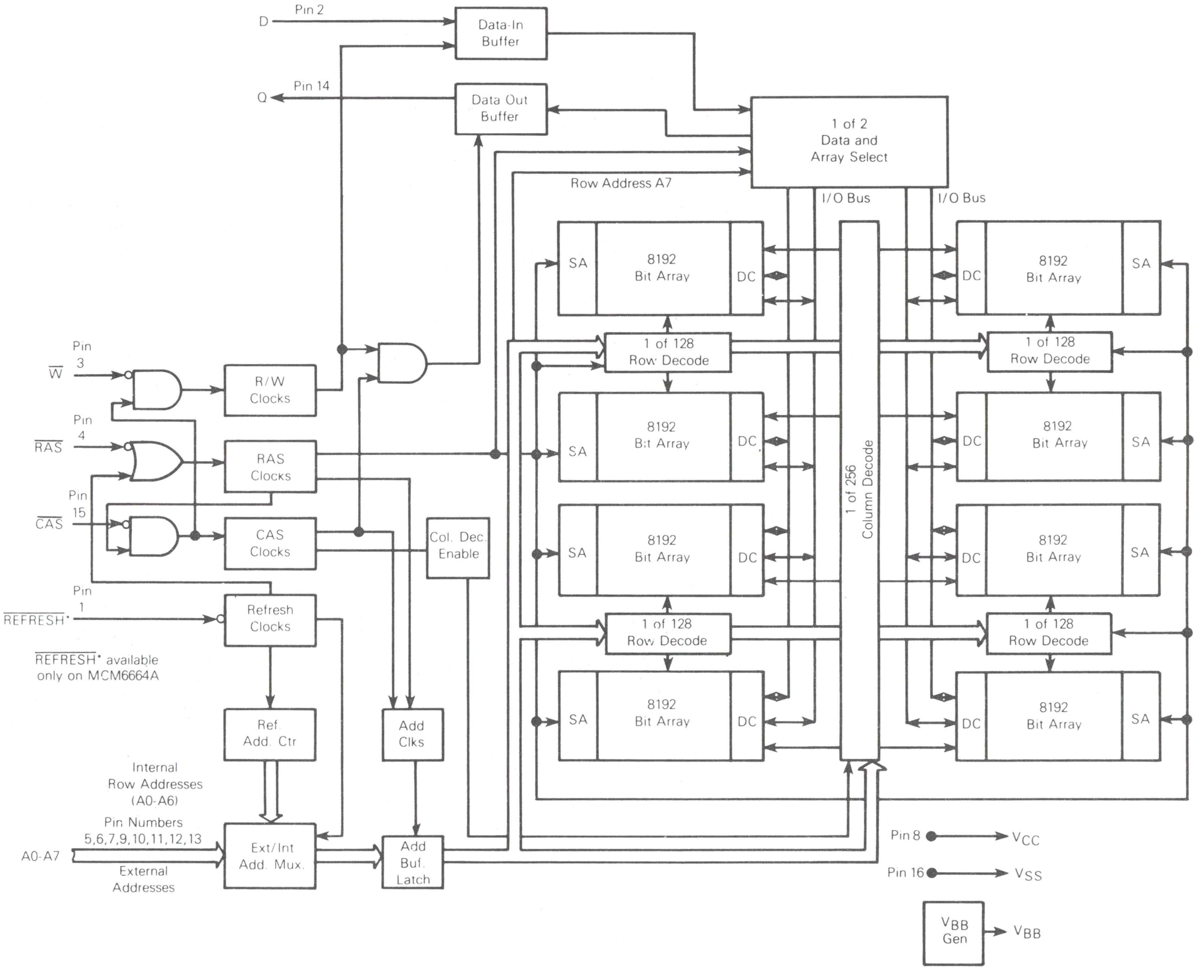


FIGURE 24 — FUNCTIONAL BLOCK DIAGRAM


D
Pin 2
Data-In Buffer
Q
Pin 14
Data Out Buffer
1 of 2 Data and Array Select
Row Address A7
I/O Bus
I/O Bus
SA
8192 Bit Array
DC
1 of 128 Row Decode
1 of 256 Column Decode
Pin 3
W̅
R/W Clocks
Pin 4
RAS̅
RAS Clocks
Pin 15
CAS̅
CAS Clocks
Col. Dec. Enable
Pin 1
REFRESH̅*
Refresh Clocks
Ref. Add. Ctr
Add Clks
Internal Row Addresses (A0-A6)
Pin Numbers 5,6,7,9,10,11,12,13
A0-A7
External Addresses
Ext/Int Add. Mux.
Add Buf. Latch
Pin 8
VCC
Pin 16
VSS
VBB Gen
VBB

REFRESH̅* available only on MCM6664A

DEVICE INITIALIZATION

Since the 64K dynamic RAM is a single supply 5 V only device, the need for power supply sequencing is no longer required as was the case in older generation dynamic RAMs. On power-up an initial pause of 100 microseconds is required for the internal substrate generator pump to establish the correct bias voltage. This is to be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize the various dynamic nodes internal to the device. During an extended inactive state of the device (greater than 2 ms with device powered up) the wake up sequence (8 active cycles) will be necessary to assure proper device operation. See Figures 25, 26 for power on characteristics of the RAM for two conditions (clocks active, clocks inactive).

The row address strobe is the primary "clock" that activates the device and maintains the data when the RAM is in the standby mode. This is the main feature that distinquishes it as a dynamic RAM as opposed to a static RAM. A dynamic RAM is placed in a low power standby mode when the device receives a positive-going row address strobe. The variation in the power dissipation of a dynamic RAM from the active to the standby state is an order of magnitude or more for NMOS devices. This feature is used to its fullest advantage with high density mainframe memory systems, where only a very small percentage of the devices are in the active mode at any one time and the rest of the devices are in the standby mode. Thus, large memory systems can be assembled that dissipate very low power per bit compared to a system where all devices are active continuously.

ADDRESSING THE RAM

The eight address pins on the device are time multiplexed with two separate 8-bit address fields that are strobed at the beginning of the memory cycle by two clocks (active negative) called the row address strobe and the column address strobe. A total of sixteen address bits will decode one of the 65,536 cell locations in the device. The column address strobe follows the row address strobe by a specified minimum and maximum time called "t_{RCD}," which is the row to column strobe delay. This time interval is also referred to as the multiplex window which gives flexibility to a system designer to set up his external addresses into the RAM. These conditions have to be met for normal read or write cycles. This initial portion of the cycle accomplishes the normal addressing of the device. There are, however, two other variations in addressing the 64K RAM: one is called the page mode cycle (described later) where an 8-bit column address field is presented on the input pins and latched by the $\overline{\text{CAS}}$ clock, and the other is the $\overline{\text{RAS}}$ only refresh cycle (described later) where a 7-bit row address field is presented on the input pins and latched by the $\overline{\text{RAS}}$ clock. In the latter case, the most significant bit on Row Address A7 (pin 9) is not required for refresh. See bit address map for the topology of the cells and their address selection.

NORMAL READ CYCLE

A read cycle is referred to as normal read cycle to differentiate if from a page-mode-read cycle, a read-while-write cycle, and read-modify-write cycle which are covered in a later section.

The memory read cycle begins with the row addresses valid and the $\overline{\text{RAS}}$ clock transitioning from V_{IH} to the V_{IL} level. The $\overline{\text{CAS}}$ clock must also make a transition from V_{IH} to the V_{IL} level at the specified t_{RCD} timing limits when the column addresses are latched. Both the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. Also, these clocks are linked in such a manner that the access time of the device is independent of the address multiplex window. The only stipulation is that the $\overline{\text{CAS}}$ clock must be active before or at

CURRENT WAVEFORMS

FIGURE 25 — SUPPLY CURRENT versus SUPPLY VOLTAGE DURING POWER UP, $\overline{\text{RAS}}$, $\overline{\text{CAS}} = V_{CC}$

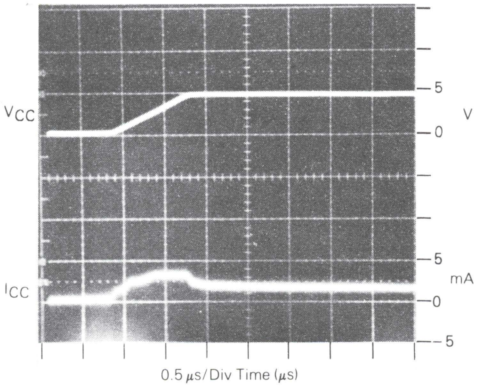
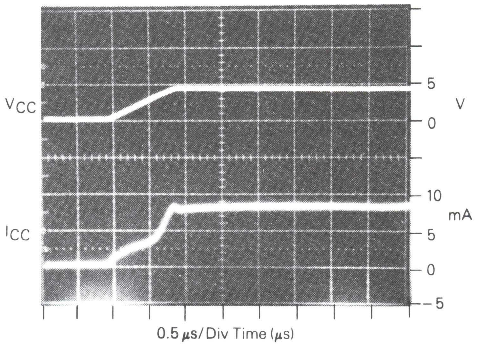


FIGURE 26 — SUPPLY CURRENT versus SUPPLY VOLTAGE DURING POWER UP, $\overline{\text{RAS}}$, $\overline{\text{CAS}} = V_{SS}$



the t_{RCD} maximum specification for an access (data valid) from the $\overline{RAS}$ clock edge to be guaranteed (t_{RAC}). If the t_{RCD} maximum condition is not met, the access (t_{CAC}) from the $\overline{CAS}$ clock active transition will determine read access time. The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available, as noted in the functional block diagram, Figure 24. This gating feature on the $\overline{CAS}$ clock will allow the external $\overline{CAS}$ signal to become active as soon as the row address hold time (t_{RAH}) specification has been met and defines the t_{RCD} minimum specification. The time difference between t_{RCD} minimum and t_{RCD} maximum can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

Once the clocks have become active, they must stay active for the minimum (t_{RAS}) period for the $\overline{RAS}$ clock and the minimum (t_{CAS}) period for the $\overline{CAS}$ clock. The $\overline{RAS}$ clock must stay inactive for the minimum (t_{RP}) time. The former is for the completion of the cycle in progress, and the latter is for the device internal circuitry to be precharged for the next active cycle.

Data out is not latched and is valid as long as the $\overline{CAS}$ clock is active; the output will switch to the three-state mode when the $\overline{CAS}$ clock goes inactive. The $\overline{CAS}$ clock can remain active for a maximum of 10 ns (t_{CRP}) into the next cycle. To perform a read cycle, the write ($\overline{W}$) input must be held at the V_{IH} level from the time the $\overline{CAS}$ clock makes its active transition (t_{RCS}) to the time when it transitions into the inactive (t_{RCH}) mode.

WRITE CYCLE

A write cycle is similar to a read cycle except that the Write ($\overline{W}$) clock must go active (V_{IL} level) at or before the $\overline{CAS}$ clock goes active at a minimum t_{WCS} time. If the above condition is met, then the cycle in progress is referred to as a early write cycle. In an early write cycle, the write clock and the data in is referenced to the active transition of the $\overline{CAS}$ clock edge. There are two important parameters with respect to the write cycle: the column strobe to write lead time (t_{CWL}) and the row strobe to write lead time (t_{RWL}). These define the minimum time that $\overline{RAS}$ and $\overline{CAS}$ clocks need to be active after the write operation has started ($\overline{W}$ clock at V_{IL} level).

It is also possible to perform a late write cycle. For this cycle the write clock is activated after the $\overline{CAS}$ goes low which is beyond t_{WCS} minimum time. Thus the parameters t_{CWL} and t_{RWL} must be satisifed before terminating this cycle. The difference between an early write cycle and a late write cycle is that in a late write cycle the write ($\overline{W}$) clock can occur much later in time with respect to the active transition of the $\overline{CAS}$ clock. This time could be as long as 10 microseconds — $[t_{RWL} + t_{RP} + 2T_t]$.

At the start of a write cycle, the data out is in a three-state condition and remains inactive throughout the cycle. The data out remains three-state because the active transition of the write ($\overline{W}$) clock prevents the $\overline{CAS}$ clock from enabling the data-out buffers as noted in Functional Block Diagram. The three-state condition (high impedance) of the Data Out Pin during a write cycle can be effectively utilized in a system that has a common input/output bus. The only stipulation is that the system use only early write mode operations for all write cycles to avoid bus contention.

READ-MODIFY-WRITE AND READ-WHILE-WRITE CYLES

As the name implies, both a read and a write cycle is accomplished at a selected bit during a single access. The read-modify-write cycle is similar to the late write cycle discussed above.

For the read-modify-write cycle a normal read cycle is initiated with the write ($\overline{W}$) clock at the V_{IH} level until the read data occurs at the device access time (t_{RAC}). At this time the write ($\overline{W}$) clock is asserted. The data in is setup and held with respect to the active edge of the write clock. The cycle described assumes a zero modify time between read and write.

Another variation of the read-modify-write cycle is the read-while-write cycle. For this cycle, the following parameters (t_{RWD}, t_{CWD}) play an important role. A read-while-write cycle starts as a normal read cycle with the write ($\overline{W}$) clock being asserted at minimum t_{RWD} or minimum t_{CWD} time, depending upon the application. This results in starting a write operation to the selected cell even before data out occurs. The minimum specification on t_{RWD} and t_{CWD} assures that data out does occur. In this case, the data in is set up with respect to write ($\overline{W}$) clock active edge.

PAGE-MODE CYCLES

Page mode operation allows faster successive data operations at the 256 column locations. Page access (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access (t_{RAC}) on the Motorola 64K dynamic RAM. Page mode operation consists of holding the $\overline{RAS}$ clock active while cycling the $\overline{CAS}$ clock to access the column locations determined by the 8-bit column address field. There are two controlling factors that limit the access to all 256 column locations in one $\overline{RAS}$ clock active operation. These are the refresh interval of the device (2 ms/128 = 15.6 microseconds) and the maximum active time specification for the $\overline{RAS}$ clock (10 microseconds). Since 10 microseconds is the smaller value, the maximum specification of the $\overline{RAS}$ clock on time is the limiting factor of the number of sequential page accesses possible. Ten microseconds will provide approximately (10 microseconds/page mode cycle time) 50 successive page accesses for every row address selected before the $\overline{RAS}$ clock is reset.

The page cycle is always initiated with a row address being provided and latched by the $\overline{RAS}$ clock, followed by the column address and $\overline{CAS}$ clock. From the timing illustrated, the initial cycle is a normal read or write cycle, that has been previously described, followed by the shorter $\overline{CAS}$ cycles (t_{PC}). The $\overline{CAS}$ cycle time (t_{PC}) consists of the $\overline{CAS}$ clock active time (t_{CAS}), and $\overline{CAS}$ clock precharge time (t_{CP}) and two transitions. In addition to read and write cycles, a read-modify-write cycle can also be performed in a page mode operation. For a read-modify-write or read-while-write type cycle, the conditions normal to that mode of operation will apply in the page mode also. The page mode cycles illustrated show a series of sequential reads separated by a series of sequential writes. This is just one mode of operation. In practice, any combination of read, write and read-modify-write cycles can be performed to suit a particular application.

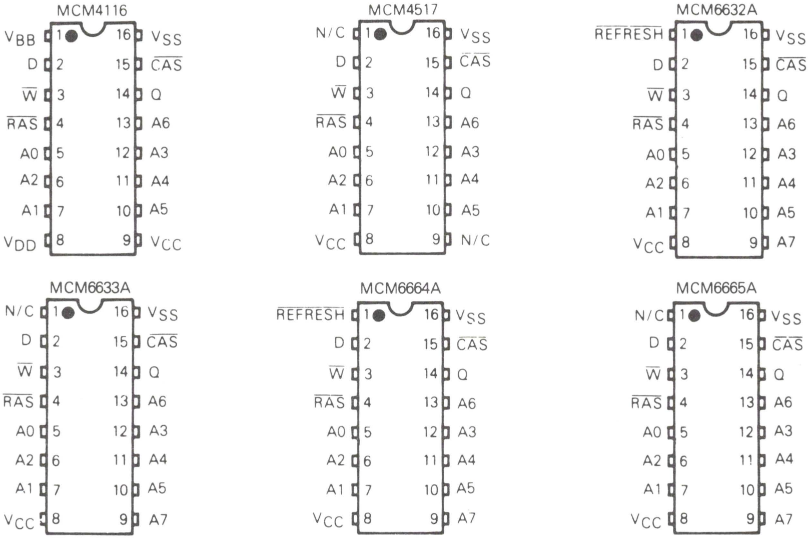
REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to

degrade with time and temperature. Therefore, to retain the correct information, the bits need to be refreshed at least once every 2 ms. This is accomplished by sequentially cycling through the 128 row address locations every 2 ms, or at least one row every 15.6 microseconds. A normal read or write operation to the RAM will serve to refresh all the bits (256) associated with that particular row decoded.

$\overline{\text{RAS}}$ Only Refresh — When the memory component is in standby the $\overline{\text{RAS}}$ only refresh scheme is employed. This refresh method performs a $\overline{\text{RAS}}$ only cycle on all 128 row addresses every 2 ms. The row addresses are latched in with the $\overline{\text{RAS}}$ clock, and the associated internal row locations are refreshed. As the heading implies, the $\overline{\text{CAS}}$ clock is not required and should be inactive or at a V_{IH} level to conserve power.

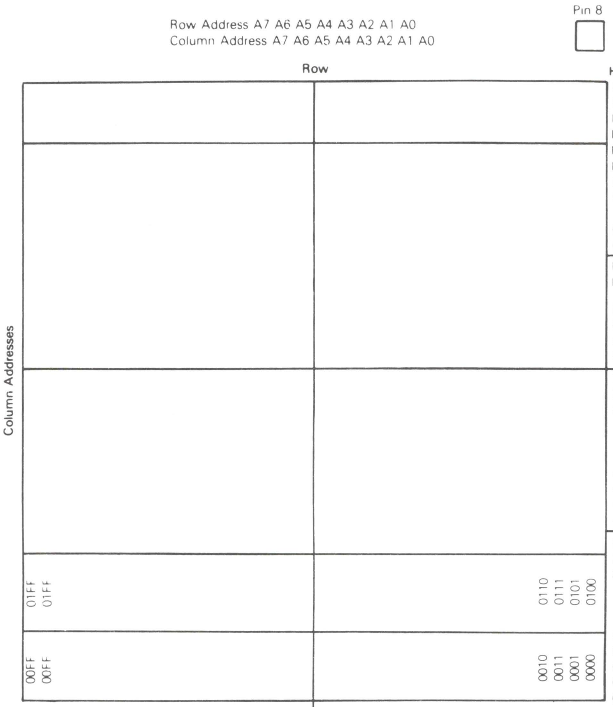
PIN ASSIGNMENT COMPARISON


MCM4116
VBB 1, D 2, W 3, RAS 4, A0 5, A2 6, A1 7, VDD 8
16 VSS, 15 CAS, 14 Q, 13 A6, 12 A3, 11 A4, 10 A5, 9 VCC
MCM4517
N/C 1, D 2, W 3, RAS 4, A0 5, A2 6, A1 7, VCC 8
16 VSS, 15 CAS, 14 Q, 13 A6, 12 A3, 11 A4, 10 A5, 9 N/C
MCM6632A
REFRESH 1, D 2, W 3, RAS 4, A0 5, A2 6, A1 7, VCC 8
16 VSS, 15 CAS, 14 Q, 13 A6, 12 A3, 11 A4, 10 A5, 9 A7
MCM6633A
N/C 1, D 2, W 3, RAS 4, A0 5, A2 6, A1 7, VCC 8
16 VSS, 15 CAS, 14 Q, 13 A6, 12 A3, 11 A4, 10 A5, 9 A7
MCM6664A
REFRESH 1, D 2, W 3, RAS 4, A0 5, A2 6, A1 7, VCC 8
16 VSS, 15 CAS, 14 Q, 13 A6, 12 A3, 11 A4, 10 A5, 9 A7
MCM6665A
N/C 1, D 2, W 3, RAS 4, A0 5, A2 6, A1 7, VCC 8
16 VSS, 15 CAS, 14 Q, 13 A6, 12 A3, 11 A4, 10 A5, 9 A7

PIN VARIATIONS

PIN NUMBER	MCM4116	MCM4517	MCM6632A	MCM6663A	MCM6664A	MCM6665A
1	V_{BB}(−5 V)	N/C	REFRESH	N/C	REFRESH	N/C
8	V_{DD}(+12 V)	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
9	V_{CC}(+5 V)	N/C	A7	A7	A7	A7

MCM6665A BIT ADDRESS MAP


Row Address A7 A6 A5 A4 A3 A2 A1 A0
Column Address A7 A6 A5 A4 A3 A2 A1 A0
Pin 8
Row
Column Addresses
01FF
01FF
0110
0111
0101
0100
00FF
00FF
0010
0011
0001
0000

Column Addresses

Hex	Dec	A7	A6	A3	A4	A5	A2	A0	A1
FE	254	1	1	1	1	1	1	1	0
FF	255	1	1	1	1	1	1	1	1
FC	252	1	1	1	1	1	1	0	0
FD	253	1	1	1	1	1	1	0	1
FA	250	1	1	1	1	1	0	1	0
FB	251	1	1	1	1	1	0	1	1
F8	248	1	1	1	1	1	0	0	0
F9	249	1	1	1	1	1	0	0	1
	•								
C0	192	1	1	0	0	0	0	0	0
C1	193	1	1	0	0	0	0	0	1
BF	191	1	0	1	1	1	1	1	1
BE	190	1	0	1	1	1	1	1	0
	•								
83	131	1	0	0	0	0	0	1	1
82	130	1	0	0	0	0	0	1	0
81	129	1	0	0	0	0	0	0	1
80	128	1	0	0	0	0	0	0	0
7E	126	0	1	1	1	1	1	1	0
7F	127	0	1	1	1	1	1	1	1
7C	124	0	1	1	1	1	1	0	0
	• • •								
42	66	0	1	0	0	0	0	1	0
43	67	0	1	0	0	0	0	1	1
40	64	0	1	0	0	0	0	0	0
41	65	0	1	0	0	0	0	0	1
3F	63	0	0	1	1	1	1	1	1
3E	62	0	0	1	1	1	1	1	0
3D	61	0	0	1	1	1	1	0	1
	• • •								
04	4	0	0	0	0	0	1	0	0
03	3	0	0	0	0	0	0	1	1
02	2	0	0	0	0	0	0	1	0
01	1	0	0	0	0	0	0	0	1
00	0	0	0	0	0	0	0	0	0

Row Addresses

Hex	Dec	A0	A2	A1	A5	A4	A3	A6	A7
FF	254	0	1	1	1	1	1	1	1
FF	255	1	1	1	1	1	1	1	1
7E	126	0	1	1	1	1	1	1	0
7F	127	1	1	1	1	1	1	1	0
	• • • • • • • •								
08	8	0	0	0	1	0	0	0	0
06	6	0	1	1	0	0	0	0	0
07	7	1	1	1	0	0	0	0	0
05	5	1	0	1	0	0	0	0	0
04	4	0	0	1	0	0	0	0	0
02	2	0	1	0	0	0	0	0	0
03	3	1	1	0	0	0	0	0	0
01	1	1	0	0	0	0	0	0	0
00	0	0	0	0	0	0	0	0	0

Pin 16

Data Stored = $D_{in} \oplus A_{0X} \oplus A_{1Y}$

Column Address A1	Row Address A0	Data Stored
0	0	True
0	1	Inverted
1	0	Inverted
1	1	True

MOTOROLA

MCM6256

Product Preview

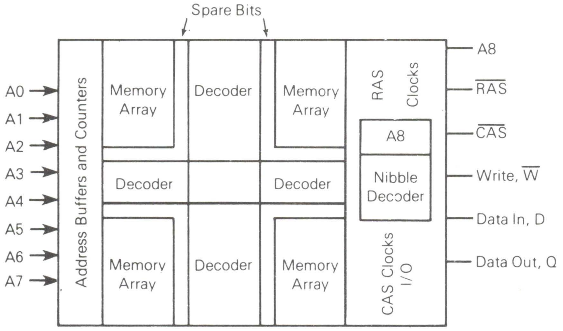
256K-BIT DYNAMIC RAM

The MCM6256 is a 262,144 bit, high-speed, dynamic Random Access Memory. Organized as 262,144 one-bit words and fabricated using Motorola's high-performance silicon-gate MOS (HMOS) technology, this new single +5 volt supply dynamic RAM combines high performance with low cost and improved reliability. The MCM6256 has the capability of using laser fuse redundancy and is manufactured using advanced direct-step on wafer photolithographic equipment.

By multiplexing row and column address inputs, the MCM6256 requires only nine address lines and permits packaging in standard 16-pin 300 mil wide dual-in-line packages. Complete address decoding is done on-chip with address latches incorporated. Data out (Q) is controlled by $\overline{\text{CAS}}$ allowing greater system flexibility.

All inputs and outputs, including clocks, are fully TTL compatible. The MCM6256 incorporates a one transistor cell design and dynamic storage techniques. In addition to the $\overline{\text{RAS}}$-only refresh mode, a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ automatic refresh is available. Another special feature of the MCM6256 is nibble mode, allowing the user to serially access 4 bits of data at a high data rate. Nibble mode address is controlled by the addresses on pin 1 (A8 row and A8 column).

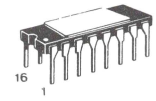
- Organized as 262,144 Words of 1 Bit
- Single +5 Volt Operation (±10%)
- Maximum Access Time:
  MCM6256-10 = 100 ns
  MCM6256-12 = 120 ns
  MCM6256-15 = 150 ns
- Low Power Dissipation:
  70 mA maximum (Active) MCM6256-10
  4 mA maximum (Standby)
- Three-State Data Output
- Early-Write Common I/O Capability
- 256 Cycle, 4 ms Refresh
- $\overline{\text{RAS}}$-Only Refresh Mode
- Automatic ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$) Refresh Mode
- Fast Nibble Mode on Read and Write Cycles
  20 ns Access Time
  40 ns Cycle Time


Spare Bits
A0
A1
A2
A3
A4
A5
A6
A7
Address Buffers and Counters
Memory Array
Decoder
Memory Array
Decoder
Decoder
Memory Array
Decoder
Memory Array
RAS Clocks
A8
Nibble Decoder
CAS Clocks I/O
A8
RAS
CAS
Write, W
Data In, D
Data Out, Q

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

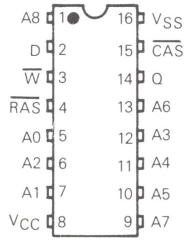
MOS
(N-CHANNEL, SILICON-GATE)

**262,144 BIT
DYNAMIC RANDOM ACCESS
MEMORY**



L SUFFIX
CERAMIC PACKAGE
CASE 690

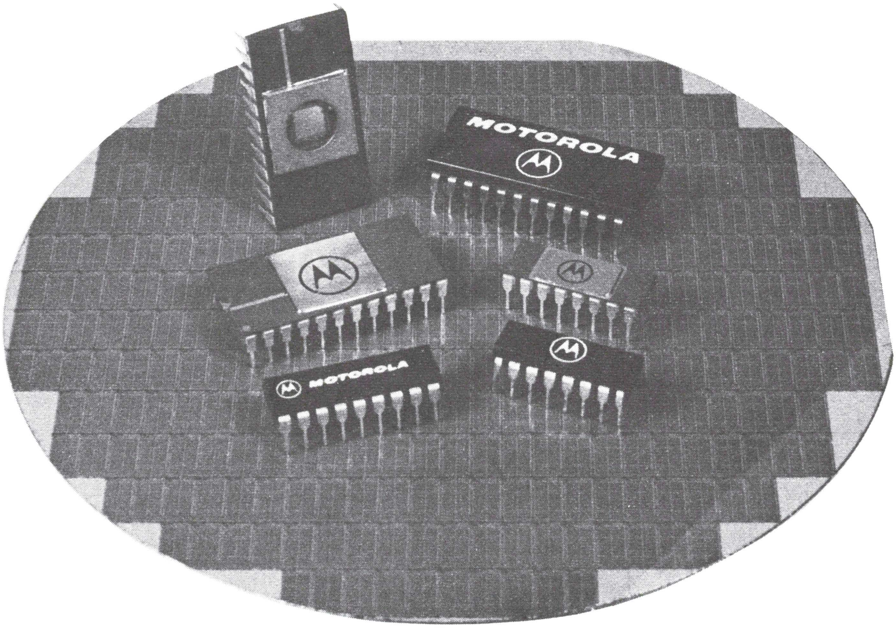
PIN ASSIGNMENT


A8 1
D 2
W 3
RAS 4
A0 5
A2 6
A1 7
VCC 8
16 VSS
15 CAS
14 Q
13 A6
12 A3
11 A4
10 A5
9 A7

PIN NAMES	
A0-A8	Address Input
D	Data In
Q	Data Out
$\overline{\text{W}}$	Read/Write Input
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
V_{CC}	Power (+5 V)
V_{SS}	Ground

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

MOS Static RAM


MOTOROLA
MOTOROLA

MOTOROLA

MCM2115A
MCM21L15A
MCM2125A
MCM21L25A

1024 × 1 STATIC RAM

The MCM2115A and MCM2125A families are high-speed, 1024 words by one-bit, random-access memories fabricated using HMOS, high-performance N-channel silicon-gate technology. Both open collector (MCM2115A) and three-state output (MCM2125A) are available. The devices use fully static circuitry throughout and require no clocks or timing strobes. Data out has the same polarity as the input data.

Access times are fully compatible with the industry-produced 1K Bipolar RAMs, yet offer up to 50% reduction in power over their Bipolar equivalents.

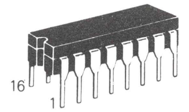
All inputs and output are directly TTL compatible. The chip select allows easy selection of an individual device when outputs are OR-tied.

- Organized as 1024 Words of 1 Bit
- Single +5 V Operation
- Maximum Access Time of 45 ns, 55 ns, and 70 ns available
- Low Operating Power Dissipation
- Pin Compatible to 93415A (2115A) and 93425A (2125A)
- TTL Inputs and Outputs
- Uncommitted Collector (2115A) and Three-State (2125A) Output

MOS

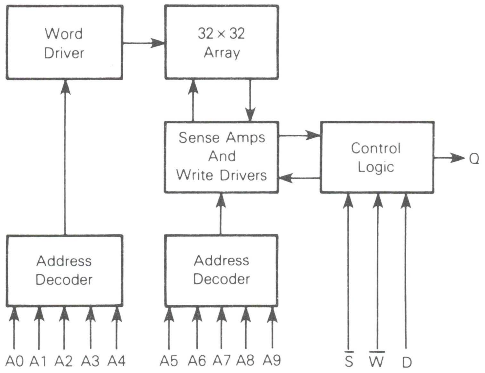
(N-CHANNEL, SILICON-GATE)

1024-BIT STATIC RANDOM ACCESS MEMORY

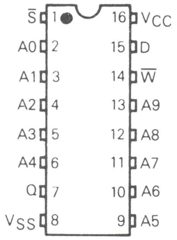


C SUFFIX
FRIT-SEAL
CERAMIC PACKAGE
CASE 620

BLOCK DIAGRAM


Word Driver
32 × 32 Array
Sense Amps And Write Drivers
Control Logic
Q
Address Decoder
Address Decoder
A0 A1 A2 A3 A4
A5 A6 A7 A8 A9
$\overline{S}$ $\overline{W}$ D

PIN ASSIGNMENT


$\overline{S}$ 1
A0 2
A1 3
A2 4
A3 5
A4 6
Q 7
V_{SS} 8
16 V_{CC}
15 D
14 $\overline{W}$
13 A9
12 A8
11 A7
10 A6
9 A5

TRUTH TABLE

Inputs			Output 2115A Family	Output 2125A Family	Mode
$\overline{S}$	$\overline{W}$	D	Q	Q	
H	X	X	H	High Z	Not Selected
L	L	L	H	High Z	Write "0"
L	L	H	H	High Z	Write "1"
L	H	X	Data Out	Data Out	Read

PIN NAMES

A	Address
D	Data Input
Q	Data Output
$\overline{S}$	Chip Select
V_{CC}	+5 V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Value	Unit
Temperature Under Bias	– 10 to + 80	°C
Voltage on Any Pin With Respect to V_{SS}	– 0.5 to + 7.0	Vdc
DC Output Current	20	mA
Power Dissipation	1.0	Watt
Operating Temperature Range	0 to + 70	°C
Storage Temperature Range	– 65 to + 150	°C

NOTE: Permanent damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC} V_{SS}	4.75 0	5.0 0	5.25 0	V
Logic 1 Voltage, All Inputs	V_{IH}	2.1	–	6	V
Logic 0 Voltage, All Inputs	V_{IL}	– 0.3	–	0.8	V

DC OPERATING CHARACTERISTICS

Parameter	Symbol	MCM2115A		MCM21L15A		MCM2125A		MCM21L25A		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Input Low Current (All Input Pins, $V_{in}=0$ to 5.5 V)	I_{IL}	–	– 40	–	– 40	–	– 40	–	– 40	μA
Input High Current	I_{IH}	–	40	–	40	–	40	–	40	μA
Output Leakage Current ($V_{out}=0.5/2.4$ V)	I_{OL}	–	–	–	–	–	50	–	50	μA
Output Leakage Current ($V_{out}=4.5$ V)	I_{CEX}	–	100	–	100	–	–	–	–	μA
Power Supply Current ($S=V_{IL}$, Outputs Open $T_A=25°C$)	ICC	–	125	–	75	–	125	–	75	mA
Output Low Voltage ($I_{OL}=7.0$ mA, 2125A, 16 mA 2115A)	VOL	–	0.45	–	0.45	–	0.45	–	0.45	V
Output High Voltage ($I_{OH}=-4.0$ mA)	VOH	–	–	–	–	2.4	–	2.4	–	V
Current Short Circuit to Ground	I_{OS}	–	–	–	–	–	– 100	–	– 100	mA

MCM2115A FAMILY AC OPERATING CONDITIONS AND CHARACTERISTICS, READ, WRITE CYCLES

($T_A=0$ to 70°C, $V_{CC}=5.0$ V ±5%)

Parameter	Symbol	MCM2115A-45		MCM2115A-55		MCM2115A-70		Units
		Min	Max	Min	Max	Min	Max	
Chip Select Low Output Valid	t_{SLQV}	5	30	5	35	5	40	ns
Chip Select High to Output Invalid	t_{SHQZ}	–	30	–	35	–	40	ns
Address Valid to Output Valid	t_{AVQV}	–	45	–	55	–	70	ns
Address Valid to Output Invalid	t_{AVQX}	10	–	10	–	10	–	ns
Write Low to Output Disable	t_{WLQZ}	–	30	–	35	–	40	ns
Write High to Output Valid	t_{WHQV}	0	30	0	35	0	45	ns
Write Low to Write High (Write Pulse Width)	t_{WLWH}	30	–	40	–	50	–	ns
Data Valid to Write Low	t_{DVWL}	5	–	5	–	5	–	ns
Write High to Data Don't Care (Data Hold)	t_{WHDX}	5	–	5	–	5	–	ns
Address Valid to Write Low (Address Setup)	t_{AVWL}	5	–	5	–	15	–	ns
Write High to Address Don't Care	t_{WHAX}	5	–	5	–	5	–	ns
Chip Select Low to Write Low	t_{SLWL}	5	–	5	–	5	–	ns
Write High to Chip Select High	t_{WHSH}	5	–	5	–	5	–	ns
Address Valid to Address Don't Care	t_{AVAX}	–	45	–	55	–	70	ns
Chip Select Low to Chip Select High	t_{SLSH}	–	45	–	55	–	70	ns

MCM21L15A FAMILY AC OPERATING CONDITIONS AND CHARACTERISTICS, READ, WRITE CYCLES

(T_A=0 to 70°C, V_{CC}=5.0 V ±5%)

Parameter	Symbol	MCM21L15A-45		MCM21L15A-70		Units
		Min	Max	Min	Max	
Chip Select Low to Output Valid	t_{SLQV}	5	30	5	30	ns
Chip Select High to Output Invalid	t_{SHQZ}	–	30	–	30	ns
Address Valid to Output Valid	t_{AVQV}	–	45	–	70	ns
Address Valid to Output Invalid	t_{AVQX}	10	–	10	–	ns
Write Low to Output Disable	t_{WLQZ}	–	25	–	25	ns
Write High to Output Valid	t_{WHQV}	0	25	0	25	ns
Write Low to Write High (Write Pulse Width)	t_{WLWH}	30	–	30	–	ns
Data Valid to Write Low	t_{DVWL}	0	–	0	–	ns
Write High to Data Don't Care	t_{WHDX}	5	–	5	–	ns
Address Valid to Write Low (Address Setup)	t_{AVWL}	5	–	5	–	ns
Write High to Address Don't Care	t_{WHAX}	5	–	5	–	ns
Chip Select Low to Write Low	t_{SLWL}	5	–	5	–	ns
Write High to Chip Select High	t_{WHSH}	5	–	5	–	ns
Address Valid to Address Don't Care	t_{AVAX}	–	45	–	70	ns
Chip Select Low to Chip Select High	t_{SLSH}	–	45	–	70	ns

MCM2125A FAMILY AC OPERATING CONDITIONS AND CHARACTERISTICS, READ, WRITE CYCLES

(T_A=0 to 70°C, V_{CC}=5.0 V ±5%)

Parameter	Symbol	MCM2125A-45		MCM2125A-55		MCM2125A-70		Units
		Min	Max	Min	Max	Min	Max	
Chip Select Low to Output Valid	t_{SLQV}	5	30	5	35	5	40	ns
Chip Select High to Output High Z	t_{SHQZ}	–	30	–	35	–	40	ns
Address Valid to Output Valid	t_{AVQV}	–	45	–	55	–	70	ns
Address Valid to Output Invalid	t_{AVQX}	10	–	10	–	10	–	ns
Write Low to Output High Z	t_{WLQZ}	–	30	–	35	–	40	ns
Write High to Output Valid	t_{WHQV}	0	30	0	35	0	45	ns
Write Low to Write High (Write Pulse Width)	t_{WLWH}	30	–	40	–	50	–	ns
Data Valid to Write Low	t_{DVWL}	5	–	5	–	5	–	ns
Write High to Data Don't Care	t_{WHDX}	5	–	5	–	5	–	ns
Address Valid to Write Low (Address Setup)	t_{AVWL}	5	–	5	–	15	–	ns
Write High to Address Don't Care	t_{WHAX}	5	–	5	–	5	–	ns
Chip Select Low to Write Low	t_{SLWL}	5	–	5	–	5	–	ns
Write High to Chip Select High	t_{WHSH}	5	–	5	–	5	–	ns
Address Valid to Address Don't Care	t_{AVAX}	–	45	–	55	–	70	ns
Chip Select Low to Chip Select High	t_{SLSH}	–	45	–	55	–	70	ns

MCM21L25A FAMILY AC OPERATING CONDITIONS AND CHARACTERISTICS, READ, WRITE CYCLES

(T_A=0 to 70°C, V_{CC}=5.0 V ±5%)

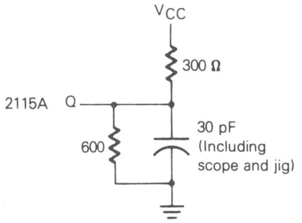
Parameter	Symbol	MCM21L25A-45		MCM21L25A-70		Units
		Min	Max	Min	Max	
Chip Select Low to Output Valid	t_{SLQV}	5	30	5	30	ns
Chip Select High to Output High Z	t_{SHQZ}	–	30	–	30	ns
Address Valid to Output Valid	t_{AVQV}	–	45	–	70	ns
Address Valid to Output Invalid	t_{AVQX}	10	–	10	–	ns
Write Low to Output High Z	t_{WLQZ}	–	25	–	25	ns
Write High to Output Valid	t_{WHQV}	0	25	0	25	ns
Write Low to Write High (Write Pulse Width)	t_{WLWH}	30	–	30	–	ns
Data Valid to Write Low	t_{DVWL}	0	–	0	–	ns
Write High to Data Don't Care	t_{WHDX}	5	–	5	–	ns
Address Valid to Write Low (Address Setup)	t_{AVWL}	5	–	5	–	ns
Write High to Address Don't Care	t_{WHAX}	5	–	5	–	ns
Chip Select Low to Write Low	t_{SLWL}	5	–	5	–	ns
Write High to Chip Select High	t_{WHSH}	5	–	5	–	ns
Address Valid to Address Don't Care	t_{AVAX}	–	45	–	70	ns
Chip Select Low to Chip Select High	t_{SLSH}	–	45	–	70	ns

CAPACITANCE (f = 1.0 MHz, $T_A = 25°C$, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Max	Unit
Input Capacitance ($V_{in} = 0$ V)	C_{in}	5	pF
Output Capacitance ($V_{out} = 0$ V)	C_{out}	8	pF

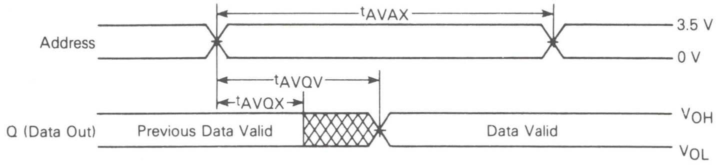
Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta_t/\Delta V$.

OUTPUT LOAD

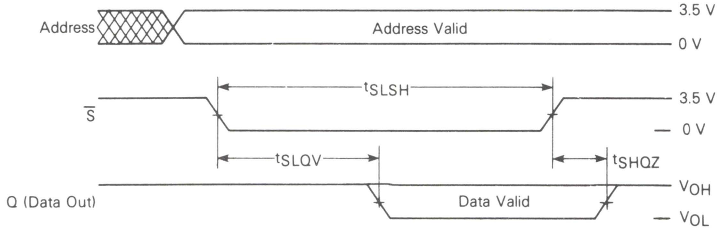

V_{CC}
300 Ω
2115A Q
600
30 pF
(Including
scope and jig)

2115A FAMILY

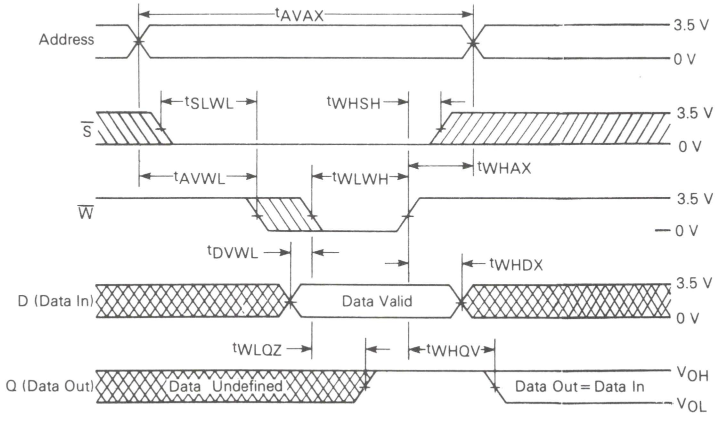
READ CYCLE TIMING 1
($\overline{S}$ Held Low, $\overline{W}$ Held High)


Address
t_{AVAX}
3.5 V
0 V
t_{AVQV}
t_{AVQX}
Q (Data Out)
Previous Data Valid
Data Valid
V_{OH}
V_{OL}

READ CYCLE TIMING 2'
($\overline{W}$ Held High)


Address
Address Valid
3.5 V
0 V
$\overline{S}$
t_{SLSH}
3.5 V
0 V
t_{SLQV}
t_{SHQZ}
Q (Data Out)
Data Valid
V_{OH}
V_{OL}

WRITE CYCLE TIMING

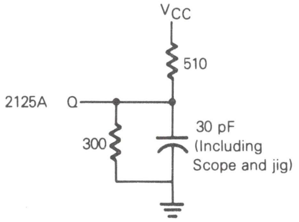

Address
t_{AVAX}
3.5 V
0 V
t_{SLWL}
t_{WHSH}
$\overline{S}$
3.5 V
0 V
t_{AVWL}
t_{WLWH}
t_{WHAX}
$\overline{W}$
3.5 V
0 V
t_{DVWL}
t_{WHDX}
D (Data In)
Data Valid
3.5 V
0 V
t_{WLQZ}
t_{WHQV}
Q (Data Out)
Data Undefined
Data Out = Data In
V_{OH}
V_{OL}

(All Time Measurements Referenced to 1.5 V)

WAVEFORMS

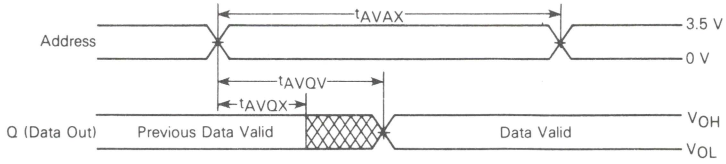
Waveform Symbol	Input	Output
═══	Must Be Valid	Will Be Valid
╲╲╲╲	Change From H to L	Will Change From H to L
╱╱╱╱	Change L to H	Will Change From L to H
XXXXXX	Don't Care: Any Change Permitted	Changing State Unknown
═> —	–	High Impedance

OUTPUT LOAD

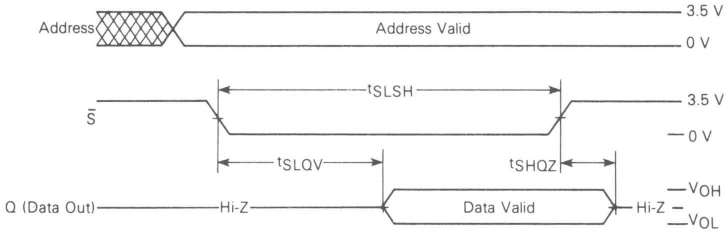

VCC
510
2125A Q
300
30 pF (Including Scope and jig)

2125A FAMILY

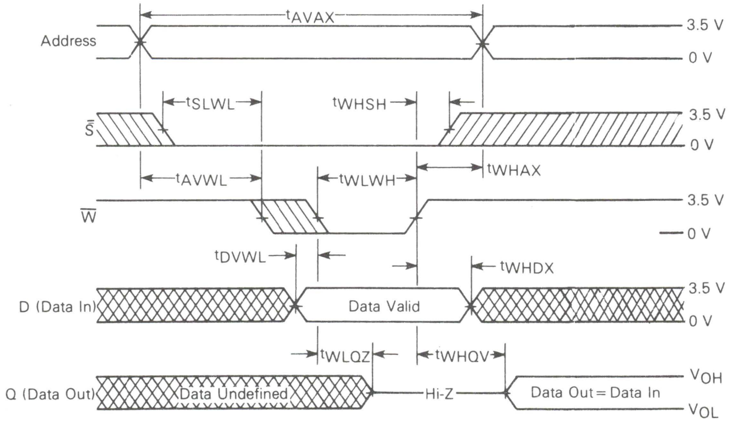
READ CYCLE TIMING 1
($\overline{S}$ Held Low, $\overline{W}$ Held High)


tAVAX
Address
3.5 V
0 V
tAVQV
tAVQX
Q (Data Out)
Previous Data Valid
Data Valid
VOH
VOL

READ CYCLE TIMING 2
($\overline{W}$ Held High)


Address
Address Valid
3.5 V
0 V
tSLSH
S̄
3.5 V
0 V
tSLQV
tSHQZ
Q (Data Out)
Hi-Z
Data Valid
Hi-Z
VOH
VOL

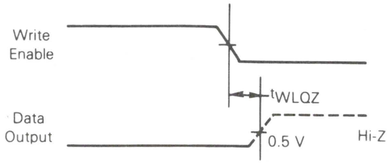
WRITE CYCLE TIMING


tAVAX
Address
3.5 V
0 V
tSLWL
tWHSH
S̄
3.5 V
0 V
tAVWL
tWLWH
tWHAX
W̄
3.5 V
0 V
tDVWL
tWHDX
D (Data In)
Data Valid
3.5 V
0 V
tWLQZ
tWHQV
Q (Data Out)
Data Undefined
Hi-Z
Data Out = Data In
VOH
VOL

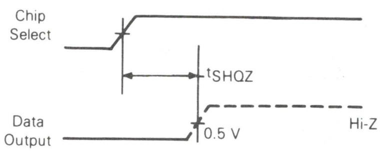
(All time measurements referenced to 1.5 V)

2115A FAMILY

WRITE ENABLE TO HIGH-Z DELAY

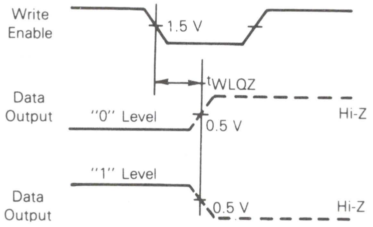

Write Enable
Data Output
tWLQZ
0.5 V
Hi-Z

PROPAGATION DELAY FROM CHIP SELECT TO HIGH-Z

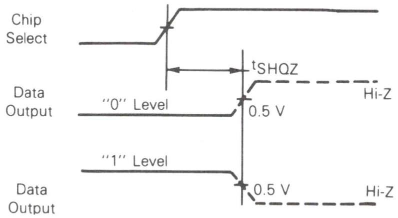

Chip Select
Data Output
tSHQZ
0.5 V
Hi-Z

2125A FAMILY

WRITE ENABLE TO HIGH-Z DELAY


Write Enable
1.5 V
tWLQZ
Data Output
"0" Level
0.5 V
Hi-Z
"1" Level
Data Output
0.5 V
Hi-Z

PROPAGATION DELAY FROM CHIP SELECT TO HIGH-Z


Chip Select
tSHQZ
Data Output
"0" Level
0.5 V
Hi-Z
"1" Level
Data Output
0.5 V
Hi-Z

MOTOROLA

MCM5101
MCM51L01

CMOS

(COMPLEMENTARY MOS)

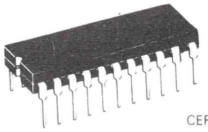
1024-BIT STATIC RANDOM ACCESS MEMORY

256 × 4 BIT STATIC RAM

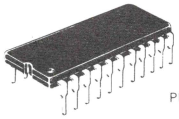
The MCM5101 family of CMOS RAMs offers ultra low power and fully static operation with a single 5-volt supply. The CMOS 1024-bit devices are organized in 256 words by 4 bits. Separate data inputs and data outputs permit maximum flexibility in bus-oriented systems. Data retention at a power supply as low as 2.0 volts over temperature readily allows design into applications using battery backup for nonvolatility. The MCM5101 is fully static and does not require clocking in standby mode.

The MCM5101 is fabricated using the Motorola advanced ion-implanted, silicon-gate technology for high performance and high reliability.

- Low Standby Power
- Fast Access Time
- Single +5.0 Volt Supply
- Fully TTL Compatible – All Inputs and Outputs
- Three-State Output
- Fully Static Operation
- Data Retention to 2.0 Volts
- Direct Replacement for:
  - Intel 5101 Series
  - AMI S5101 Series
  - Hitachi HM435101 Series
- Pin Replacement for Harris HM6501 Series



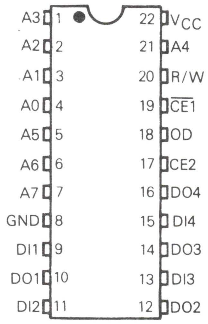
C SUFFIX
CERDIP PACKAGE
CASE 736



P SUFFIX
PLASTIC PACKAGE
CASE 708

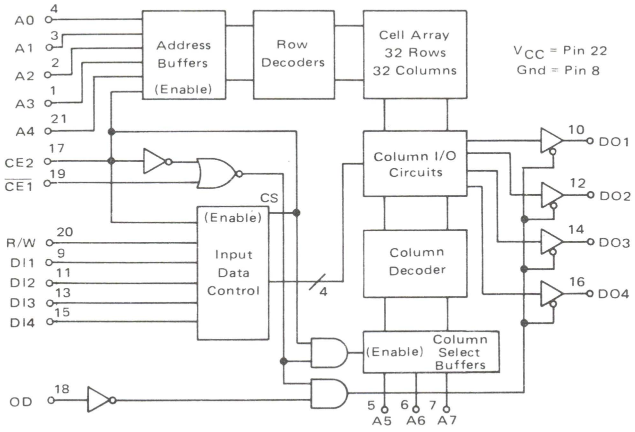
Type Number	Typical Current @2 V (μA)	Typical Current @ 5 V (μA)	Max Access (ns)
MCM51L01C45, P45	0.14	0.2	450
MCM51L01C65, P65	0.14	0.2	650
MCM5101C65, P65	0.70	1.0	650
MCM5101C80, P80	–	10	800

PIN ASSIGNMENT



A3 1
A2 2
A1 3
A0 4
A5 5
A6 6
A7 7
GND 8
DI1 9
DO1 10
DI2 11
22 V_{CC}
21 A4
20 R/W
19 $\overline{CE1}$
18 OD
17 CE2
16 DO4
15 DI4
14 DO3
13 DI3
12 DO2

BLOCK DIAGRAM



A0 4
A1 3
A2 2
A3 1
A4 21
CE2 17
$\overline{CE1}$ 19
R/W 20
DI1 9
DI2 11
DI3 13
DI4 15
OD 18
Address Buffers (Enable)
Row Decoders
Cell Array 32 Rows 32 Columns
V_{CC} = Pin 22
Gnd = Pin 8
Column I/O Circuits
CS
(Enable) Input Data Control
4
Column Decoder
(Enable) Column Select Buffers
5 6 7
A5 A6 A7
10 DO1
12 DO2
14 DO3
16 DO4

TRUTH TABLE

$\overline{CE1}$	CE2	OD	R/W	D_{in}	Output	Mode
H	X	X	X	X	High-Z	Not Selected
X	L	X	X	X	High-Z	Not Selected
X	X	H	H	X	High-Z	Output Disabled
L	H	H	L	X	High-Z	Write
L	H	L	L	X	D_{in}	Write
L	H	L	H	X	D_{out}	Read

DS9828/9-80

MAXIMUM RATINGS (Voltages referenced to V_{SS} Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage on Any Pin	V_{in}	−0.3 to V_{CC}+0.3	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC} V_{SS}	4.75 0	5.0 0	5.25 0	V
Logic 1 Voltage, All Inputs	V_{IH}	2.2	--	V_{CC}+0.3	V
Logic 0 Voltage, All Inputs	V_{IL}	−0.3	–	0.65	V

DC CHRACTERISTICS

Characteristic	Symbol	MCM51L01-45 MCM51L01-65			MCM5101-65			MCM5101-80			Unit
		Min	Typ(1)	Max	Min	Typ(1)	Max	Min	Typ(1)	Max	
Input Current	I_{in}(2)	–	5.0	–	–	5.0	–	–	5.0	–	nA
Input High Voltage	V_{IH}	2.2	–	V_{CC}+0.3	2.2	–	V_{CC}+0.3	2.2	–	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.3	–	0.65	−0.3	–	0.65	−0.3	–	0.65	V
Output High Voltage (I_{OH} = −1.0 mA)	V_{OH}	2.4	–	–	2.4	–	–	2.4	–	–	V
Output Low Voltage (I_{OL} = 2.0 mA)	V_{OL}	–	–	0.4	–	–	0.4	–	–	0.4	V
Output Leakage Current (CE1 = 2.2 V, V_{OL} = 0 V to V_{CC})	I_{LO}(2)	–	–	±1.0	–	–	±1.0	–	–	±2.0	μA
Operating Current (V_{in} = V_{CC}, except CE1 ≤ 0.65 V, outputs open)	I_{CC1}	–	9.0	22	–	9.0	22	–	11	25	mA
Operating Current (V_{in} = 2.2 V, Except CE1 ≤ 0.65 V, outputs open)	I_{CC2}	–	13	27	–	13	27	–	15	30	mA
Standby Current (CE2 ≤ 0.2 V, V_{in} = 0 V or V_{CC})	I_{CCL}(2)(4)	–	–	10	–	–	200	–	–	500	μA

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V periodically sampled rather than 100% tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (V_{in} = 0 V)	C_{in}	4.0	8.0	pF
Output Capacitance (V_{out} = 0 V)	C_{out}	8.0	12.0	pF

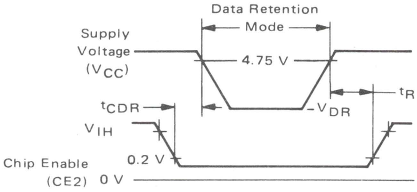
LOW V_{CC} DATA RETENTION CHARACTERISTICS (Excluding MCM5101-80)

Parameter	Test Conditions		Symbol	Min	Typ(1)	Max	Unit
V_{CC} for Data Retention	CE2 ≤ 0.2 V		V_{DR}	2.0	–	–	V
MCM51L01-45, -65 Data Retention Current		V_{DR} = 2.0 V	I_{CCDR1}	–	0.14	10	μA
MCM5101-65 Data Retention Current		V_{DR} = 2.0 V	I_{CCDR2}	–	0.70	200	μA
Chip Deselect to Data Retention Time			t_{CDR}	0	–	–	ns
Operation Recover Time			t_R	t_{RC}(3)	–	–	ns

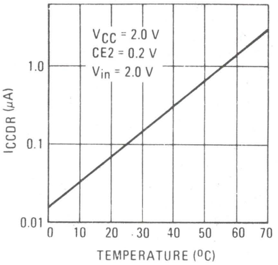
Notes:

1. Typical values are T_A = 25°C and nominal supply voltage
2. Current through all inputs and outputs included in I_{CCL} measurement
3. t_{RC} = Read Cycle Time
4. Low current state is for CE2 = 0 only

LOW V_{CC} DATA RETENTION WAVEFORM



TYPICAL I_{CCDR} vs TEMPERATURE



AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted)

Input Pulse Levels.. +0.65 V to 2.2 V
Input Rise and Fall Times...20 ns
Output Load................................. 1 TTL Gate and C_L = 100 pF
Timing Measurement Reference Level................................1.5 V

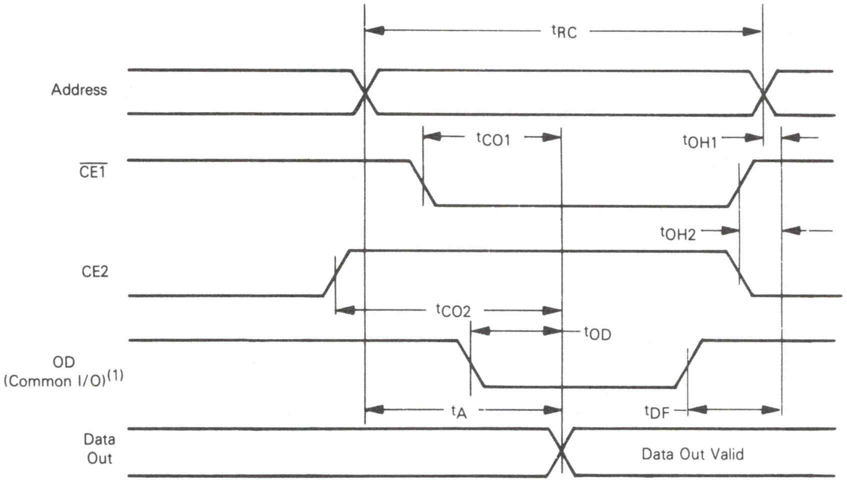
READ CYCLE

Parameter	Symbol	MCM51L01-45		MCM51L01-65 MCM5101-65		MCM5101-80		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle	t_{RC}	450	–	650	–	800	–	ns
Access Time	t_A	–	450	–	650	–	800	ns
Chip Enable ($\overline{CE1}$) to Output	t_{CO1}	–	400	–	600	–	800	ns
Chip Enable (CE2) to Output	t_{CO2}	–	500	–	700	–	850	ns
Output Disable to Output	t_{OD}	–	250	–	350	–	450	ns
Data Output to High-Z State	t_{DF}	0	130	0	150	0	200	ns
Previous Read Data Valid with Respect to Address Change	t_{OH1}	0	–	0	–	0	–	ns
Previous Read Data Valid with Respect to Chip Enable	t_{OH2}	0	–	0	–	0	–	ns

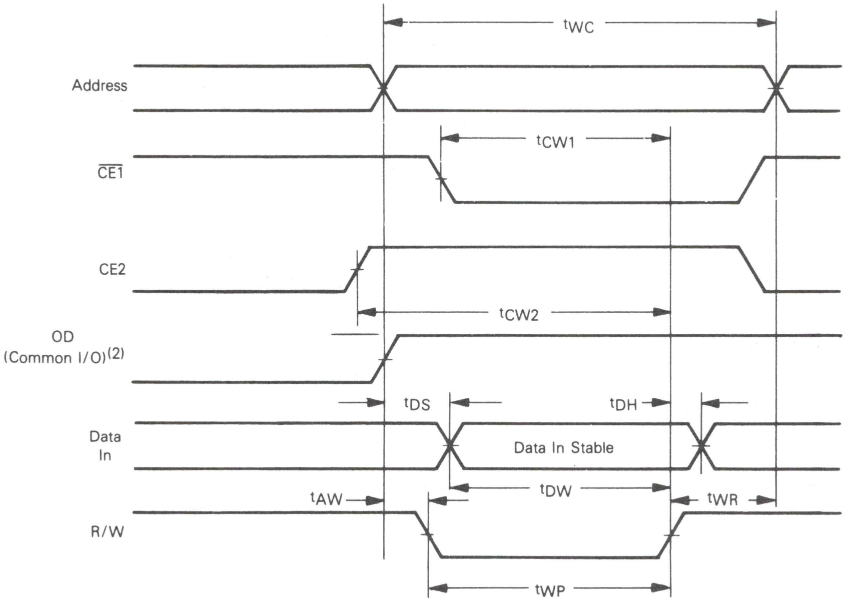
WRITE CYCLE

Parameter	Symbol	MCM51L01-45		MCM51L01-65 MCM5101-65		MCM5101-80		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle	t_{WC}	450	–	650	–	800	–	ns
Write Delay	t_{AW}	130	–	150	–	200	–	ns
Chip Enable ($\overline{CE1}$) to Write	t_{CW1}	350	–	550	–	650	–	ns
Chip Enable (CE2) to Write	t_{CW2}	350	–	550	–	650	–	ns
Data Setup	t_{DW}	250	–	400	–	450	–	ns
Data Hold	t_{DH}	50	–	100	–	100	–	ns
Write Pulse	t_{WP}	250	–	400	–	450	–	ns
Write Recovery	t_{WR}	50	–	50	–	100	–	ns
Output Disable Setup	t_{DS}	130	–	150	–	200	–	ns

READ CYCLE TIMING


t_{RC}
Address
t_{CO1}
t_{OH1}
$\overline{CE1}$
t_{OH2}
CE2
t_{CO2}
t_{OD}
OD
(Common I/O)(1)
t_A
t_{DF}
Data
Out
Data Out Valid

WRITE CYCLE TIMING


t_{WC}
Address
t_{CW1}
$\overline{CE1}$
CE2
t_{CW2}
OD
(Common I/O)(2)
t_{DS}
t_{DH}
Data
In
Data In Stable
t_{AW}
t_{DW}
t_{WR}
R/W
t_{WP}

Notes:
1. OD may be tied low for separate I/O operation
2. During the write cycle, OD is "high" for common I/O and "don't care" for separate I/O operation

MOTOROLA

MCM6810
(1.0 MHz)
MCM68A10
(1.5 MHz)
MCM68B10
(2.0 MHz)

MOS
(N-CHANNEL, SILICON-GATE)

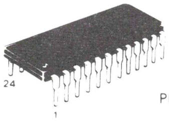
128 × 8-BIT STATIC
RANDOM ACCESS
MEMORY

128 × 8-BIT STATIC RANDOM ACCESS MEMORY

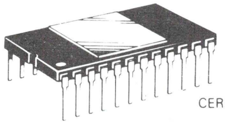
The MCM6810 is a byte-organized memory designed for use in bus-organized systems. It is fabricated with N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, has compatibility with TTL and DTL, and needs no clocks or refreshing because of static operation.

The memory is compatible with the M6800 Microcomputer Family, providing random storage in byte increments. Memory expansion is provided through multiple Chip Select inputs.

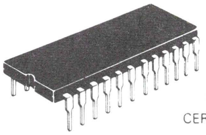
- Organized as 128 Bytes of 8 Bits
- Static Operation
- Bidirectional Three-State Data Input/Output
- Six Chip Select Inputs (Four Active Low, Two Active High)
- Single 5-Volt Power Supply
- TTL Compatible
- Maximum Access Time = 450 ns — MCM6810
  360 ns — MCM68A10
  250 ns — MCM68B10



P SUFFIX
PLASTIC PACKAGE
CASE 709

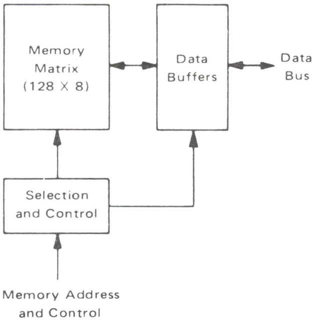


L SUFFIX
CERAMIC PACKAGE
CASE 716

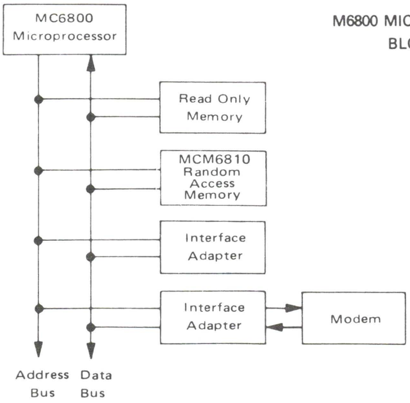


S SUFFIX
CERDIP PACKAGE
CASE 623

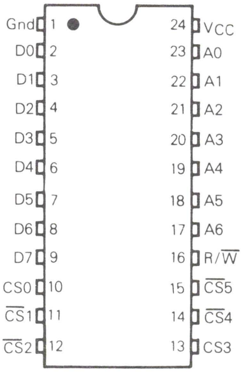
MCM6810 RANDOM ACCESS MEMORY BLOCK DIAGRAM


Memory
Matrix
(128 X 8)
Data
Buffers
Data
Bus
Selection
and Control
Memory Address
and Control

M6800 MICROCOMPUTER FAMILY BLOCK DIAGRAM


MC6800
Microprocessor
Read Only
Memory
MCM6810
Random
Access
Memory
Interface
Adapter
Interface
Adapter
Modem
Address
Bus
Data
Bus

PIN ASSIGNMENT


Gnd 1
D0 2
D1 3
D2 4
D3 5
D4 6
D5 7
D6 8
D7 9
CS0 10
$\overline{CS1}$ 11
$\overline{CS2}$ 12
24 VCC
23 A0
22 A1
21 A2
20 A3
19 A4
18 A5
17 A6
16 R/$\overline{W}$
15 $\overline{CS5}$
14 $\overline{CS4}$
13 CS3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature Range MCM6810, MCM68A10, MCM68B10 MCM6810C, MCM68A10C	T_A	T_L to T_H 0 to +70 −40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage (e.g., either V_{SS} or V_{CC}).

THERMAL CHARACTERISTICS

Characteristics	Symbol	Value	Unit
Thermal Resistance Ceramic Plastic Cerdip	θ_{JA}	 60 120 65	°C/W

POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \cdot \theta_{JA}) \qquad (1)$$

Where:

$T_A \equiv$ Ambient Temperature, °C

$\theta_{JA} \equiv$ Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D \equiv P_{INT} + P_{PORT}$

$P_{INT} \equiv I_{CC} \times V_{CC}$, Watts — Chip Internal Power

$P_{PORT} \equiv$ Port Power Dissipation, Watts — User Determined

For most applications $P_{PORT} \ll P_{INT}$ and can be neglected. P_{PORT} may become significant if the device is configured to drive Darlington bases or sink LED loads.

An approximate relationship between P_D and T_J (if P_{PORT} is neglected) is:

$$P_D = K \div (T_J + 273°C) \qquad (2)$$

Solving equations 1 and 2 for K gives:

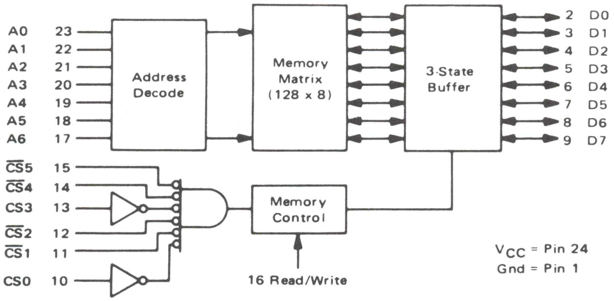
$$K = P_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D^2 \qquad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0, $T_A = T_L$ to T_H unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Input High Voltage	V_{IH}	$V_{SS}+2.0$	V_{CC}	V
Input Low Voltage	V_{IL}	$V_{SS}-0.3$	$V_{SS}+0.8$	V
Input Current (A_n, $R/\overline{W}$, $\overline{CS}_n$) (V_{in} = 0 to 5.25 V)	I_{in}	–	2.5	μA
Output High Voltage (I_{OH} = −205 μA)	V_{OH}	2.4	–	V
Output Low Voltage (I_{OL} = 1.6 mA)	V_{OL}	–	0.4	V
Output Leakage Current (Three-State) (CS = 0.8 V or $\overline{CS}$ = 2.0 V, V_{out} = 0.4 V to 2.4 V)	I_{TSI}	–	10	μA
Supply Current (V_{CC} = 5.25 V, All Other Pins Grounded) 1.0 MHz 1.5, 2.0 MHz	I_{CC}	– –	80 100	mA
Input Capacitance (A_n, $R/\overline{W}$, CS_n, $\overline{CS}_n$) (V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	C_{in}	–	7.5	pF
Output Capacitance (D_n) (V_{out} = 0, T_A = 25°C, f = 1.0 MHz, CSO = 0)	C_{out}	–	12.5	pF

BLOCK DIAGRAM

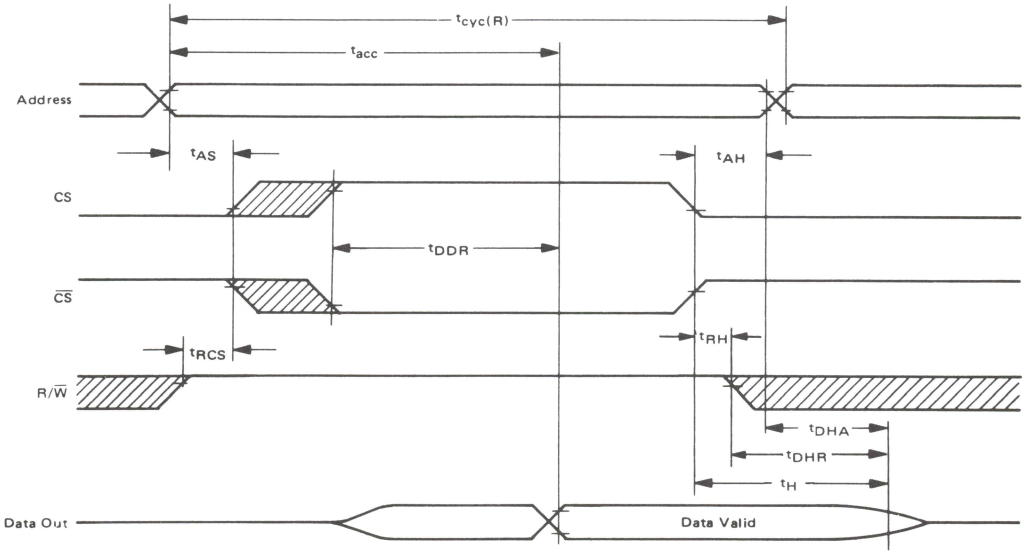

A0 23
A1 22
A2 21
A3 20
A4 19
A5 18
A6 17
Address Decode
Memory Matrix (128 x 8)
3-State Buffer
2 D0
3 D1
4 D2
5 D3
6 D4
7 D5
8 D6
9 D7
$\overline{CS}$5 15
$\overline{CS}$4 14
CS3 13
$\overline{CS}$2 12
$\overline{CS}$1 11
CS0 10
Memory Control
16 Read/Write
V_{CC} = Pin 24
Gnd = Pin 1

AC OPERATING CONDITIONS AND CHARACTERISTICS

READ CYCLE (V_{CC} = 5.0 V ±5%, V_{SS} = 0, T_A = T_L to T_H unless otherwise noted.)

Characteristic	Symbol	MCM6810		MCM68A10		MCM68B10		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	$t_{cyc(R)}$	450	–	360	–	250	–	ns
Access Time	t_{acc}	–	450	–	360	–	250	ns
Address Setup Time	t_{AS}	20	–	20	–	20	–	ns
Address Hold Time	t_{AH}	0	–	0	–	0	–	ns
Data Delay Time (Read)	t_{DDR}	–	230	–	220	–	180	ns
Read to Select Delay Time	t_{RCS}	0	–	0	–	0	–	ns
Data Hold from Address	t_{DHA}	10	–	10	–	10	–	ns
Output Hold Time	t_H	10	–	10	-	10	–	ns
Data Hold from Read	t_{DHR}	10	80	10	60	10	60	ns
Read Hold from Chip Select	t_{RH}	0	–	0	–	0	–	ns

READ CYCLE TIMING


$t_{cyc(R)}$
t_{acc}
Address
t_{AS}
t_{AH}
CS
t_{DDR}
$\overline{CS}$
t_{RH}
t_{RCS}
R/$\overline{W}$
t_{DHA}
t_{DHR}
t_H
Data Out
Data Valid

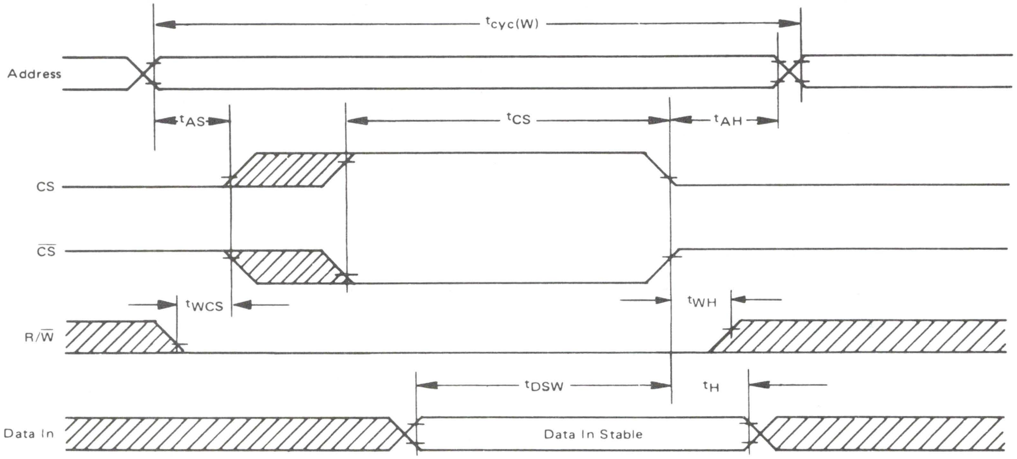
NOTES:
1. Voltage levels shown are $V_L \leq 0.4$ V, $V_H \geq 2.4$ V, unless otherwise specified.
2. Measurement points shown are 0.8 V and 2.0 V, unless otherwise specified.
3. CS and $\overline{CS}$ have same timing.

▨ = Don't Care

WRITE CYCLE (V_{CC} = 5.0 V ±5%, V_{SS} = 0, T_A = T_L to T_H unless otherwise noted.)

Characteristic	Symbol	MCM6810		MCM68A10		MCM68B10		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	$t_{cyc(W)}$	450	–	360	–	250	–	ns
Address Setup Time	t_{AS}	20	–	20	–	20	–	ns
Address Hold Time	t_{AH}	0	–	0	–	0	–	ns
Chip Select Pulse Width	t_{CS}	300	–	250	–	210	–	ns
Write to Chip Select Delay Time	t_{WCS}	0	–	0	–	0	–	ns
Data Setup Time (Write)	t_{DSW}	190	–	80	–	60	–	ns
Input Hold Time	t_H	10	–	10	–	10	–	ns
Write Hold Time from Chip Select	t_{WH}	0	–					

WRITE CYCLE TIMING

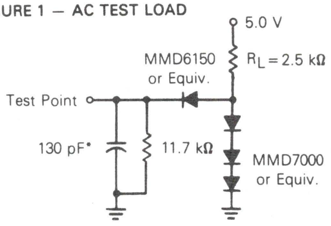

$t_{cyc(W)}$
Address
t_{AS}
t_{CS}
t_{AH}
CS
$\overline{CS}$
t_{WCS}
t_{WH}
R/$\overline{W}$
t_{DSW}
t_H
Data In
Data In Stable

NOTES:

1. Voltage levels shown are $V_L \leq 0.4$ V, $V_H \geq 2.4$ V, unless otherwise specified.
2. Measurement points shown are 0.8 V and 2.0 V, unless otherwise specified.
3. CS and $\overline{CS}$ have same timing.

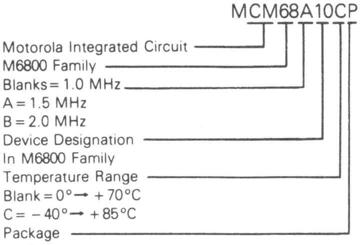
▨ = Don't Care

FIGURE 1 — AC TEST LOAD



*Includes Jig Capacitance

ORDERING INFORMATION



MCM68A10CP

Motorola Integrated Circuit
M6800 Family
Blanks = 1.0 MHz
A = 1.5 MHz
B = 2.0 MHz
Device Designation
In M6800 Family
Temperature Range
Blank = 0° → +70°C
C = −40° → +85°C
Package
P = Plastic
S = Cerdip
L = Ceramic

BETTER PROGRAM

Better program processing is available on all types listed. Add suffix letters to part number.

Level 1 add "S"   Level 2 add "D"   Level 3 add "DS"

Level 1 "S" = 10 Temp Cycles — (−25 to 150°C);
Hi Temp testing at T_A max.
Level 2 "D" = 168 Hour Burn-in at 125°C
Level 3 "DS" = Combination of Level 1 and 2.

Speed	Device	Temperature Range
1.0 MHz	MCM6810P,L,S MCM6810CP,CL,CS	0 to +70°C −40 to +85°C
1.5 MHz	MCM68A10P,L,S MCM68A10CP,CL,CS	0 to +70°C −40 to +85°C
2.0 MHz	MCM68B10P,L,S	0 to +70°C

MOTOROLA

MCM2114
MCM21L14

MOS

(N-CHANNEL, SILICON-GATE)

4096-BIT STATIC RANDOM ACCESS MEMORY

4096-BIT STATIC RANDOM ACCESS MEMORY

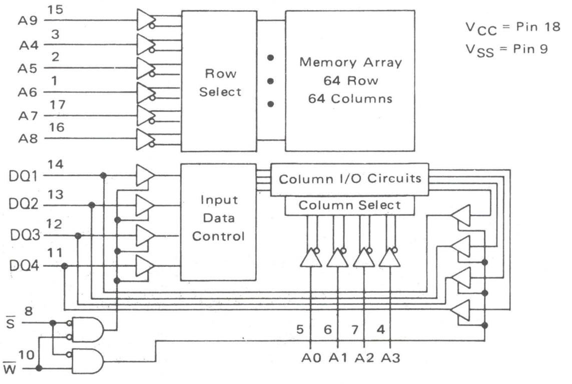
The MCM2114 is a 4096-bit random access memory fabricated with high density, high reliability N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, is directly compatible with TTL and DTL, and requires no clocks or refreshing because of fully static operation. Data access is particularly simple, since address setup times are not required. The output data has the same polarity as the input data.

The MCM2114 is designed for memory applications where simple interfacing is the design objective. The MCM2114 is assembled in 18-pin dual-in-line packages with the industry standard pin-out. A separate chip select ($\overline{S}$) lead allows easy selection of an individual package when the three-state outputs are OR-tied.

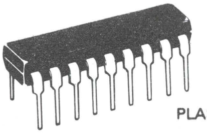
The MCM2114 series has a maximum current of 100 mA. Low power versions (i.e., MCM21L14 series) are available with a maximum current of only 70 mA.

- 1024 Words by 4-Bit Organization
- Industry Standard 18-Pin Configuration
- Single +5 Volt Supply
- No Clock or Timing Strobe Required
- Fully Static: Cycle Time = Access Time
- Maximum Access Time
  MCM2114-20/MCM21L14-20 200 ns
  MCM2114-25/MCM21L14-25 250 ns
  MCM2114-30/MCM21L14-30 300 ns
  MCM2114-45/MCM21L14-45 450 ns
- Fully TTL Compatible
- Common Data Input and Output
- Three-State Outputs for OR-Ties
- Low Power Version Available

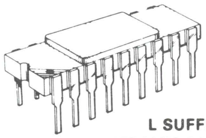
BLOCK DIAGRAM



A9 15
A4 3
A5 2
A6 1
A7 17
A8 16
Row Select
Memory Array 64 Row 64 Columns
V_{CC} = Pin 18
V_{SS} = Pin 9
DQ1 14
DQ2 13
DQ3 12
DQ4 11
Input Data Control
Column I/O Circuits
Column Select
$\overline{S}$ 8
$\overline{W}$ 10
5 6 7 4
A0 A1 A2 A3

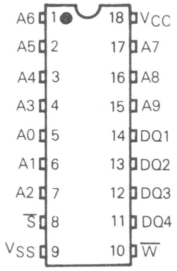


P SUFFIX
PLASTIC PACKAGE
CASE 707



L SUFFIX
CERAMIC PACKAGE
CASE 680

PIN ASSIGNMENT



A6 1
A5 2
A4 3
A3 4
A0 5
A1 6
A2 7
$\overline{S}$ 8
V_{SS} 9
18 V_{CC}
17 A7
16 A8
15 A9
14 DQ1
13 DQ2
12 DQ3
11 DQ4
10 $\overline{W}$

PIN NAMES	
A0-A9	Address Input
$\overline{W}$	Write Enable
$\overline{S}$	Chip Select
DQ1-DQ4	Data Input/Output
V_{CC}	Power (+5 V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Value	Unit
Temperature Under Bias	− 10 to + 80	°C
Voltage on Any Pin With Respect to V_{SS}	− 0.5 to + 7.0	V
DC Output Current	5.0	mA
Power Dissipation	1.0	Watt
Operating Temperature Range	0 to + 70	°C
Storage Temperature Range	− 65 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
	V_{SS}	0	0	0	
Logic 1 Voltage, All Inputs	V_{IH}	2.0	−	6.0	V
Logic 0 Voltage, All Inputs	V_{IL}	− 0.5	−	0.8	V

DC CHARACTERISTICS

Parameter	Symbol	MCM2114			MCM21L14			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Load Current (All Input Pins, $V_{in} = 0$ to 5.5 V)	I_{LI}	−	−	10	−	−	10	μA
I/O Leakage Current ($\overline{S} = 2.4$ V, $V_{DQ} = 0.4$ V to V_{CC})	$\lvert I_{LO} \rvert$	−	−	10	−	−	10	μA
Power Supply Current ($V_{in} = 5.5$ V, $I_{DQ} = 0$ mA, $T_A = 25°C$)	I_{CC1}	−	80	95	−	−	65	mA
Power Supply Current ($V_{in} = 5.5$ V, $I_{DQ} = 0$ mA, $T_A = 0°C$)	I_{CC2}	−	−	100	−	−	70	mA
Output Low Current $V_{OL} = 0.4$ V	I_{OL}	2.1	6.0	−	2.1	6.0	−	mA
Output High Current $V_{OH} = 2.4$ V	I_{OH}	−	− 1.4	− 1.0	−	− 1.4	− 1.0	mA

NOTE: Duration not to exceed 30 seconds.

CAPACITANCE ($f = 1.0$ MHz, $T_A = 25°C$, periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Input Capacitance ($V_{in} = 0$ V)	C_{in}	5.0	pF
Input/Output Capacitance ($V_{DQ} = 0$ V)	$C_{I/O}$	5.0	pF

Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta_t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted.)

Input Pulse Levels	0.8 Volt to 2.4 Volts	Input and Output Timing Levels	1.5 Volts
Input Rise and Fall Times	10 ns	Output Load	1 TTL Gate and $C_L = 100$ pF

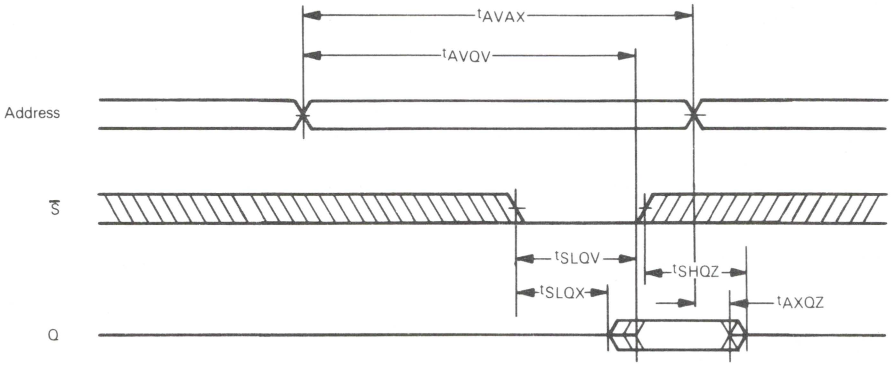
READ (NOTE 1), WRITE (NOTE 2) CYCLES

Parameter	Symbol	MCM2114-20 MCM21L14-20		MCM2114-25 MCM21L14-25		MCM2114-30 MCM21L14-30		MCM2114-45 MCM21L14-45		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Address Valid to Address Don't Care	t_{AVAX}	200	−	250	−	300	−	450	−	ns
Address Valid to Output Valid	t_{AVQV}	−	200	−	250	−	300	−	450	ns
Chip Select Low to Data Valid	t_{SLQV}	−	70	−	85	−	100	−	120	ns
Chip Select Low to Output Don't Care	t_{SLQX}	20	−	20	−	20	−	20	−	ns
Chip Select High to Output High Z	t_{SHQZ}	−	60	−	70	−	80	−	100	ns
Address Don't Care to Output High Z	t_{AXQZ}	50	−	50	−	50	−	50	−	ns
Write Low to Write High	t_{WLWH}	120	−	135	−	150	−	200	−	ns
Write High to Address Don't Care	t_{WHAX}	0	−	0	−	0	−	0	−	ns
Write Low to Output High Z	t_{WLQZ}	−	60	−	70	−	80	−	100	ns
Data Valid to Write High	t_{DVWH}	120	−	135	−	150	−	200	−	ns
Write High to Data Don't	t_{WHDX}	0	−	0	−	0	−	0	−	ns

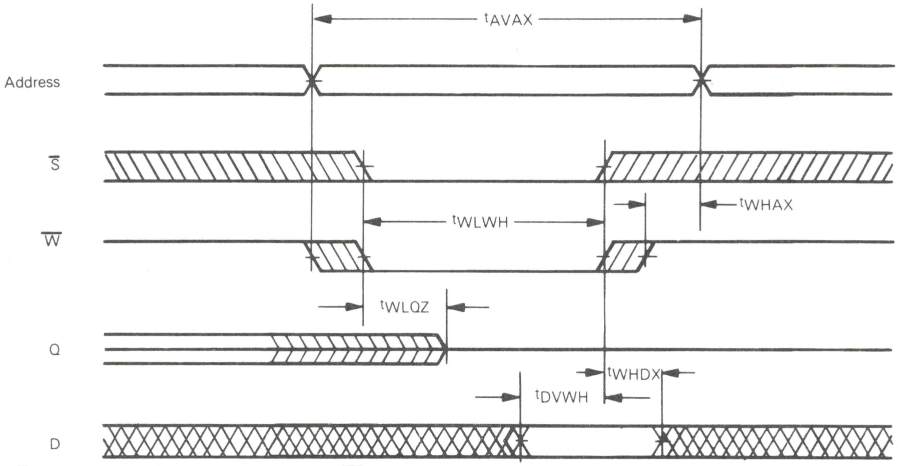
NOTES: 1. A Read occurs during the overlap of a low $\overline{S}$ and a high $\overline{W}$.

2. A Write occurs during the overlap of a low $\overline{S}$ and a low $\overline{W}$.

READ CYCLE TIMING ($\overline{W}$ HELD HIGH)


tAVAX
tAVQV
Address
S̄
tSLQV
tSHQZ
tSLQX
tAXQZ
Q

WRITE CYCLE TIMING (NOTE 3)


tAVAX
Address
S̄
tWHAX
tWLWH
W̄
tWLQZ
Q
tWHDX
tDVWH
D

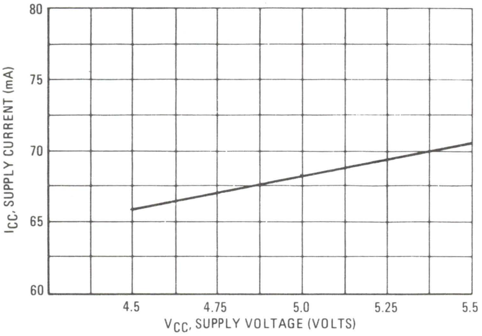
3. If the $\overline{S}$ low transition occurs simultaneously with the $\overline{W}$ low transition, the output buffers remain in a high-impedance state.

WAVEFORMS

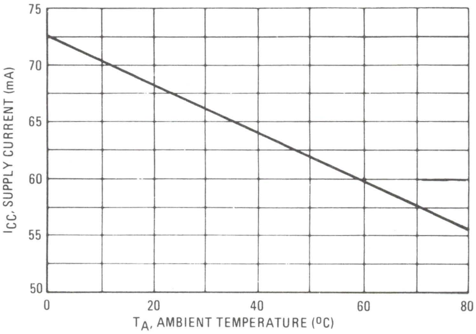
Waveform Symbol	Input	Output
═	MUST BE VALID	WILL BE VALID
▧	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
▨	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
⊠	DON'T CARE. ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
⟩	–	HIGH IMPEDANCE

TYPICAL CHARACTERISTICS

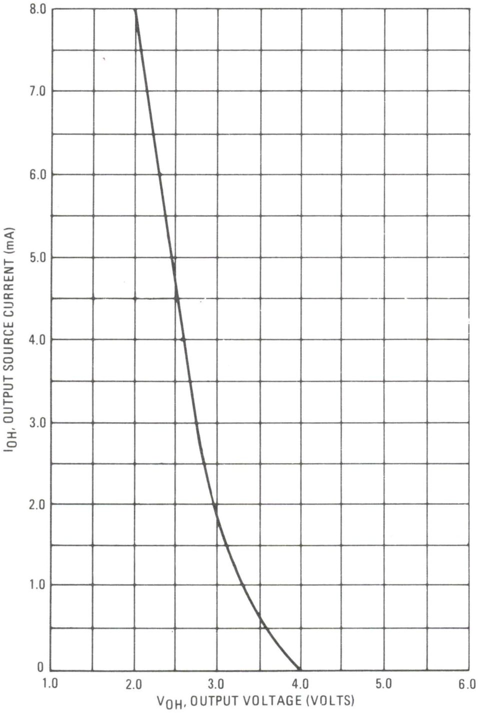
SUPPLY CURRENT versus SUPPLY VOLTAGE



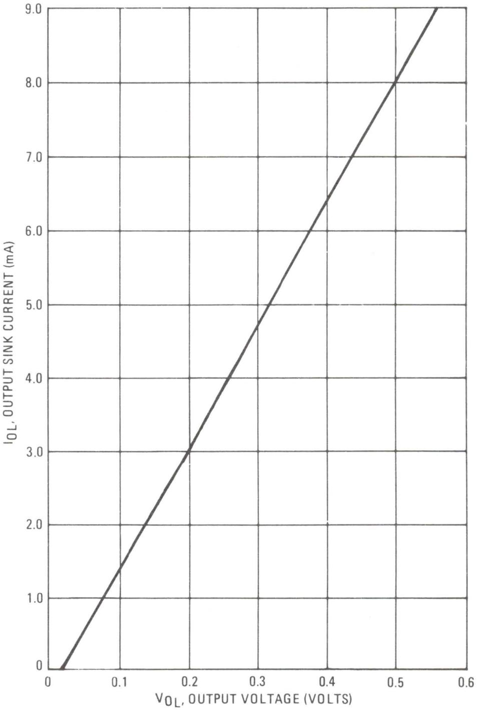
SUPPLY CURRENT versus AMBIENT TEMPERATURE



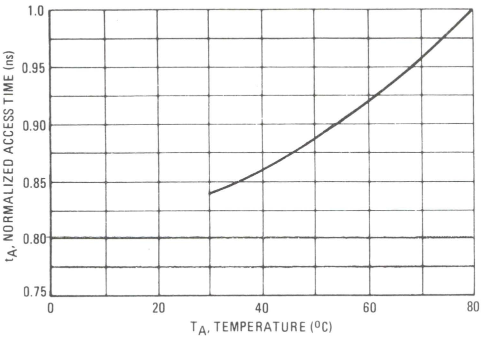
OUTPUT SOURCE CURRENT versus OUTPUT VOLTAGE



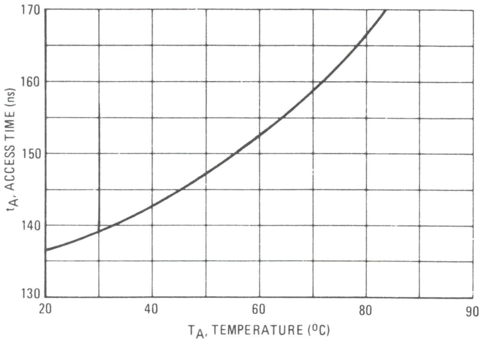
OUTPUT SINK CURRENT versus OUTPUT VOLTAGE



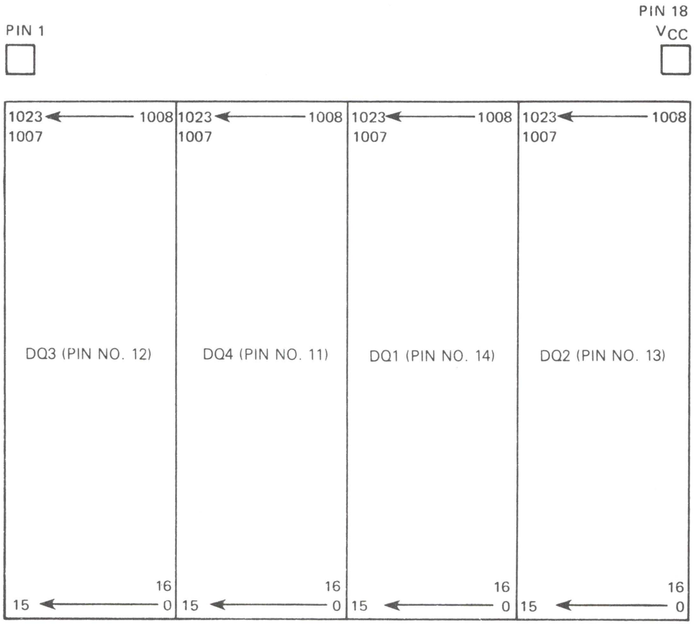
NORMALIZED ACCESS TIME versus TEMPERATURE



TYPICAL ACCESS TIME versus TEMPERATURE



MCM2114/MCM21L14 BIT MAP


PIN 1
PIN 18
VCC
1023
1008
1007
DQ3 (PIN NO. 12)
DQ4 (PIN NO. 11)
DQ1 (PIN NO. 14)
DQ2 (PIN NO. 13)
16
15
0

To determine the precise location on the die of a word in memory, reassign address numbers to the address pins as in the table below. The bit locations can then be determined directly from the bit map.

PIN NUMBER	REASSIGNED ADDRESS NUMBER
1	A6
2	A5
3	A4
4	A3
5	A0

PIN NUMBER	REASSIGNED ADDRESS NUMBER
6	A1
7	A2
15	$\overline{A9}$
16	$\overline{A8}$
17	$\overline{A7}$

MOTOROLA

MCM2147

4096-BIT STATIC RANDOM ACCESS MEMORY

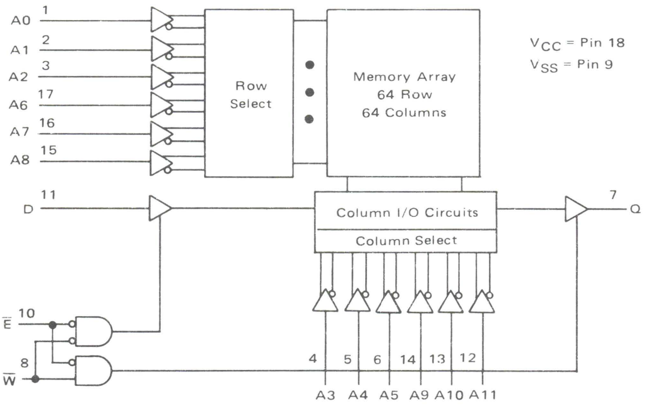
The MCM2147 is a 4096-bit static random access memory organized as 4096 words by 1-bit using Motorola's N-channel silicon-gate MOS technology. It uses a design approach which provides the simple timing features associated with fully static memories and the reduced standby power associated with semi-static and dynamic memories. This means low standby power without the need for clocks, nor reduced data rates due to cycle times that exceed access times.

$\overline{E}$ controls the power-down feature. It is not a clock but rather a chip select that affects power consumption. In less than a cycle time after $\overline{E}$ goes high, deselect mode, the part automatically reduces its power requirements and remains in this low-power standby mode as long as $\overline{E}$ remains high. This feature results in system power savings as great as 85% in larger systems, where most devices are deselected. The automatic power-down feature causes no performance degradation.

The MCM2147 is in an 18 pin dual in-line package with the industry standard pinout. It is TTL compatible in all respects. The data out has the same polarity as the input data. A data input and a separate three-state output provide flexibility and allow easy OR-ties.

- Fully Static Memory – No Clock or Timing Strobe Required
- Single +5 V Supply
- High Density 18 Pin Package
- Automatic Power-Down
- Directly TTL Compatible–All Inputs and Outputs
- Separate Data Input and Output
- Three-State Output
- Access Time – MCM2147-55 = 55 ns max
  MCM2147-70 = 70 ns max
  MCM2147-85 = 85 ns max
  MCM2147-100 = 100 ns max

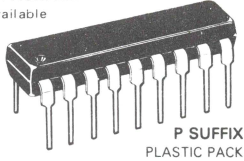
BLOCK DIAGRAM


A0 1
A1 2
A2 3
A6 17
A7 16
A8 15
Row Select
Memory Array
64 Row
64 Columns
V_{CC} = Pin 18
V_{SS} = Pin 9
D 11
Column I/O Circuits
Column Select
7 Q
$\overline{E}$ 10
$\overline{W}$ 8
4 5 6 14 13 12
A3 A4 A5 A9 A10 A11

MOS

(N-CHANNEL, SILICON-GATE)

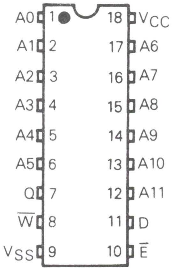
4096-BIT STATIC RANDOM ACCESS MEMORY



C SUFFIX
FRIT-SEAL
CERAMIC PACKAGE
also available

P SUFFIX
PLASTIC PACKAGE
CASE 707

PIN ASSIGNMENT


A0 1
A1 2
A2 3
A3 4
A4 5
A5 6
Q 7
$\overline{W}$ 8
V_{SS} 9
18 V_{CC}
17 A6
16 A7
15 A8
14 A9
13 A10
12 A11
11 D
10 $\overline{E}$

PIN NAMES

A0-A11	Address Input
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
D	Data Input
Q	Data Output
V_{CC}	Power (+5 V)
V_{SS}	Ground

TRUTH TABLE

$\overline{E}$	$\overline{W}$	Mode	Output	Power
H	X	Not Selected	High Z	Standby
L	L	Write	High Z	Active
L	H	Read	Data Out	Active

DS9821/10-80

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Value	Unit
Temperature Under Bias	-10 to +85	^{o}C
Voltage on Any Pin With Respect to V_{CC}	-0.5 to +7.0	Vdc
DC Output Current	20	mA
Power Dissipation	1.0	Watt
Operating Temperature Range	0 to +70	^{o}C
Storage Temperature Range	-65 to +150	^{o}C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC} V_{SS}	4.5 0	5.0 0	5.5 0	V
Logic 1 Voltage, All Inputs	V_{IH}	2.0	–	V_{CC}	V
Logic 0 Voltage, All Inputs	V_{IL}	–0.3	–	0.8	V

DC CHARACTERISTICS

Parameter	Symbol	MCM2147-55			MCM 2147-70			MCM2147-85			MCM2147-100			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Load Current (All Input Pins, V_{in} = 0 to 5.5 V)	I_{IL}	–	0.01	10	–	0.01	10	–	0.01	10	–	0.01	10	μA
Output Leakage Current ($\overline{E}$ = 2.0 V, V_{out} = 0 to 5.5 V)	I_{OL}	–	0.1	50	–	0.1	50	–	0.1	50	–	0.1	50	μA
Power Supply Current ($\overline{E}$ = V_{IL}, Outputs Open, T_A = 25°C)	I_{CC1}	–	120	170	–	100	150	–	95	130	–	90	110	mA
Power Supply Current ($\overline{E}$ = V_{IL}, Outputs Open, T_A = 0°C)	I_{CC2}	–	–	180	–	–	160	–	–	140	–	–	120	mA
Standby Current ($\overline{E}$ = V_{IH})	I_{SB}	–	15	30	–	10	20	–	15	25	–	10	20	mA
Input Low Voltage	V_{IL}	-0.3	–	0.8	-0.3	–	0.8	-0.3	–	0.8	-0.3	–	0.8	V
Input High Voltage	V_{IH}	2.0	–	6.0	2.0	–	6.0	2.0	–	6.0	2.0	–	6.0	V
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	–	–	0.4	–	–	0.4	–	–	0.4	–	–	0.4	V
Output High Voltage (I_{OH} = –4.0 mA)	V_{OH}	2.4	–	–	2.4	–	–	2.4	–	–	2.4	–	–	V

Typical values are for T_A = 25°C and V_{CC} = +5.0 V.

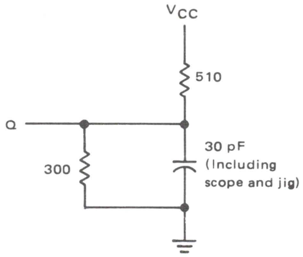
CAPACITANCE

(f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Max	Unit
Input Capacitance (V_{in} = 0 V)	C_{in}	5.0	pF
Output Capacitance (V_{out} = 0 V)	C_{out}	10	pF

Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = \frac{I\Delta_t}{\Delta V}$.

FIGURE 1 — OUTPUT LOAD



AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted)

Input Pulse Levels..0 Volt to 3.5 Volts
Input Rise and Fall Times..10 ns
Input and Output Timing Levels..................................1.5 Volts
Output Load..See Figure 1

READ, WRITE CYCLES

Parameter	Symbol	MCM2147-55		MCM2147-70		MCM2147-85		MCM2147-100		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Address Valid to Address Don't Care (Cycle Time When Chip Enable is Held Active)	t_{AVAX}	55	–	70	–	85	–	100	–	ns
Chip Enable Low to Chip Enable High	t_{ELEH}	55	–	70	–	85	–	100	–	ns
Address Valid to Output Valid (Access)	t_{AVQV}	–	55	–	70	–	85	–	100	ns
Chip Enable Low to Output Valid (Access)	t_{ELQV1}*	–	55	–	70	–	85	–	100	ns
	t_{ELQV2}*	–	65	–	80	–	95	–	110	ns
Address Valid to Output Invalid	t_{AVQX}	10	–	10	–	10	–	10	–	ns
Chip Enable Low to Output Invalid	t_{ELQX}	10	–	10	–	10	–	10	–	ns
Chip Enable High to Output High Z	t_{EHQZ}	0	40	0	40	0	40	0	40	ns
Chip Selection to Power-Up Time	t_{PU}	0	–	0	–	0	–	0	–	ns
Chip Deselection to Power-Down Time	t_{PD}	0	30	0	30	0	30	0	30	ns
Address Valid to Chip Enable Low (Address Setup)	t_{AVEL}	0	–	0	–	0	–	0	–	ns
Chip Enable Low to Write High	t_{ELWH}	45	–	55	–	70	–	80	–	ns
Address Valid to Write High	t_{AVWH}	45	–	55	–	70	–	80	–	ns
Address Valid to Write Low (Address Setup)	t_{AVWL}	0	–	0	–	0	–	0	–	ns
Write Low to Write High (Write Pulse Width)	t_{WLWH}	35	–	40	–	55	–	65	–	ns
Write High to Address Don't Care	t_{WHAX}	10	–	15	–	15	–	15	–	ns
Data Valid to Write High	t_{DVWH}	25	–	30	–	45	–	55	–	ns
Write High to Data Don't Care (Data Hold)	t_{WHDX}	10	–	10	–	10	–	10	–	ns
Write Low to Output High Z	t_{WLQZ}	0	30	0	35	0	45	0	50	ns
Write High to Output Valid	t_{WHQV}	0	–	0	–	0	–	0	–	ns

*t_{ELQV1} is access from chip enable when the 2147 is deselected for at least 55 ns prior to this cycle. t_{ELQV2} is access from chip enable for 0 ns < deselect time < 55 ns. If deselect time = 0 ns, then $t_{ELQV} = t_{AVQV}$.

TIMING PARAMETER ABBREVIATIONS

t X X X X

signal name from which interval is defined
transition direction for first signal
signal name to which interval is defined
transition direction for second signal

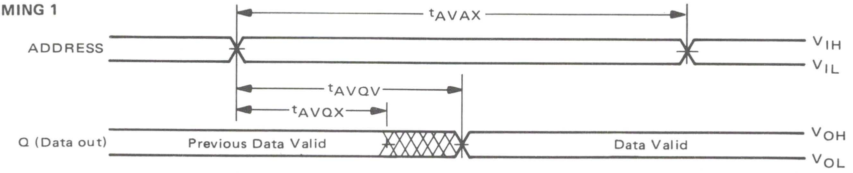
The transition definitions used in this data sheet are:

H = transition to high
L = transition to low
V = transition to valid
X = transition to invalid or don't care
Z = transition to off (high impedance)

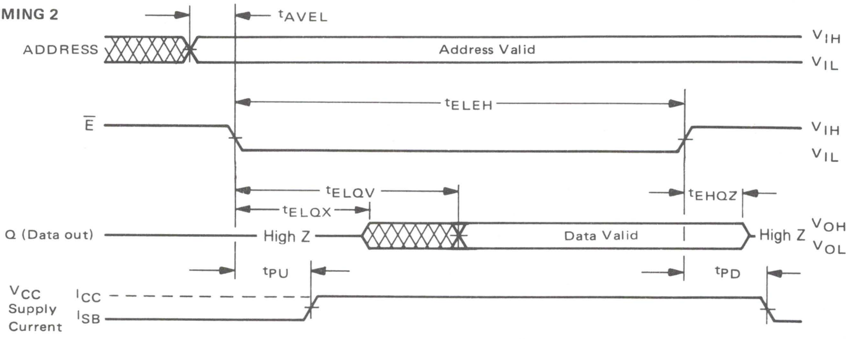
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE TIMING 1
($\overline{\text{E}}$ Held Low)

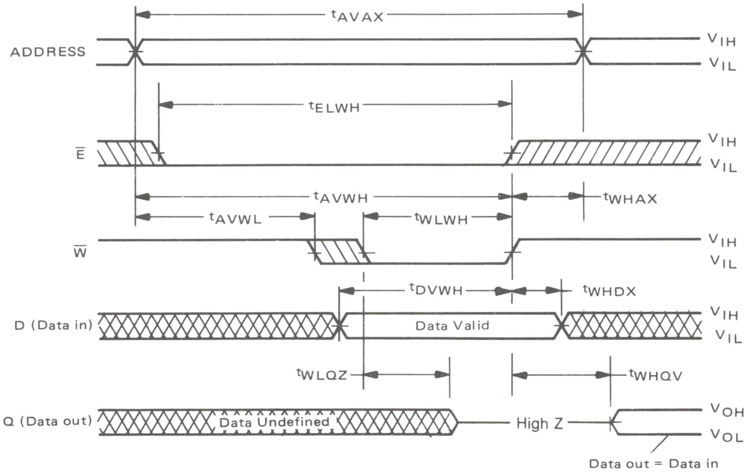

t_{AVAX}
ADDRESS
V_{IH}
V_{IL}
t_{AVQV}
t_{AVQX}
Q (Data out)
Previous Data Valid
Data Valid
V_{OH}
V_{OL}

READ CYCLE TIMING 2


t_{AVEL}
ADDRESS
Address Valid
V_{IH}
V_{IL}
$\overline{E}$
t_{ELEH}
V_{IH}
V_{IL}
t_{ELQV}
t_{ELQX}
t_{EHQZ}
Q (Data out)
High Z
Data Valid
High Z
V_{OH}
V_{OL}
t_{PU}
t_{PD}
V_{CC} Supply Current
I_{CC}
I_{SB}

NOTE: $\overline{W}$ is high for Read Cycles.

WRITE CYCLE TIMING


t_{AVAX}
ADDRESS
V_{IH}
V_{IL}
t_{ELWH}
$\overline{E}$
V_{IH}
V_{IL}
t_{AVWH}
t_{WHAX}
t_{AVWL}
t_{WLWH}
$\overline{W}$
V_{IH}
V_{IL}
t_{DVWH}
t_{WHDX}
D (Data in)
Data Valid
V_{IH}
V_{IL}
t_{WLQZ}
t_{WHQV}
Q (Data out)
Data Undefined
High Z
V_{OH}
V_{OL}
Data out = Data in

WAVEFORMS

Waveform Symbol	Input	Output
═	MUST BE VALID	WILL BE VALID
▥	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
▨	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
▩	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
⟩—	–	HIGH IMPEDANCE

DEVICE DESCRIPTION

The MCM2147 is produced with a high-performance MOS technology which combines on-chip substrate bias generation with device scaling to achieve high speed. The speed-power product of this process is about four times better than earlier MOS processes.

This gives the MCM2147 its high speed, low power and ease-of-use. The low-power standby feature is controlled with the $\overline{E}$ input. *$\overline{E}$ is not a clock and does not have to be cycled.* This allows the user to tie $\overline{E}$ directly to system addresses and use the line as part of the normal decoding logic. Whenever the MCM2147 is deselected, it automatically reduces its power requirements.

SYSTEM POWER SAVINGS

The automatic power-down feature adds up to significant system power savings. Unselected devices draw low standby power and only the active devices draw active power. Thus the average power consumed by a device declines as the system size increases, asymptotically approaching the standby power level as shown in Figure 2.

The automatic power-down feature is obtained without any performance degradation, since access time from chip enable is ⩽ access time from address valid. Also the fully static design gives access time equal cycle time so multiple read or write operations are possible during a single select period. The resultant data rates are 14.3 MHz and 18 MHz for the MCM2147-70 and MCM2147-55 respectively.

DECOUPLING AND BOARD LAYOUT CONSIDERATIONS

The power switching characteristic of the MCM2147 requires careful decoupling. It is recommended that a 0.1 μF to 0.3 μF ceramic capacitor be used on every other device, with a 22 μF to 47 μF bulk electrolytic decoupler every 16 devices. The actual values to be used will depend on board layout, trace widths and duty cycle.

Power supply gridding is recommended for PC board layout. A very satisfactory grid can be developed on a two-layer board with vertical traces on one side and horizontal traces on the other, as shown in Figure 3. If fast drivers are used, terminations are recommended on input signal lines to the MCM2147 because significant reflections are possible when driving their high impedance inputs. Terminations may be required to match the impedance of the line to the driver.

FIGURE 2 — AVERAGE DEVICE DISSIPATION versus MEMORY SIZE

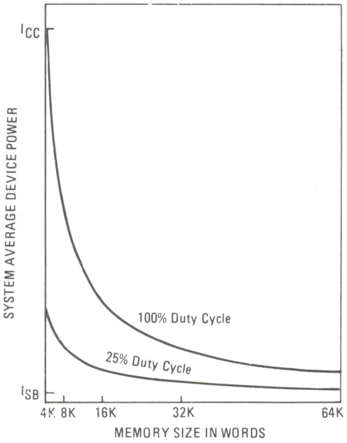
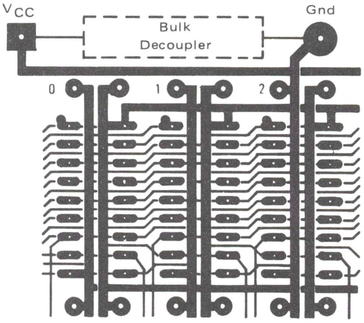


FIGURE 3 — PC LAYOUT



MOTOROLA

MCM65147

Advance Information

4096-BIT STATIC RANDOM ACCESS MEMORY

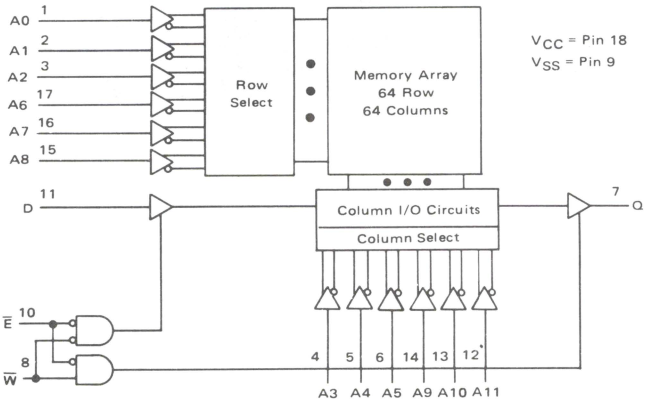
The MCM65147 is a 4096-bit static Random Access Memory organized as 4096 words by 1-bit, fabricated using Motorola's high performance CMOS silicon gate technology (HCMOS). It uses a design approach which provides the simple timing features associated with fully static memories and the reduced power associated with CMOS memories. This means low power without the need for clocks, nor reduced data rates due to cycle times that exceed access times.

Chip enable ($\overline{E}$) controls the power-down feature. It is not a clock, but rather a chip control that affects power consumption. After $\overline{E}$ goes high, initiating deselect mode, the part automatically reduces its power requirements and remains in this low-power standby mode as long as $\overline{E}$ remains high.

The MCM65147 is in an 18-pin dual in-line package with the industry standard pinout. It is TTL compatible in all respects. The data out has the same polarity as the input data. A data input and a separate three-state output provide flexibility and allow easy OR-ties.

- Single +5 V Supply
- Fully Static Memory — No Clock or Timing Strobe Required
- Maximum Access Time
    - MCM65147-55 = 55 ns
    - MCM65147-70 = 70 ns
- Automatic Power Down
- Low Power Dissipation
    - 75 mW Typical (Active)
    - 125 μW Typical (Standby)
- Low Standby Power Version Available
- Directly TTL Compatible — All Inputs and Output
- Separate Data Input and Three-State Output
- Equal Access and Cycle Time
- High Density 18-Pin Package

BLOCK DIAGRAM

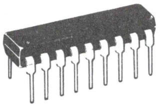


A0 1
A1 2
A2 3
A6 17
A7 16
A8 15
Row Select
Memory Array
64 Row
64 Columns
V_{CC} = Pin 18
V_{SS} = Pin 9
D 11
Column I/O Circuits
Column Select
7
Q
$\overline{E}$ 10
$\overline{W}$ 8
4 5 6 14 13 12
A3 A4 A5 A9 A10 A11

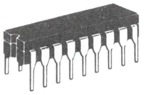
CMOS

(COMPLIMENTARY MOS)

4,096 × 1 BIT
STATIC RANDOM
ACCESS MEMORY

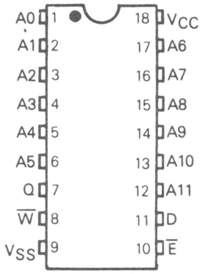


P SUFFIX
PLASTIC PACKAGE
CASE 707



C SUFFIX
FRIT-SEAL CERAMIC PACKAGE
CASE 726

PIN ASSIGNMENTS



A0 1
A1 2
A2 3
A3 4
A4 5
A5 6
Q 7
$\overline{W}$ 8
V_{SS} 9
18 V_{CC}
17 A6
16 A7
15 A8
14 A9
13 A10
12 A11
11 D
10 $\overline{E}$

PIN NAMES

A0-A11	Address
$\overline{E}$	Chip Enable
D	Data In
Q	Data Out
$\overline{W}$	Write
V_{CC}	Power (+5 V)
V_{SS}	Ground

Motorola reserves the right to make changes to any product herein to improve reliability, function or design. Motorola does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under its patent rights nor the rights of others.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS (See note)

Rating	Value	Unit
Temperature Under Bias	−10 to +85	°C
Voltage on Any Pin with Respect to V_{CC}	−0.5 to +7.0	V
Power Dissipation	1.0	Watt
Operating Temperature Range	0 to +70	°C
Storage Temperature Range	−65 to +150	°C

NOTE:

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC} V_{SS}	4.5 0	5.0 0	5.5 0	V
Logic 1 Voltage, All Inputs	V_{IH}	2.0	–	6.0	V
Logic 0, Voltage, All Inputs	V_{IL}	−0.3	–	0.8	V

DC CHARACTERISTICS

Parameter	Symbol	MCM65L147-55			MCM65147-55			MCM65L147-70			MCM65147-70			Unit
		Min	Typ*	Max	Min	Typ*	Max	Min	Typ*	Max	Min	Typ*	Max	
Input Load Current (All Input Pins, $V_{in}=0$ to 5.5 V)	I_{IL}	–	0.01	1.0	–	0.01	1.0	–	0.01	1.0	–	0.01	1.0	μA
Output Leakage Current ($\overline{E}=2.0$ V, $V_{out}=0$ to 5.5 V)	I_{OL}	–	0.1	1.0	–	0.1	1.0	–	0.1	1.0	–	0.1	1.0	μA
Power Supply Current ($\overline{E}=V_{IL}$, Output Open)	I_{CC1}	–	15	35	–	15	35	–	15	35	–	15	35	mA
Standby Current ($\overline{E}=V_{IH}$)	I_{SB1}	–	5	12	–	5	12	–	5	12	–	5	12	mA
Standby Current ($\overline{E}=V_{CC}-0.2$ V) ($0.2\text{ V}\geq V_{in}\geq V_{CC}-0.2$ V)	I_{SB2}	–	25	100	–	200	800	–	25	100	–	200	800	μA
Input Low Voltage	V_{IL}	−0.3	–	0.8	−0.3	–	0.8	−0.3	–	0.8	−0.3	–	0.8	V
Input High Voltage	V_{IH}	2.0	–	6.0	2.0	–	6.0	2.0	–	6.0	2.0	–	6.0	V
Output Low Voltage ($I_{OL}=12.0$ mA)	V_{OL}	–	–	0.4	–	–	0.4	–	–	0.4	–	–	0.4	V
Output High Voltage** ($I_{OH}=-8.0$ mA)	V_{OH}	2.4	–	–	2.4	–	–	2.4	–	–	2.4	–	–	V

*Typical values are for $T_A=25°C$ and $V_{CC}=+5.0$ V.

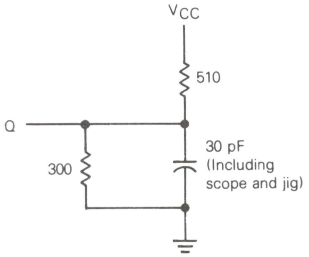
**Also, output voltages are compatible with Motorola's new High-Speed CMOS Logic Family, if the same power supply voltage is used.

CAPACITANCE (f = 1.0 MHz, $T_A=25°C$, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Max	Unit
Input Capacitance ($V_{in}=0$ V)	C_{in}	5.0	pF
Output Capacitance ($V_{out}=0$ V)	C_{out}	7.0	pF

Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C=I\Delta_t/\Delta V$.

FIGURE 1 — OUTPUT LOAD



AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted)

Input Pulse Levels	0 Volt to 3.5 Volts	Input and Output Timing Levels	0.8 and 2.0 Volts
Input Rise and Fall Times	10 ns	Output Load	See Figure 1

READ, WRITE CYCLES

Parameter	Symbol	MCM65147-55		MCM65147-70		Unit
		Min	Max	Min	Max	
Address Valid to Address Don't Care (Cycle Time when Chip Enable is Held Active)	t_{AVAX}	55	–	70	–	ns
Chip Enable Low to Chip Enable High	t_{ELEH}	55	–	70	–	ns
Address Valid to Output Valid (Access)	t_{AVQV}	–	55	–	70	ns
Chip Enable Low to Output Valid (Access)	t_{ELQV}	–	55	–	70	ns
Address Valid to Output Invalid	t_{AVQX}	5	–	5	–	ns
Chip Enable Low to Output Invalid	t_{ELQX}	10	–	10	–	ns
Chip Enable High to Output High Z	t_{EHQZ}	0	40	0	40	ns
Chip Selection to Power-Up Time	t_{PU}	0	–	0	–	ns
Chip Deselection to Power-Down Time	t_{PD}	0	30	0	30	ns
Address Valid to Chip Enable Low (Address Setup)	t_{AVEL}	0	–	0	–	ns
Chip Enable Low to Write High	t_{ELWH}	45	–	55	–	ns
Address Valid to Write High	t_{AVWH}	45	–	55	–	ns
Address Valid to Write Low (Address Setup)	t_{AVWL}	0	–	0	–	ns
Write Low to Write High (Write Pulse Width)	t_{WLWH}	35	–	40	–	ns
Write High to Address Don't Care	t_{WHAX}	10	–	15	–	ns
Data Valid to Write High	t_{DVWH}	25	–	30	–	ns
Write High to Data Don't Care (Data Hold)	t_{WHDX}	10	–	10	–	ns
Write Low to Output High Z	t_{WLQZ}	0	30	0	35	ns
Write High to Output Valid	t_{WHQV}	0	–	0	–	ns

TIMING PARAMETER ABBREVIATIONS

```
                                          t X X X X
   signal name from which interval is defined ┘ │ │ │
         transition direction for first signal ──┘ │ │
      signal name to which interval is defined ────┘ │
       transition direction for second signal ───────┘
```

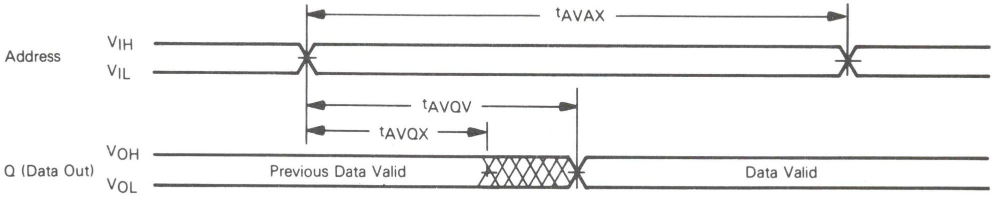
The transition definitions used in this data sheet are:

H = transition to high
L = transition to low
V = transition to valid
X = transition to invalid or don't care
Z = transition to off (high impedance)

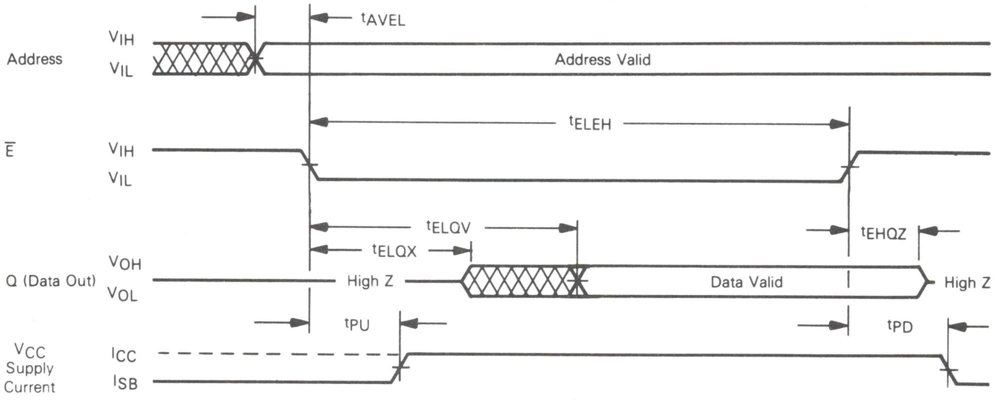
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE TIMING 1
($\overline{E}$ Held Low)

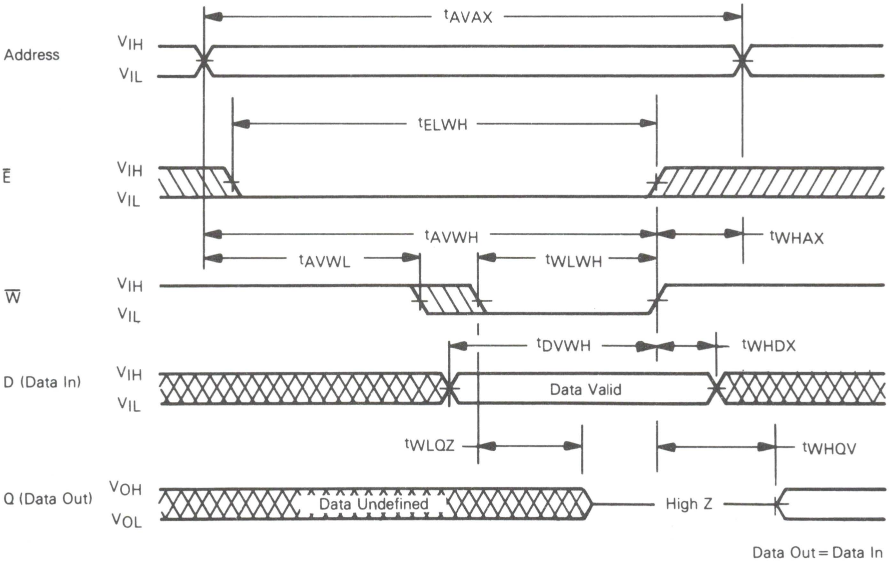

tAVAX
Address
VIH
VIL
tAVQV
tAVQX
Q (Data Out)
VOH
VOL
Previous Data Valid
Data Valid

READ CYCLE TIMING 2


tAVEL
Address
VIH
VIL
Address Valid
tELEH
Ē
VIH
VIL
tELQV
tELQX
tEHQZ
Q (Data Out)
VOH
VOL
High Z
Data Valid
High Z
tPU
tPD
VCC
Supply
Current
ICC
ISB

NOTE: $\overline{W}$ is high for Read Cycles

WRITE CYCLE TIMING


tAVAX
Address
VIH
VIL
tELWH
Ē
VIH
VIL
tAVWH
tWHAX
tAVWL
tWLWH
W̄
VIH
VIL
tDVWH
tWHDX
D (Data In)
VIH
VIL
Data Valid
tWLQZ
tWHQV
Q (Data Out)
VOH
VOL
Data Undefined
High Z
Data Out = Data In

MOTOROLA

MCM6641
MCM66L41

Advance Information

4096-BIT STATIC RANDOM ACCESS MEMORIES

The MCM6641 series 4096 × 1-bit Random Access Memory is fabricated with high density, high reliability N-channel silicon-gate technology. For ease of use, the device operates from a single 5-volt power supply, is directly compatible with TTL and DTL, and requires no clocks or refreshing because of fully static operation. The fully static operation allows chip selects to be tied low, further simplifying system timing. Data access is particularly simple, since address setup times are not required. The output data has the same polarity as the data input.

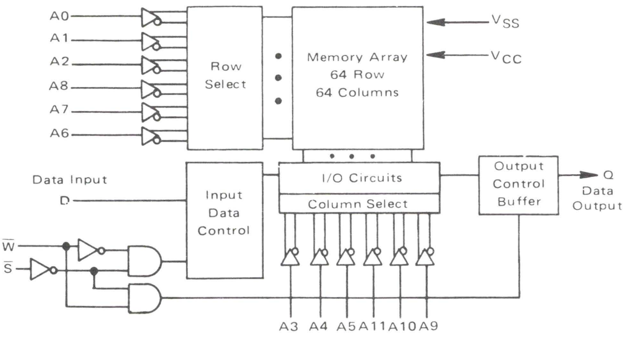
The MCM6641 is designed for memory applications where simple interfacing is the design objective, and is assembled in 18-pin dual-in-line packages with the industry standard pin-outs.

- Single ± 10% + 5 V Supply
- Fully Static Operation — No Clock, Timing Strobe, Pre-Charge, or Refresh Required
- Industry Standard 18-Pin Configuration
- Fully TTL Compatible
- Common Data Input and Output Capability
- Three-State Outputs for OR-Tie Capability
- Power Dissipation MCM6641 Less Than 550 mW (Maximum)
  MCM66L41 Less Than 385 mW (Maximum)
- Standby Power Dissipation Less Than 125 mW (Typical)
- Plug-In Replacement For TMS4044

MAXIMUM ACCESS TIME/MINIMUM CYCLE TIME

MCM6641-20 MCM66L41-20	200 ns	MCM6641-30 MCM66L41-30	300 ns
MCM6641-25 MCM66L41-25	250 ns	MCM6641-45 MCM66L41-45	450 ns

BLOCK DIAGRAM

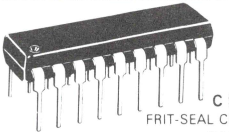

A0
A1
A2
A8
A7
A6
Row Select
Memory Array
64 Row
64 Columns
V_{SS}
V_{CC}
I/O Circuits
Column Select
Output Control Buffer
Q
Data Output
Data Input
D
Input Data Control
$\overline{W}$
$\overline{S}$
A3 A4 A5 A11 A10 A9

This document contains information on a new product. Specifications and information herein are subject to change without notice.

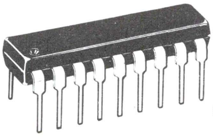
MOS

(N-CHANNEL, SILICON-GATE)

4096-BIT STATIC
RANDOM ACCESS MEMORIES

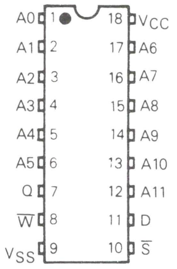


C SUFFIX
FRIT-SEAL CERAMIC PACKAGE
CASE 707-01



P SUFFIX
PLASTIC PACKAGE
CASE 707

PIN ASSIGNMENT


A0 1
A1 2
A2 3
A3 4
A4 5
A5 6
Q 7
$\overline{W}$ 8
V_{SS} 9
18 V_{CC}
17 A6
16 A7
15 A8
14 A9
13 A10
12 A11
11 D
10 $\overline{S}$

PIN NAMES	
A0-A11	Address Input
D	Data Input
Q	Data Output
$\overline{S}$	Chip Select
V_{CC}	Power Supply (+5 V)
V_{SS}	Ground
$\overline{W}$	Write Enable

TRUTH TABLE

$\overline{S}$	$\overline{W}$	D	Q	Mode
H	X	X	High Z	Not Selected
L	L	L	High Z	Write "0"
L	L	H	High Z	Write "1"
L	H	X	Output data	Read

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Value	Unit
Temperature Under Bias	-10 to +80	°C
Voltage on Any Pin With Respect to V_{SS}	-0.5 to +7.0	Vdc
DC Output Current	20	mA
Power Dissipation	1.0	Watt
Operating Temperature Range	0 to +70	°C
Storage Temperature Range	-65 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC} V_{SS}	4.5 0	5.0 0	5.5 0	V
Logic 1 Voltage, All Inputs	V_{IH}	2.0	–	6.0	V
Logic 0 Voltage, All Inputs	V_{IL}	−0.5	–	0.8	V

DC CHARACTERISTICS

Parameter	Symbol	MCM6641			MCM66L41			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Load Current (All Input Pins, $V_{in}=0$ to 5.5 V)	I_{LI}	–	–	10	–	–	10	μA
Output Leakage Current (CS = 2.4 V, $V_{in}=0.4$ to V_{CC})	$\lvert I_{LO}\rvert$	–	–	10	–	–	10	μA
Power Supply Current ($V_{CC}=5.5$ V, $I_{out}=0$ mA, $T_A=0°C$)	I_{CC}	–	80	100	–	55	70	mA
Output Low Voltage, $I_{OL}=2.1$ mA	V_{OL}	–	0.15	0.4	–	0.15	0.4	V
Output High Voltage, $I_{OH}=1.0$ mA	V_{OH}	2.4	–	–	2.4	–	–	V
Output Short Circuit Current	I_{OS}*	–	–	40	–	–	40	mA

*Duration not to exceed 30 seconds.

CAPACITANCE (f = 1.0 MHz, $T_A=25°C$, $V_{CC}=5.0$ V, periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Input Capacitance ($V_{in}=0$ V)	C_{in}	5.0	pF
Output Capacitance ($V_{out}=0$ V)	C_{out}	10	pF

Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C=I\Delta_t/\Delta V$.

STANDBY OPERATION

(Typical Supply Values)

Device	Supply	Operating	Standby	Max Standby Power
MCM6641	V_{CC}	+5 V	+2.4 V	225 mW
MCM66L41	V_{CC}	+5 V	+2.4 V	150 mW

AC OPERATING CONDITIONS AND CHARACTERISTICS

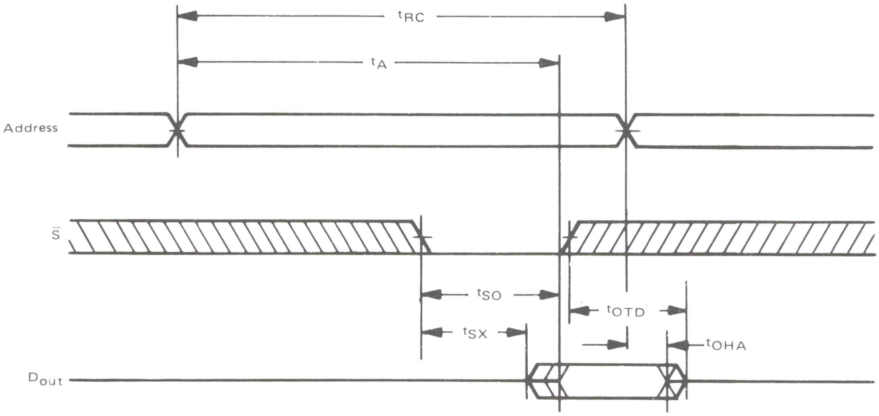
(Full operating voltage and temperature range unless otherwise noted)

Input Pulse Levels......................................0.8 Volt to 2.0 Volts
Input Rise and Fall Times..10 ns
Input and Output Timing Levels..................................1.5 Volts
Output Load...................................1 TTL Gate and $C_L = 100$ pF

READ (NOTE 1), WRITE (NOTE 2) CYCLES

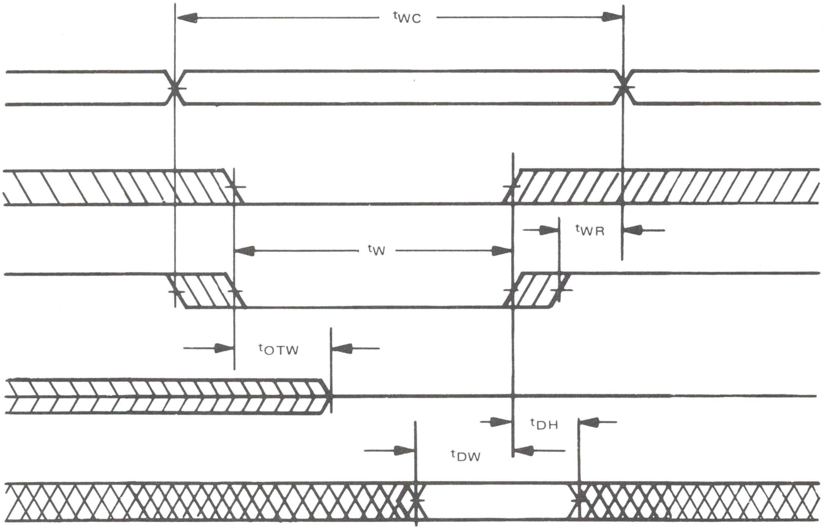
Parameter	Symbol	MCM6641-20 MCM66L41-20		MCM6641-25 MCM66L41-25		MCM6641-30 MCM66L41-30		MCM6641-45 MCM66L41-45		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	200	—	250	—	300	—	450	—	ns
Access Time	t_A	—	200	—	250	—	300	—	450	ns
Chip Selection to Output Valid	t_{SO}	—	70	—	85	—	100	—	120	ns
Chip Selection to Output Active	t_{SX}	10	—	10	—	10	—	10	—	ns
Output 3-State From Deselection	t_{OTD}	—	40	—	60	—	80	—	100	ns
Output Hold From Address Change	t_{OHA}	50	—	50	—	50	—	50	—	ns
Write Cycle Time	t_{WC}	200	—	250	—	300	—	450	—	ns
Write Time	t_W	100	—	125	—	150	—	200	—	ns
Write Release Time	t_{WR}	0	—	0	—	0	—	0	—	ns
Output 3-State From Write	t_{OTW}	—	40	—	60	—	80	—	100	ns
Data to Write Time Overlap	t_{DW}	100	—	125	—	150	—	200	—	ns
Data Hold From Write Time	t_{DH}	0	—	0	—	0	—	0	—	ns

READ CYCLE TIMING
($\overline{W}$ HELD HIGH)



NOTES:
1. A Read occurs during the overlap of a low $\overline{S}$ and a high $\overline{W}$.
2. A Write occurs during the overlap of a low $\overline{S}$ and a low $\overline{W}$.
3. If the $\overline{S}$ low transition occurs simultaneously with the $\overline{W}$ low transition, the output buffers remain in a high-impedance state.

WRITE CYCLE TIMING (Note 3)


t_{WC}
Address
$\overline{S}$
t_{WR}
t_W
$\overline{W}$
t_{OTW}
D_{out}
t_{DH}
t_{DW}
D_{in}

MOTOROLA

MCM65116

Advance Information

16K BIT STATIC RANDOM ACCESS MEMORY

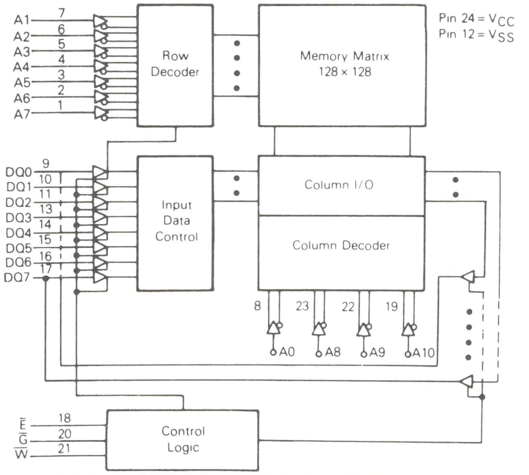
The MCM65116 is a 16,384-bit Static Random Access Memory organized as 2048 words by 8-bits, fabricated using Motorola's High-performance silicon-gate CMOS (HCMOS) technology. It uses a design approach which provides the simple timing features associated with fully static memories and the reduced power associated with CMOS memories. This means low standby power without the need for clocks, nor reduced data rates due to cycle times that exceed access time.

Chip Enable ($\overline{E}$) controls the power-down feature. It is not a clock but rather a chip control that affects power consumption. In less than a cycle time after chip enable ($\overline{E}$) goes high, the part automatically reduces its power requirements and remains in this low-power standby as long as the chip enable ($\overline{E}$) remains high. The automatic power-down feature causes no performance degradation.

The MCM65116 is in a 24-pin dual-in-line package with the industry standard JEDEC approved pinout and is pinout compatible with the industry standard 16K EPROM/ROM.

- Single +5 V Supply
- 2048 Words by 8-Bit Organization
- HCMOS Technology
- Fully Static: No Clock or Timing Strobe Required
- Maximum Access Time: MCM65116-12 — 120 ns
  MCM65116-15 — 150 ns
  MCM65116-20 — 200 ns
- Power Dissipation: 55 mA Maximum (Active)
  10 mA Maximum (Standby-TTL Levels)
  2 mA Maximum (Standby)
  100 μA Maximum (Standby-MCM65LT16)
- Low Voltage Data Retention (MCM65L116 only) 100 μW Maximum

BLOCK DIAGRAM

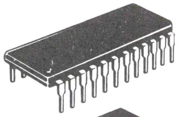


Pin 24 = V_{CC}
Pin 12 = V_{SS}
A1 7
A2 6
A3 5
A4 4
A5 3
A6 2
A7 1
Row Decoder
Memory Matrix 128 × 128
DQ0 9
DQ1 10
DQ2 11
DQ3 13
DQ4 14
DQ5 15
DQ6 16
DQ7 17
Input Data Control
Column I/O
Column Decoder
8 23 22 19
A0 A8 A9 A10
$\overline{E}$ 18
$\overline{G}$ 20
$\overline{W}$ 21
Control Logic

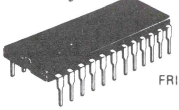
This document contains information on a new product. Specifications and information herein are subject to change without notice.

HCMOS
(COMPLEMENTARY MOS)

**2,048 × 8 BIT
STATIC RANDOM
ACCESS MEMORY**

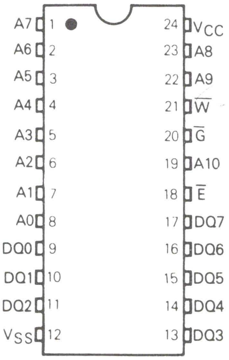


P SUFFIX
PLASTIC PACKAGE
CASE 709



C SUFFIX
FRIT-SEAL CERAMIC PACKAGE
CASE 623

PIN ASSIGNMENTS



A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
DQ0 9
DQ1 10
DQ2 11
V_{SS} 12
24 V_{CC}
23 A8
22 A9
21 $\overline{W}$
20 $\overline{G}$
19 A10
18 $\overline{E}$
17 DQ7
16 DQ6
15 DQ5
14 DQ4
13 DQ3

PIN NAMES

A0-A10	Address Input
DQ0-DQ7	Data Input/Output
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$	Chip Enable
V_{CC}	Power (+5 V)
V_{SS}	Ground

ADI-911/5-82

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Value	Unit
Temperature Under Bias	−10 to +80	°C
Voltage on Any Pin With Respect to V_{SS}	−1.0 to +7.0	V
DC Output Current	20	mA
Power Dissipation	1.2	Watt
Operating Temperature Range	0 to +70	°C
Storage Temperature Range	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature ranges unless otherwise noted.)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	3.5	6.0	V
	V_{IL}	−1.0*	–	0.8	V

*The device will withstand undershoots to the −1.0 volt level with a maximum pulse width of 50 ns at the −0.3 volt level. This is periodically sampled rather than 100% tested.

RECOMMENDED OPERATING CHARACTERISTICS

Parameter	Symbol	MCM65116			MCM65L116			Unit
		Min	Typ*	Max	Min	Typ*	Max	
Input Leakage Current (V_{CC} = 5.5 V, V_{in} = GND to V_{CC})	$\lvert I_{LI} \rvert$	–	–	1	–	–	1	μA
Output Leakage Current ($\overline{E} = V_{IH}$ or $\overline{G} = V_{IH}$ $V_{I/O}$ = GND to V_{CC})	$\lvert I_{LO} \rvert$	–	–	1	–	–	1	μA
Operating Power Supply Current ($\overline{E} = V_{IL}$, $I_{I/O}$ = 0 mA)	I_{CC}	–	35	55	–	35	55	mA
Average Operating Current Minimum cycle, duty = 100%	I_{CC2}	–	35	55	–	35	55	mA
Standby Power Supply Current ($\overline{E} = V_{IH}$)	I_{SB}	–	5	10	–	5	10	mA
($\overline{E} \geq V_{CC} - 0.2$ V, $V_{in} \geq V_{CC} - 0.2$ V or $V_{in} \leq 0.2$ V)	I_{SB1}	–	20	2000	–	4	100	μA
Output Low Voltage (I_{OL} = 2.1 mA)	V_{OL}	–	–	0.4	–	–	0.4	V
Output High Voltage (I_{OH} = −1.0 mA)**	V_{OH}	2.4	–	–	2.4	–	–	V

*V_{CC} = 5 V, T_A = 25°C

**Also, output voltages are compatible with Motorola's new high-speed CMOS logic family if the same power supply voltage is used.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance except $\overline{E}$	C_{in}	3	5	pF
Input/Output Capacitance and $\overline{E}$ Input Capacitance	$C_{I/O}$	5	7	pF

MODE SELECTION

Mode	$\overline{E}$	$\overline{G}$	$\overline{W}$	V_{CC} Current	DQ
Standby	H	X	X	I_{SB}, I_{SB1}	High Z
Read	L	L	H	I_{CC}	Q
Write Cycle (1)	L	H	L	I_{CC}	D
Write Cycle (2)	L	L	L	I_{CC}	D

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted.)

Input Pulse Levels..0.8 Volt to 2.4 Volts

Input Rise and Fall Times ....10 ns

Input and Output Timing Levels ....1.5 Volts

Output Load ....1 TTL Gate and $C_L = 100$ pF

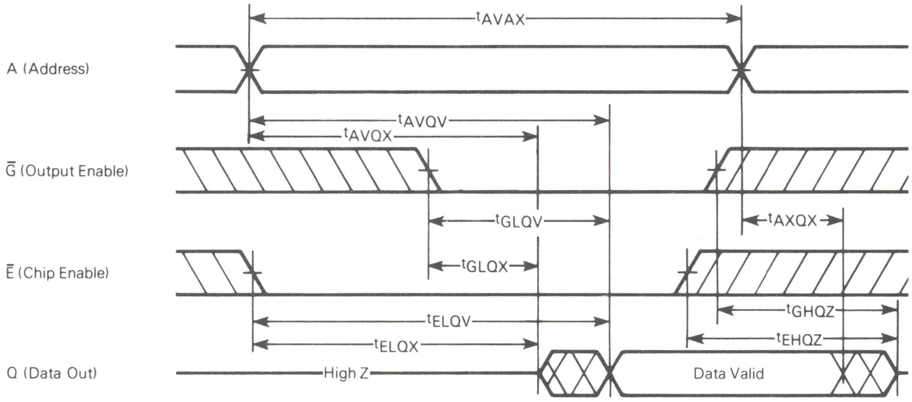
READ CYCLE

Parameter	Symbol	MCM65116-12 MCM65L116-12		MCM65116-15 MCM65L116-15		MCM65116-20 MCM65L116-20		Unit
		Min	Max	Min	Max	Min	Max	
Address Valid to Address Don't Care (Cycle Time when Chip Enable is Held Active)	t_{AVAX}	120	–	150	–	200	–	ns
Chip Enable Low to Chip Enable High	t_{ELEH}	120	–	150	–	200	–	ns
Address Valid to Output Valid (Access)	t_{AVQV}	–	120	–	150	–	200	ns
Chip Enable Low to Output Valid (Access)	t_{ELQV}	–	120	–	150	–	200	ns
Address Valid to Output Invalid	t_{AVQX}	10	–	15	–	15	–	ns
Chip Enable Low to Output Invalid	t_{ELQX}	10	–	15	–	15	–	ns
Chip Enable High to Output High Z	t_{EHQZ}	0	40	0	50	0	60	ns
Output Enable to Output Valid	t_{GLQV}	–	80	–	100	–	120	ns
Output Enable to Output Invalid	t_{GLQX}	10	–	15	–	15	–	ns
Output Enable to Output High Z	t_{GLQZ}	0	40	0	50	0	60	ns
Address Invalid to Output Invalid	t_{AXQX}	10	–	15	–	15	–	ns
Address Valid to Chip Enable Low (Address Setup)	t_{AVEL}	0	–	0	–	0	–	ns
Chip Enable to Power-Up Time	t_{PU}	0	–	0	–	0	–	ns
Chip Disable to Power-Down Time	t_{PD}	–	30	–	30	–	30	ns

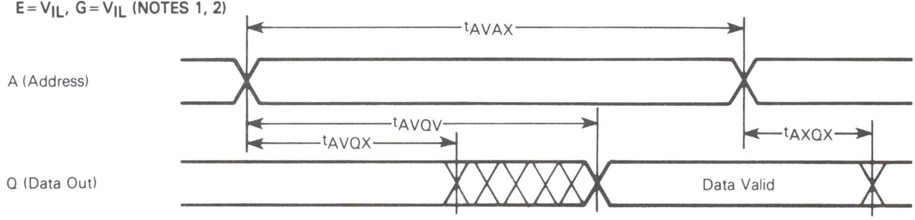
WRITE CYCLE

Parameter	Symbol	MCM65116-12 MCM65L116-12		MCM65116-15 MCM65L116-15		MCM65116-20 MCM65L116-20		Unit
		Min	Max	Min	Max	Min	Max	
Chip Enable Low to Write High	t_{ELWH}	70	–	90	–	120	–	ns
Address Valid to Write High	t_{AVWH}	105	–	120	–	140	–	ns
Address Valid to Write Low (Address Setup)	t_{AVWL}	20	–	20	–	20	–	ns
Write Low to Write High (Write Pulse Width)	t_{WLWH}	70	–	90	–	120	–	ns
Write High to Address Don't Care	t_{WHAX}	5	–	10	–	10	–	ns
Data Valid to Write High	t_{DVWH}	35	–	40	–	60	–	ns
Write High to Data Don't Care (Data Hold)	t_{WHDX}	5	–	10	–	10	–	ns
Write Low to Output High Z	t_{WLQZ}	0	50	0	60	0	60	ns
Write High to Output Valid	t_{WHQV}	5	–	10	–	10	–	ns
Output Disable to Output High Z	t_{GHQZ}	0	40	0	50	0	60	ns

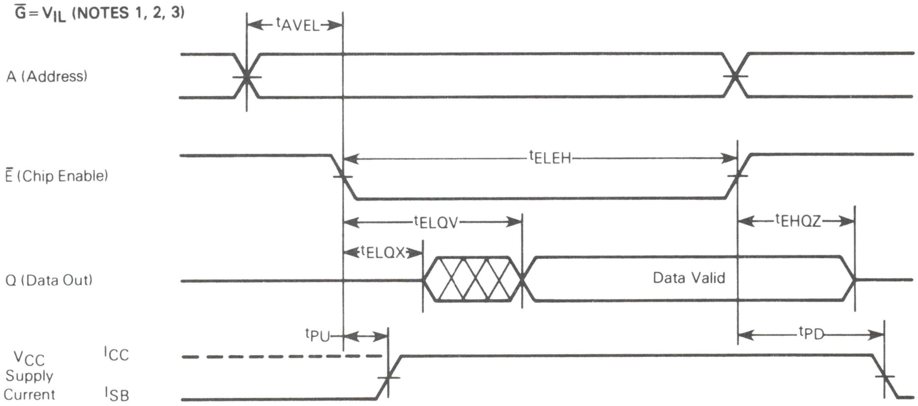
READ CYCLE TIMING 1 (NOTES 1 AND 2)


tAVAX
A (Address)
tAVQV
tAVQX
$\overline{G}$ (Output Enable)
tGLQV
tAXQX
$\overline{E}$ (Chip Enable)
tGLQX
tGHQZ
tELQV
tEHQZ
tELQX
Q (Data Out)
High Z
Data Valid

READ CYCLE TIMING 2
$\overline{E}=V_{IL}$, $\overline{G}=V_{IL}$ (NOTES 1, 2)


tAVAX
A (Address)
tAVQV
tAVQX
tAXQX
Q (Data Out)
Data Valid

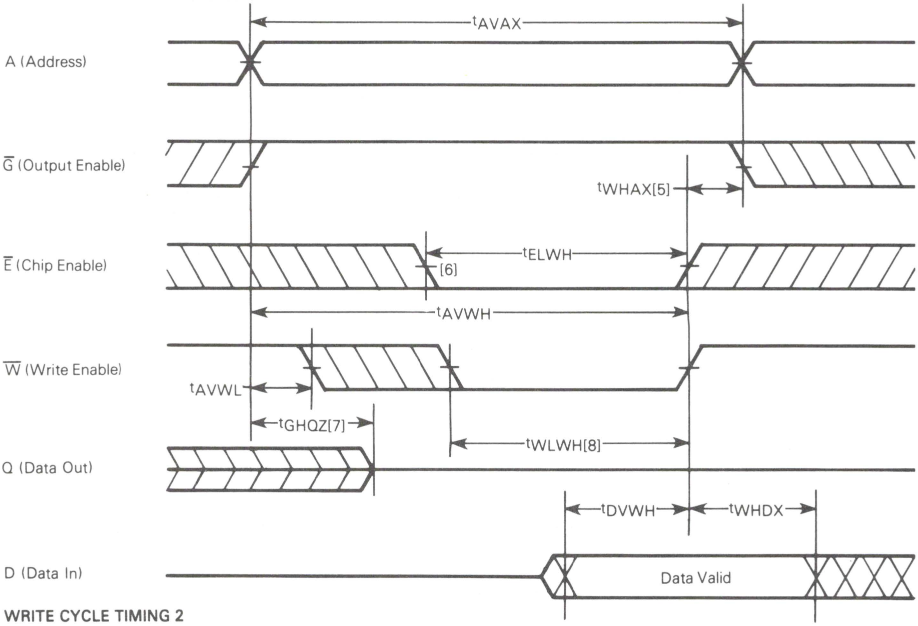
READ CYCLE TIMING 3
$\overline{G}=V_{IL}$ (NOTES 1, 2, 3)


tAVEL
A (Address)
tELEH
$\overline{E}$ (Chip Enable)
tELQV
tEHQZ
tELQX
Q (Data Out)
Data Valid
tPU
tPD
VCC Supply Current
ICC
ISB

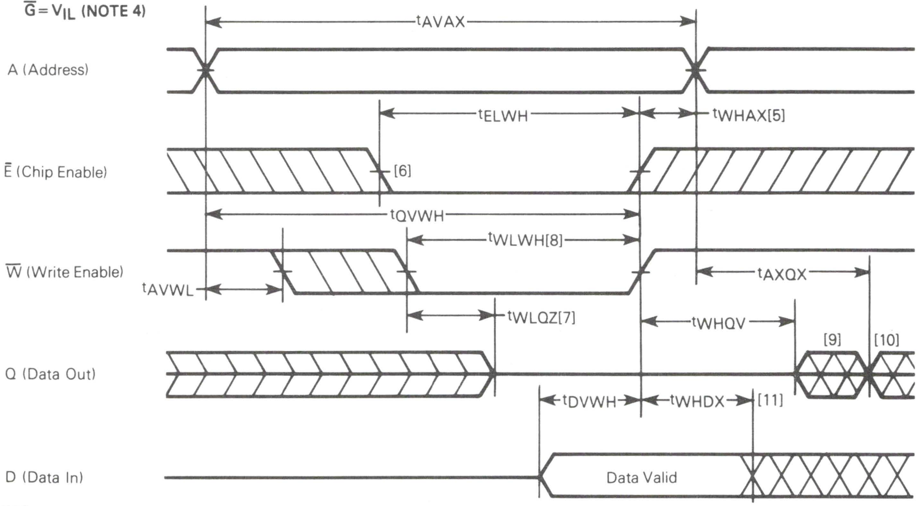
NOTES:

1. Write Enable ($\overline{W}$) is High for Read Cycle.
2. When Chip Enable ($\overline{E}$) is Low, the address input must not be in the high impedance state.
3. Address Valid prior to or coincident with Chip Enable ($\overline{E}$) transition Low.

WRITE CYCLE TIMING 1 (NOTE 4)


tAVAX
A (Address)
G̅ (Output Enable)
tWHAX[5]
E̅ (Chip Enable)
tELWH
[6]
tAVWH
W̅ (Write Enable)
tAVWL
tGHQZ[7]
tWLWH[8]
Q (Data Out)
tDVWH
tWHDX
D (Data In)
Data Valid

WRITE CYCLE TIMING 2
$\overline{G} = V_{IL}$ (NOTE 4)


tAVAX
A (Address)
tELWH
tWHAX[5]
E̅ (Chip Enable)
[6]
tQVWH
tWLWH[8]
W̅ (Write Enable)
tAVWL
tAXQX
tWLQZ[7]
tWHQV
[9]
[10]
Q (Data Out)
tDVWH
tWHDX
[11]
D (Data In)
Data Valid

NOTES:

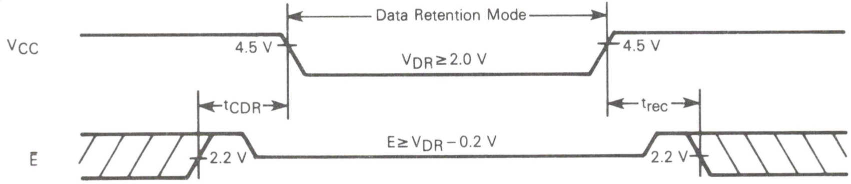
4. Write Enable ($\overline{W}$) must be high during all address transitions.
5. t_{WHAX} is measured from the earlier of Chip Enable ($\overline{E}$) or Write Enable ($\overline{W}$) going high to the end of write cycle.
6. If the Chip Enable ($\overline{E}$) low transition occurs simultaneously with the Write Enable ($\overline{W}$) low transitions or after the Write Enable ($\overline{W}$) transition, the output remains in a high impedance state.
7. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
8. A write occurs during the overlap of a low Chip Enable ($\overline{E}$) and a low Write Enable ($\overline{W}$).
9. Q (Data Out) is the same phase as write data of this write cycle.
10. Q (Data Out) is the read of the next address.
11. If Chip Enable ($\overline{E}$) is low during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

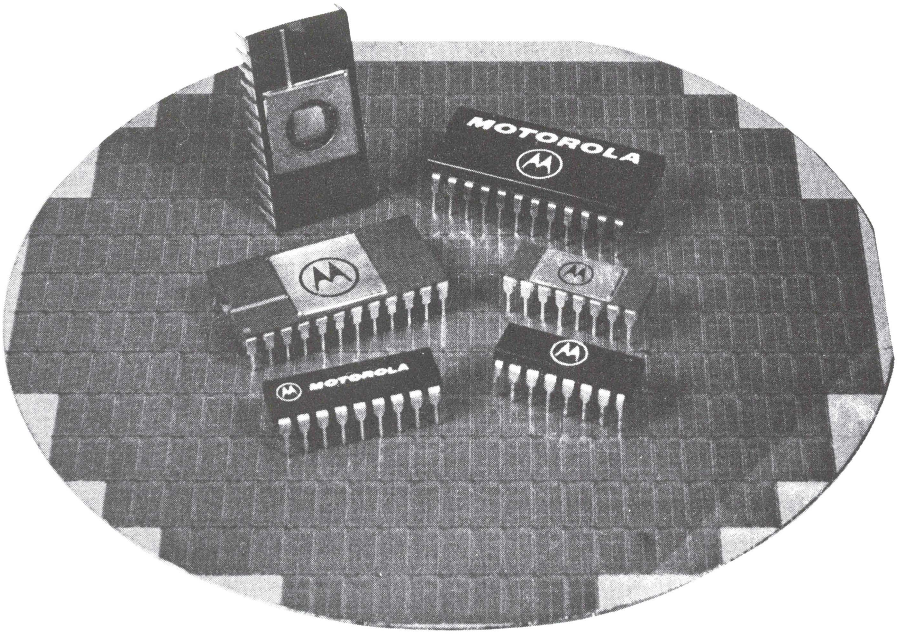
LOW V_{CC} DATA RETENTION CHARACTERISTICS ($T_A = 0$ to $+70°C$) (MCM65L116 Only)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
V_{CC} for Data Retention	$\overline{E} \geq V_{CC} - 0.2$ V $V_{in} \geq V_{CC} - 0.2$ V or $V_{in} \leq 0.2$ V	V_{DR}	2.0	–	–	V
Data Retention Current	$V_{CC} = 3.0$ V, $\overline{E} \geq 2.8$ V $V_{in} \geq 2.8$ V or $V_{in} \leq 0.2$ V	I_{CCDR}	–	–	50	μA
Chip Disable to Data Retention Time	See Retention Waveform	t_{CDR}	0	–	–	ns
Operation Recovery Time		t_{rec}	*t_{AVAX}	–	–	ns

*t_{AVAX} = Read Cycle Time.

LOW V_{CC} DATA RETENTION WAVEFORM


Data Retention Mode
VCC
4.5 V
VDR ≥ 2.0 V
4.5 V
tCDR
trec
Ē
2.2 V
E ≥ VDR − 0.2 V
2.2 V


MOTOROLA
MOTOROLA

MOS EPROM

MOTOROLA

MCM2708
MCM27A08

MOS

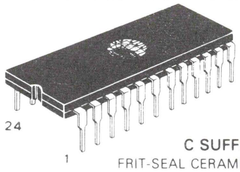
(N-CHANNEL, SILICON-GATE)

1024 X 8-BIT
UV ERASABLE PROM

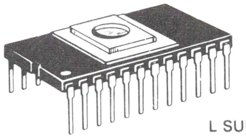
1024 X 8 ERASABLE PROM

The MCM2708/27A08 is an 8192-bit Erasable and Electrically Reprogrammable PROM designed for system debug usage and similar applications requiring nonvolatile memory that could be reprogrammed periodically. The transparent window on the package allows the memory content to be erased with ultraviolet light. Pin-for-pin mask-programmable ROMs are available for large volume production runs of systems initially using the MCM2708/27A08.

- Organized as 1024 Bytes of 8 Bits
- Static Operation
- Standard Power Supplies of +12 V, +5 V and −5 V
- Maximum Access Time = 300 ns — MCM27A08
  450 ns — MCM2708
- Low Power Dissipation
- Chip-Select Input for Memory Expansion
- TTL Compatible
- Three-State Outputs
- Pin Equivalent to the 2708
- Pin-for-Pin Compatible to MCM65308, MCM68308 or 2308 Mask-Programmable ROMs



C SUFFIX
FRIT-SEAL CERAMIC PACKAGE
CASE 623A



L SUFFIX
CERAMIC PACKAGE
CASE 716

PIN CONNECTION DURING READ OR PROGRAM

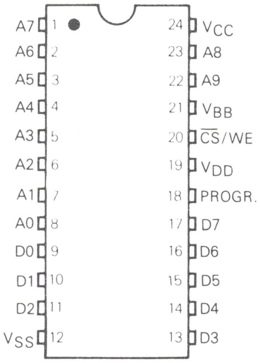
Mode	Pin Number						
	9-11, 13-17	12	18	19	20	21	24
Read	D_{out}	V_{SS}	V_{SS}	V_{DD}	V_{IL}	V_{BB}	V_{CC}
Program	Din	V_{SS}	Pulsed V_{IHP}	V_{DD}	V_{IHW}	V_{BB}	V_{CC}

ABSOLUTE MAXIMUM RATINGS (1)

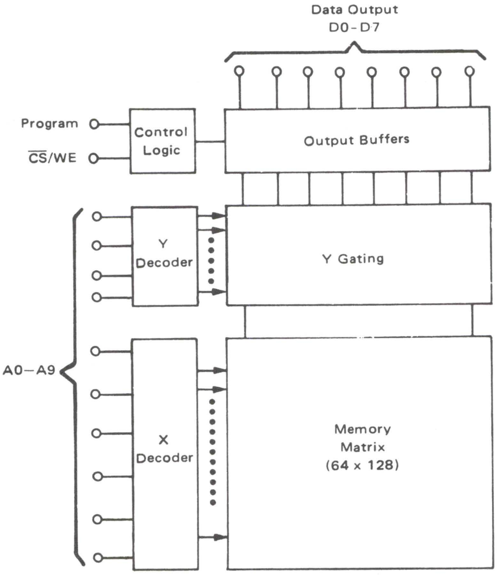
Rating	Value	Unit
Operating Temperature	0 to +70	°C
Storage Temperature	−65 to +125	°C
V_{DD} with Respect to V_{BB}	+20 to −0.3	Vdc
V_{CC} and V_{SS} with Respect to V_{BB}	+15 to −0.3	Vdc
All Input or Output Voltages with Respect to V_{BB} during Read	+15 to −0.3	Vdc
$\overline{CS}$/WE Input with Respect to V_{BB} during Programming	+20 to −0.3	Vdc
Program Input with Respect to V_{BB}	+35 to −0.3	Vdc
Power Dissipation	1.8	Watts

Note 1:
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

PIN ASSIGNMENT



BLOCK DIAGRAM



DC READ OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED DC READ OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC} V_{DD} V_{BB}	4.75 11.4 -5.25	5.0 12 -5.0	5.25 12.6 -4.75	Vdc Vdc Vdc
Input High Voltage	V_{IH}	3.0	–	V_{CC} + 1.0	Vdc
Input Low Voltage	V_{IL}	V_{SS}	–	0.65	Vdc

READ OPERATION DC CHARACTERISTICS

Characteristic	Condition	Symbol	Min	Typ	Max	Unit
Address and CS Input Sink Current	V_{in} = 5.25 V or V_{in} = V_{IL}	I_{in}	–	1	10	μA
Output Leakage Current	V_{out} = 5.25 V, $\overline{CS}$/WE = 5 V	I_{LO}	–	1	10	μA
V_{DD} Supply Current (Note 2)	Worst-Case Supply Currents	I_{DD}	–	50	65	mA
V_{CC} Supply Current (Note 2)	All Inputs High	I_{CC}	–	6	10	mA
V_{BB} Supply Current (Note 2)	$\overline{CS}$/WE = 5.0 V, T_A = 0°C	I_{BB}	–	30	45	mA
Output Low Voltage	I_{OL} = 1.6 mA	V_{OL}	–	–	0.45	V
Output High Voltage	I_{OH} = -100 μA	$V_{OH}1$	3.7	–	–	V
Output High Voltage	I_{OH} = -1.0 mA	$V_{OH}2$	2.4	–	–	V
Power Dissipation (Note 2)	T_A = 70°C	P_D	–	–	800	mW

Note 2:

The total power dissipation is specified at 800 mW. It is not calculable by summing the various current (I_{DD}, I_{CC}, and I_{BB}) multiplied by their respective voltages, since current paths exist between the various power supplies and V_{SS}. The I_{DD}, I_{CC}, and I_{BB} currents should be used to determine power supply capacity only.

V_{BB} must be applied prior to V_{CC} and V_{DD}. V_{BB} must also be the last power supply switched off.

AC READ OPERATING CONDITIONS AND CHARACTERISTICS
(Full operating voltage and temperature range unless otherwise noted.)
(All timing with t_r = t_f = 20 ns, Load per Note 3)

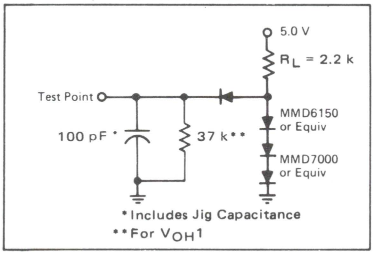
Characteristic	Symbol	MCM27A08			MCM2708			Unit
		Min	Typ	Max	Min	Typ	Max	
Address to Output Delay	t_{AO}	–	220	300	–	280	450	ns
Chip Select to Output Delay	t_{CO}	–	60	120	–	60	120	ns
Data Hold from Address	t_{DHA}	0	–	–	0	–	–	ns
Data Hold from Deselection	t_{DHD}	0	–	120	0	–	120	ns

CAPACITANCE (periodically sampled rather than 100% tested.)

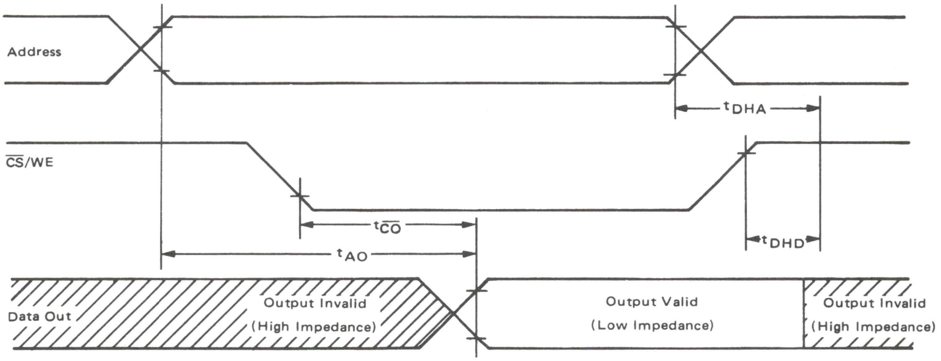
Characteristic	Condition	Symbol	Typ	Max	Unit
Input Capacitance (f = 1.0 MHz)	V_{in} = 0 V, T_A = 25°C	C_{in}	4.0	6.0	pF
Output Capacitance (f = 1.0 MHz)	V_{out} = 0 V, T_A = 25°C	C_{out}	8.0	12	pF

Note 3:
Output Load = 1 TTL Gate and C_L = 100 pF (Includes Jig Capacitance)
Timing Measurement Reference Levels: Inputs: 0.8 V and 2.8 V
Outputs: 0.8 V and 2.4 V

AC TEST LOAD


5.0 V
R_L = 2.2 k
Test Point
100 pF *
37 k**
MMD6150 or Equiv
MMD7000 or Equiv
*Includes Jig Capacitance
**For $V_{OH}1$

READ OPERATION TIMING DIAGRAM


Address
t_{DHA}
$\overline{CS}$/WE
$t_{\overline{CO}}$
t_{DHD}
t_{AO}
Data Out
Output Invalid
(High Impedance)
Output Valid
(Low Impedance)
Output Invalid
(High Impedance)

DC PROGRAMMING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED PROGRAMMING OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	Vdc
	V_{DD}	11.4	12	12.6	Vdc
	V_{BB}	-5.25	-5.0	-4.75	Vdc
Input High Voltage for All Addresses and Data	V_{IH}	3.0	–	V_{CC} + 1.0	Vdc
Input Low Voltage (except Program)	V_{IL}	V_{SS}	–	0.65	Vdc
$\overline{\text{CS}}$/WE Input High Voltage (Note 4)	V_{IHW}	11.4	12	12.6	Vdc
Program Pulse Input High Voltage (Note 4)	V_{IHP}	25	–	27	Vdc
Program Pulse Input Low Voltage (Note 5)	V_{ILP}	V_{SS}	–	1.0	Vdc

Note 4: Referenced to V_{SS}.
Note 5: $V_{IHP} - V_{ILP}$ = 25 V min.

PROGRAMMING OPERATION DC CHARACTERISTICS

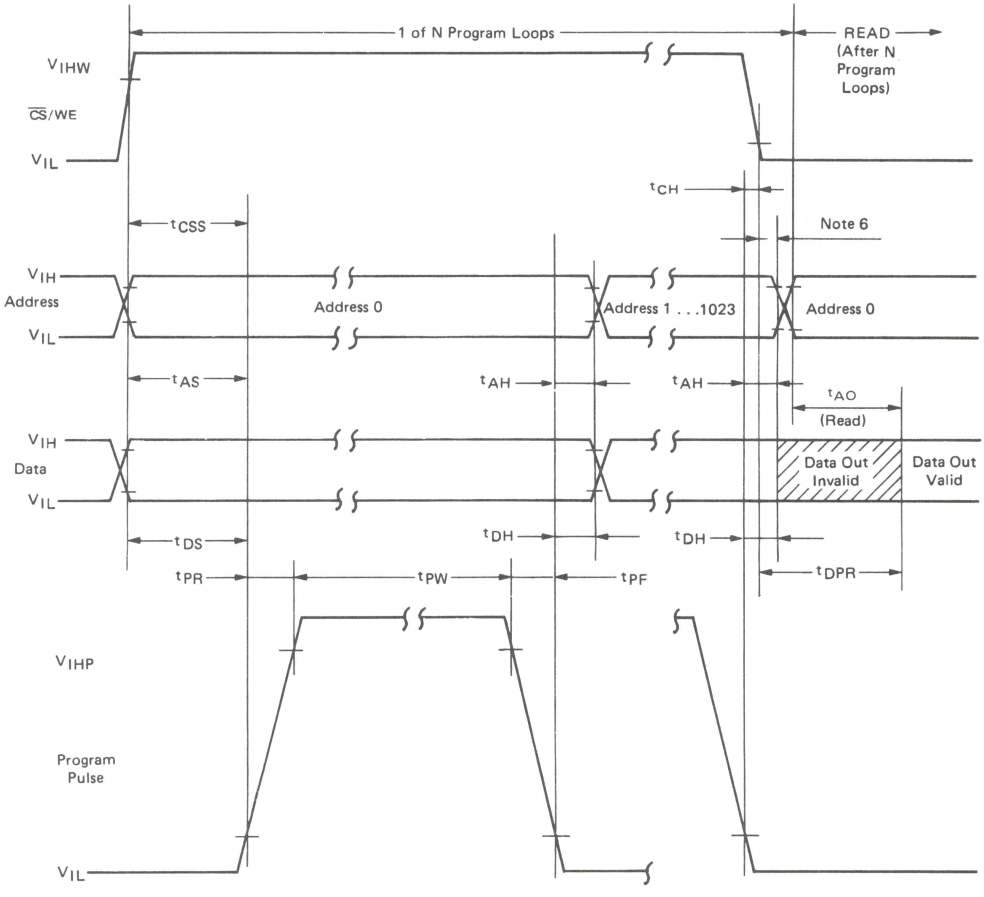
Characteristic	Condition	Symbol	Min	Typ	Max	Unit
Address and $\overline{\text{CS}}$/WE Input Sink Current	V_{in} = 5.25 V	I_{LI}	–	–	10	µAdc
Program Pulse Source Current		I_{IPL}	–	–	3.0	mAdc
Program Pulse Sink Current		I_{IPH}	–	–	20	mAdc
V_{DD} Supply Current	Worst-Case Supply Currents All Inputs High $\overline{\text{CS}}$/WE = 5 V, T_A = 0°C	I_{DD}	–	50	65	mAdc
V_{CC} Supply Current		I_{CC}	–	6	10	mAdc
V_{BB} Supply current		I_{BB}	–	30	45	mAdc

AC PROGRAMMING OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
Address Setup Time	t_{AS}	10	–	µs
$\overline{\text{CS}}$/WE Setup Time	t_{CSS}	10	–	µs
Data Setup Time	t_{DS}	10	–	µs
Address Hold Time	t_{AH}	1.0	–	µs
$\overline{\text{CS}}$/WE Hold Time	t_{CH}	0.5	–	µs
Data Hold Time	t_{DH}	1.0	–	µs
Chip Deselect to Output Float Delay	t_{DF}	0	120	ns
Program to Read Delay	t_{DPR}	–	10	µs
Program Pulse Width	t_{PW}	0.1	1.0	ms
Program Pulse Rise Time	t_{PR}	0.5	2.0	µs
Program Pulse Fall Time	t_{PF}	0.5	2.0	µs

PROGRAMMING OPERATION TIMING DIAGRAM


1 of N Program Loops
READ
(After N Program Loops)
V_{IHW}
$\overline{CS}$/WE
V_{IL}
t_{CH}
Note 6
t_{CSS}
V_{IH}
Address
V_{IL}
Address 0
Address 1 . . .1023
Address 0
t_{AS}
t_{AH}
t_{AH}
t_{AO}
(Read)
V_{IH}
Data
V_{IL}
Data Out Invalid
Data Out Valid
t_{DS}
t_{DH}
t_{DH}
t_{PR}
t_{PW}
t_{PF}
t_{DPR}
V_{IHP}
Program Pulse
V_{IL}

Note 6: The $\overline{CS}$/WE transition must occur after the Program Pulse transition and before the Address Transition.

PROGRAMMING INSTRUCTIONS

After the completion of an ERASE operation, every bit in the device is in the "1" state (represented by Output High). Data are entered by programming zeros (Output Low) into the required bits. The words are addressed the same way as in the READ operation. A programmed "0" can only be changed to a "1" by ultraviolet light erasure.

To set the memory up for programming mode, the $\overline{\text{CS}}$/WE input (Pin 20) should be raised to +12 V. Programming data is entered in 8-bit words through the data output terminals (D0 to D7).

Logic levels for the data lines and addresses and the supply voltages (V_{CC}, V_{DD}, V_{BB}) are the same as for the READ operation.

After address and data setup one program pulse per address is applied to the program input (Pin 18). A program loop is a full pass through all addresses. Total programming time, $T_{Ptotal} = N \times t_{PW} \geqslant 100$ ms. The required number of program loops (N) is a function of the program pulse width (t_{PW}), where: $0.1 \text{ ms} \leqslant t_{PW} \leqslant 1.0$ ms; correspondingly N is: $100 \leqslant N \leqslant 1000$. There must be N successive loops through all 1024 addresses. It is not permitted to apply more than one program pulse in succession to the same address (i.e., N program pulses to an address and then change to the next address to be programmed). At the end of a program sequence the $\overline{\text{CS}}$/WE falling edge transition must occur before the first address transition, when changing from a PROGRAM to a READ cycle. The program pin (Pin 18) should be pulled down to V_{ILP} with an active device, because this pin sources a small amount of current (I_{IPL}) when $\overline{\text{CS}}$/WE is at V_{IHW} (12 V) and the program pulse is at V_{ILP}.

EXAMPLES FOR PROGRAMMING

Always use the $T_{Ptotal} = N \times t_{PW} \geqslant 100$ ms relationship.

1. All 8192 bits should be programmed with a 0.2 ms program pulse width.

   The minimum number of program loops:

   $N = \frac{T_{Ptotal}}{t_{PW}} = \frac{100 \text{ ms}}{0.2 \text{ ms}} = 500$. One program loop consists of words 0 to 1023.

2. Words 0 to 200 and 300 to 700 are to be programmed. All other bits are "don't care". The program pulse width is 0.5 ms. The minimum number of program loops, $N = \frac{100}{0.5} = 200$. One program loop consists of words 0 to 1023. The data entered into the "don't care" bits should be all 1s.

3. Same requirements as example 2, but the EPROM is now to be updated to include data for words 850 to 880. The minimum number of program loops is the same as in the previous example, N = 200. One program loop consists of words 0 to 1023. The data entered into the "don't care" bits should be all 1s. Addresses 0 to 200 and 300 to 700 must be reprogrammed with their original data pattern.

ERASING INSTRUCTIONS

The MCM2708/27A08 can be erased by exposure to high intensity shortwave ultraviolet light, with a wavelength of 2537 Å. The recommended integrated dose (i.e., UV-intensity x exposure time) is 12.5 Ws/cm^2. As an example, using the "Model 30-000" UV-Eraser (Turner Designs, Mountain View, CA94043) the ERASE-time is 30 minutes. The lamps should be used without shortwave filters and the MCM2708/27A08 should be positioned about one inch away from the UV-tubes.

MOTOROLA

TMS2716
TMS27A16

MOS

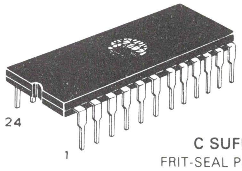
(N-CHANNEL, SILICON-GATE)

2048 × 8-BIT
UV ERASABLE PROM

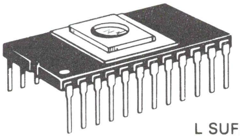
2048 × 8 ERASABLE PROM

The TMS2716 and TMS27A16 are 16,384-bit Erasable and Electrically Reprogrammable PROMs designed for system debug usage and similar applications requiring nonvolatile memory that could be reprogrammed periodically. The transparent window on the package allows the memory content to be erased with ultraviolet light. The TMS2716 is pin compatible with 2708 EPROMs, allowing easy memory size doubling.

- Organized as 2048 Bytes of 8 Bits
- Fully Static Operation (No Clocks, No Refresh)
- Standard Power Supplies of +12 V, +5 V, and −5 V
- Maximum Access Time = 300 ns – TMS27A16
  450 ns – TMS2716
- Chip-Select Input for Memory Expansion
- TTL Compatible – No Pull-up Resistors Required
- Three-State Outputs for OR-Tie Capability
- The TMS2716 is Pin Compatible to MCM2708 and MCM68708 EPROMs

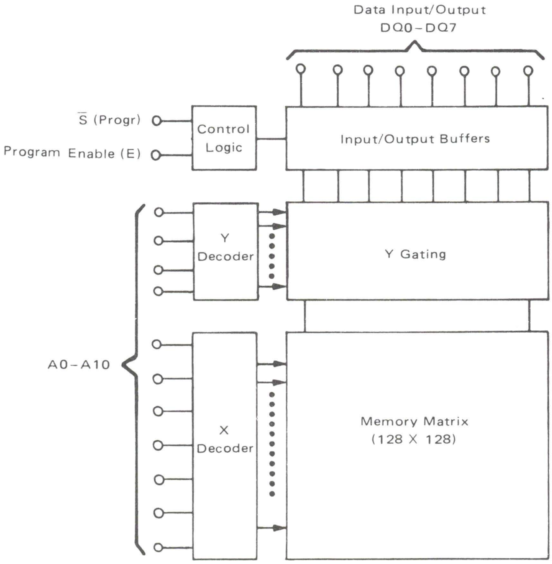


C SUFFIX
FRIT-SEAL PACKAGE
CASE 623A



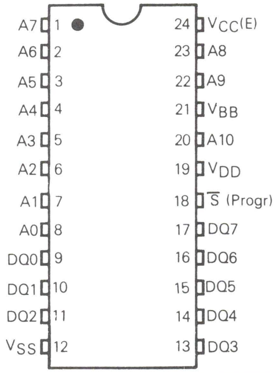
L SUFFIX
CERAMIC PACKAGE
CASE 716

BLOCK DIAGRAM



Data Input/Output
DQ0–DQ7
S̄ (Progr)
Program Enable (E)
Control Logic
Input/Output Buffers
Y Decoder
Y Gating
A0–A10
X Decoder
Memory Matrix
(128 × 128)

PIN ASSIGNMENT



A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
DQ0 9
DQ1 10
DQ2 11
VSS 12
24 VCC(E)
23 A8
22 A9
21 VBB
20 A10
19 VDD
18 S̄ (Progr)
17 DQ7
16 DQ6
15 DQ5
14 DQ4
13 DQ3

PIN NAMES

A0-A10	Address Inputs
DQ0-DQ7	Data Input (Program or Output (Read)
(E)	Program Enable
S̄	Chip Select
(Progr)	Program Pulse
V_{BB}	−5 V Power Supply
V_{CC}	+5 V Power Supply
V_{DD}	+12 V Power Supply
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS (1)

Rating	Value	Unit
Operating Temperature	0 to +70	°C
Storage Temperature	−65 to +125	°C
V_{DD} with Respect to V_{BB}	+20 to −0.3	V
V_{CC} and V_{SS} with Respect to V_{BB}	+15 to −0.3	V
All Input or Output Voltage with Respect to V_{BB} During Read	+15 to −0.3	V
(E) Input with Respect to V_{BB} During Programming	+20 to −0.3	V
Program Input with Respect to V_{BB}	+35 to −0.3	V
Power Dissipation	1.8	Watts

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

PIN CONNECTION DURING READ OR PROGRAM

	Pin Number		
Mode	9–11, 13–17	18	24
Read	D_{out}	V_{IL} or V_{IH}	V_{CC}
Program	D_{in}	Pulsed V_{IHP}	V_{IHW}

DC READ OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED DC READ OPERATING CONDITIONS

Parameter		Symbol	Min	Nom	Max	Unit
Supply Voltage	TMS2716	V_{CC}	4.75	5.0	5.25	V
		V_{DD}	11.4	12	12.6	V
		V_{BB}	−5.25	−5.0	−4.75	V
	TMS27A16	V_{CC}	4.5	5.0	5.5	V
		V_{DD}	10.8	12	13.2	V
		V_{BB}	−5.5	−5.0	−4.5	V
Input High Voltage		V_{IH}	2.2	–	V_{CC} + 1.0	V
Input Low Voltage		V_{IL}	V_{SS}	–	0.65	V

READ OPERATING DC CHARACTERISTICS

Characteristic	Condition	Symbol	Min	Typ	Max	Unit
Address Input Sink Current	$V_{in} = V_{CC}$max or $V_{in} = V_{IL}$	I_{in}	–	1	10	µA
Output Leakage Current	$V_{out} = V_{CC}$max and $\overline{S} = 5$ V	I_{LO}	–	1	10	µA
V_{DD} Supply Current	Worst-Case Supply Currents All Inputs High (E) = 5.0 V, T_A = 0°C	I_{DD}	–	–	65	mA
V_{CC} Supply Current		I_{CC}	–	–	12	mA
V_{BB} Supply Current		I_{BB}	–	–	45	mA
Output Low Voltage	I_{OL} = 1.6 mA	V_{OL}	–	–	0.45	V
Output High Voltage	I_{OH} = −100 µA	V_{OH1}	3.7	–	–	V
Output High Voltage	I_{OH} = −1.0 mA	V_{OH2}	2.4	–	–	V

V_{BB} must be applied prior to V_{CC} and V_{DD}. V_{BB} must also be the last power supply switched off.

CAPACITANCE (periodically sampled rather than 100% tested)

Characteristic	Condition	Symbol	Typ	Max	Unit
Input Capacitance (f = 1.0 MHz)	V_{in} = 0 V, T_A = 25°C	C_{in}	4.0	6.0	pF
Output Capacitance (f = 1.0 MHz)	V_{out} = 0 V, T_A = 25°C	C_{out}	8.0	12	pF

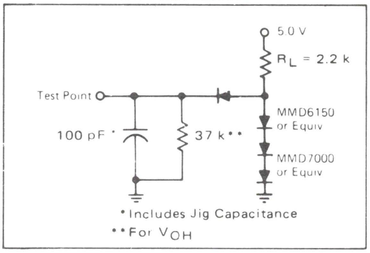
AC READ OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)
(All timing with $t_r = t_f = 20$ ns, Load per Note 2)

Characteristic	Symbol	TMS2716		TMS27A16		Unit
		Min	Max	Min	Max	
Address to Output Delay	t_{AVQV}	–	450	–	300	ns
Chip Select to Output Delay	t_{SLQV}	–	120	–	120	ns
Data Hold from Address	t_{AXQZ}	10	–	10	–	ns
Data Hold from Deselection	t_{SHQZ}	10	120	10	120	ns

NOTE 2: Output Load = 1 TTL Gate and C_L = 100 pF (Includes Jig Capacitance)
Timing Measurement Reference Levels – Inputs: 0.8 V and 2.8 V
Outputs: 0.8 V and 2.4 V

AC TEST LOAD


5.0 V
R_L = 2.2 k
Test Point
100 pF *
37 k**
MMD6150 or Equiv
MMD7000 or Equiv

* Includes Jig Capacitance
** For V_{OH}

TIMING PARAMETER ABBREVIATIONS

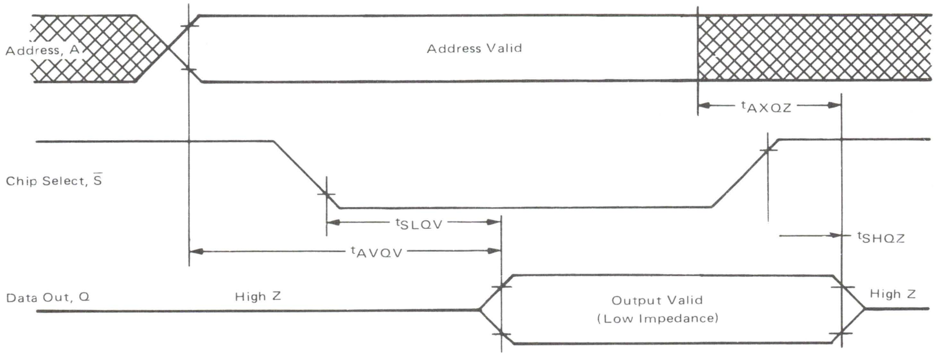
t X X X X
signal name from which interval is defined
transition direction for first signal
signal name to which interval is defined
transition direction for second signal

The transition definitions used in this data sheet are:
- H = transition to high
- L = transition to low
- V = transition to valid
- X = transition to invalid or don't care
- Z = transition to off (high impedance)

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ OPERATION TIMING DIAGRAM


Address, A
Address Valid
t_{AXQZ}
Chip Select, $\overline{S}$
t_{SLQV}
t_{AVQV}
t_{SHQZ}
Data Out, Q
High Z
Output Valid
(Low Impedance)
High Z

DC PROGRAMMING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED PROGRAMMING OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage — TMS2716 and TMS27A16	V_{CC} V_{DD} V_{BB}	4.75 11.4 -5.25	5.0 12 -5.0	5.25 12.6 -4.75	Vdc Vdc Vdc
Input High Voltage for Data	V_{IHD}	3.8	–	$V_{CC}+1$	Vdc
Input Low Voltage for Data	V_{ILD}	V_{SS}	–	0.65	Vdc
Input High Voltage for Addresses	V_{IHA}	3.8	–	$V_{CC}+1$	Vdc
Input Low Voltage for Addresses	V_{ILA}	V_{SS}	–	0.4	Vdc
Program Enable (E) Input High Voltage (Note 3)	V_{IHW}	11.4	12	12.6	Vdc
Program Enable (E) Input Low Voltage (Note 3)	$V_{ILW}=V_{CC}$	4.75	5.0	5.25	Vdc
Program Pulse Input High Voltage (Note 3)	V_{IHP}	25	–	27	Vdc
Program Pulse Input Low Voltage (Note 4)	V_{ILP}	V_{SS}	–	1.0	Vdc

NOTE 3: Referenced to V_{SS}.
NOTE 4: $V_{IHP} - V_{ILP} = 25$ V min.

PROGRAMMING OPERATION DC CHARACTERISTICS

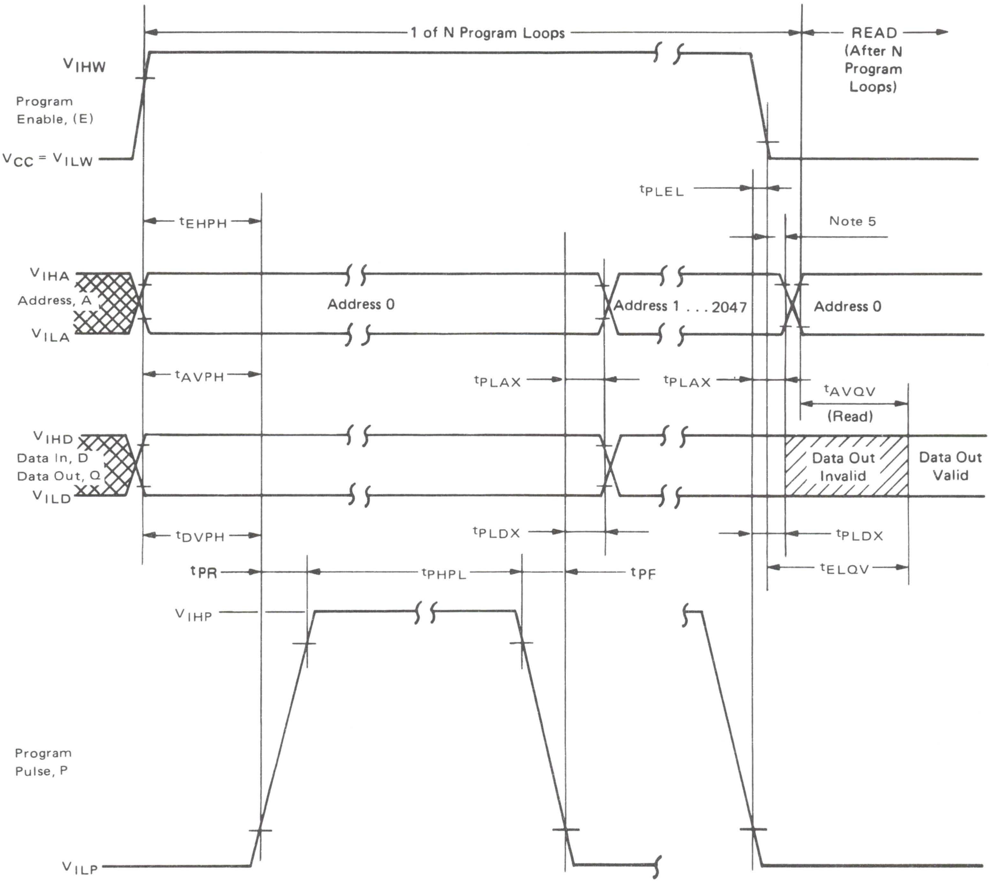
Characteristic	Condition	Symbol	Min	Typ	Max	Unit
Address Input Sink Current	$V_{in} = 5.25$ V	I_{LI}	–	–	10	µAdc
Program Pulse Source Current		I_{IPL}	–	–	3.0	mAdc
Program Pulse Sink Current		I_{IPH}	–	–	20	mAdc
V_{DD} Supply Current	Worst-Case Supply Currents All Inputs High (E) = 5 V, $T_A = 0^oC$	I_{DD}	–	–	65	mAdc
V_{CC} Supply Current		I_{CC}	–	–	15	mAdc
V_{BB} Supply current		I_{BB}	–	–	45	mAdc

AC PROGRAMMING OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Address Setup Time	t_{AVPH}	10	–	µs
(E) Setup Time	t_{EHPH}	10	–	µs
Data Setup Time	t_{DVPH}	10	–	µs
Address Hold Time	t_{PLAX}	1.0	–	µs
(E) Hold Time	t_{PLEL}	0.5	–	µs
Data Hold Time	t_{PLDX}	1.0	–	µs
Program to Read Delay	t_{ELQV}	–	10	µs
Program Pulse Width	t_{PHPL}	0.1	1.0	ms
Program Pulse Rise Time	t_{PR}	0.5	2.0	µs
Program Pulse Fall Time	t_{PF}	0.5	2.0	µs

PROGRAMMING OPERATION TIMING DIAGRAM


1 of N Program Loops
READ (After N Program Loops)
V_{IHW}
Program Enable, (E)
$V_{CC} = V_{ILW}$
t_{PLEL}
t_{EHPH}
Note 5
V_{IHA}
Address, A
V_{ILA}
Address 0
Address 1 . . . 2047
Address 0
t_{AVPH}
t_{PLAX}
t_{PLAX}
t_{AVQV}
(Read)
V_{IHD}
Data In, D
Data Out, Q
V_{ILD}
Data Out Invalid
Data Out Valid
t_{DVPH}
t_{PLDX}
t_{PLDX}
t_{PR}
t_{PHPL}
t_{PF}
t_{ELQV}
V_{IHP}
Program Pulse, P
V_{ILP}

NOTE 5: This Program Enable tranistion must occur after the Program Pulse transition and before the Address Transition.

WAVEFORM DEFINITIONS

Waveform Symbol	Input	Output	Waveform Symbol	Input	Output
═	MUST BE VALID	WILL BE VALID	▩	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
▧	CHANGE FROM H TO L	WILL CHANGE FROM H TO L	>—		HIGH IMPEDANCE
▨	CHANGE FROM L TO H	WILL CHANGE FROM L TO H			

PROGRAMMING INSTRUCTIONS

After the completion of an ERASE operation, every bit in the device is in the "1" state (represented by Output High). Data are entered by programming zeros (Output Low) into the required bits. The words are addressed the same way as in the READ operation. A programmed "0" can only be changed to a "1" by ultraviolet light erasure.

To set the memory up for programming mode, the V_{CC}(E) input (Pin 24) should be raised to +12 V. Programming data is entered in 8-bit words through the data output terminals (DQ0 to DQ7).

The V_{DD} and V_{BB} supply voltages are the same as for the READ operation.

After address and data setup, one program pulse per address is applied to the program input. A program loop is a full pass through all addresses. Total programming time/address, $T_{Ptotal} = N \times t_{PHPL} \geqslant 100$ ms. The required number of program loops (N) is a function of the program pulse width (t_{PHPL}) where: $0.1 \text{ ms} \leqslant t_{PHPL} \leqslant 1.0$ ms; correspondingly, N is: $100 \leqslant N \leqslant 1000$. There must be N successive loops through all 2048 addresses. It is not permitted to apply more than one program pulse in succession to the same address (i.e., N program pulses to an address and then change to the next address to be programmed). At the end of a program sequence the Program Enable (E) falling edge transition must occur before the first address transition, when changing from a PROGRAM to a READ cycle. The program pin should be pulled down to V_{ILP} with an active device, because this pin sources a small amount of current (I_{IPL}) when (E) is at V_{IHW} (12 V) and the program pulse is at V_{ILP}.

EXAMPLE FOR PROGRAMMING

Always use the $T_{Ptotal} = N \times t_{PHPL} \geqslant 100$ ms relationship.

1. All 16,384 bits should be programmed with a 0.2 ms program pulse width.

The minimum number of program loops:

$$N = \frac{T_{Ptotal}}{t_{PHPL}} = \frac{100 \text{ ms}}{0.2 \text{ ms}} = 500.$$

One program loop consists of words 0 to 2047.

2. Words 0 to 200 and 300 to 700 are to be programmed. All other bits are "don't care". The program pulse width is 0.5 ms. The minimum number of program loops, N = 100/0.5 = 200. One program loop consists of words 0 to 2047. The data entered into the "don't care" bits should be all 1s.

3. Same requirements as example 2, but the EPROM is now to be updated to include data for words 850 to 880. The minimum number of program loops is the same as in the previous example, N = 200. One program loop consists of words 0 to 2047. The data entered into the "don't care" bits should be all 1s. Addresses 0 to 200 and 300 to 700 must be reprogrammed with their original data pattern.

ERASING INSTRUCTIONS

The TMS2716/27A16 can be erased by exposure to high intensity shortwave ultraviolet light, with a wavelength of 2537 Å. The recommended integrated dose (i.e., UV-intensity × exposure time) is 12.5 Ws/cm^2. As an example, using the "Model 30-000" UV-Eraser (Turner Designs, Mountain View, CA 94043) the ERASE-time is 30 minutes. The lamps should be used without shortwave filters and the TMS2716/27A16 should be positioned about one inch away from the UV-tubes.

MOTOROLA

MCM2716

MOS

(N-CHANNEL, SILICON-GATE)

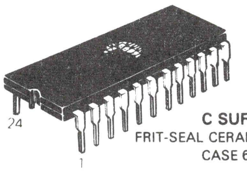
2048 × 8-BIT
UV ERASABLE PROM

2048 × 8-BIT UV ERASABLE PROM

The MCM2716 is a 16,384-bit Erasable and Electrically Reprogrammable PROM designed for system debug usage and similar applications requiring nonvolatile memory that could be reprogrammed periodically. The transparent lid on the package allows the memory content to be erased with ultraviolet light.

For ease of use, the device operates from a single power supply and has a static power-down mode. Pin-for-pin mask programmable ROMs are available for large volume production runs of systems initially using the MCM2716.

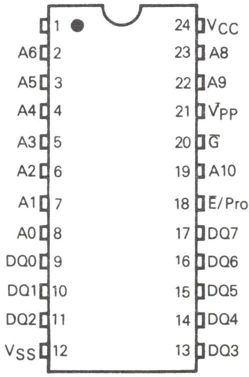
- Single 5 V Power Supply
- Automatic Power-down Mode (Standby)
- Organized as 2048 Bytes of 8 Bits
- TTL Compatible During Read and Program
- Maximum Access Time = 450 ns MCM2716
- Pin Equivalent to Intel's 2716
- Pin Compatible to MCM68A316E
- Output Enable Active Level is User Selectable



C SUFFIX
FRIT-SEAL CERAMIC PACKAGE
CASE 623A

L SUFFIX CERAMIC PACKAGE
ALSO AVAILABLE — CASE 716

PIN ASSIGNMENT

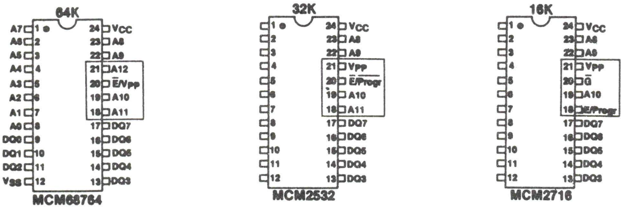

A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
DQ0 9
DQ1 10
DQ2 11
VSS 12
24 VCC
23 A8
22 A9
21 VPP
20 G̅
19 A10
18 E̅/Progr
17 DQ7
16 DQ6
15 DQ5
14 DQ4
13 DQ3

***Pin Names**

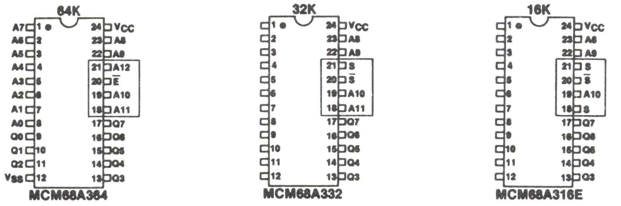
A . . . . Address
DQ . . . . Data Input/Output
E̅/Progr . . . . Chip Enable/Program
G̅ . . . . Output Enable

*New industry standard nomenclature

MOTOROLA'S PIN-COMPATIBLE EPROM FAMILY


64K
A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
DQ0 9
DQ1 10
DQ2 11
VSS 12
24 VCC
23 A8
22 A9
21 A12
20 E̅/VPP
19 A10
18 A11
17 DQ7
16 DQ6
15 DQ5
14 DQ4
13 DQ3
MCM68764
32K
24 VCC
23 A8
22 A9
21 VPP
20 E̅/Progr
19 A10
18 A11
17 DQ7
16 DQ6
15 DQ5
14 DQ4
13 DQ3
MCM2532
16K
24 VCC
23 A8
22 A9
21 VPP
20 G̅
19 A10
18 E̅/Progr
17 DQ7
16 DQ6
15 DQ5
14 DQ4
13 DQ3
MCM2716

MOTOROLA'S PIN-COMPATIBLE ROM FAMILY


64K
A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
Q0 9
Q1 10
Q2 11
VSS 12
24 VCC
23 A8
22 A9
21 A12
20 E̅
19 A10
18 A11
17 Q7
16 Q6
15 Q5
14 Q4
13 Q3
MCM68A364
32K
24 VCC
23 A8
22 A9
21 S
20 S̅
19 A10
18 A11
17 Q7
16 Q6
15 Q5
14 Q4
13 Q3
MCM68A332
16K
24 VCC
23 A8
22 A9
21 S
20 S̅
19 A10
18 S
17 Q7
16 Q6
15 Q5
14 Q4
13 Q3
MCM68A316E

INDUSTRY STANDARD PINOUTS

ABSOLUTE MAXIMUM RATINGS

Rating	Value	Unit
Temperature Under Bias ($V_{PP}=5$ V)	−10 to +80	°C
Operating Temperature Range	0 to +70	°C
Storage Temperature	−65 to +125	°C
All Input or Output Voltages with Respect to V_{SS}	+6 to −0.3	V
V_{PP} Supply Voltage with Respect to V_{SS}	+28 to −0.3	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

MODE SELECTION

Mode	Pin Number					
	9-11, 13-17 DQ	12 V_{SS}	18 $\overline{E}$/Progr	20 $\overline{G}$*	21 V_{PP}	24 V_{CC}
Read	Data Out	V_{SS}	V_{IL}	V_{IL}	V_{CC}*	V_{CC}
Output Disable	High Z	V_{SS}	Don't Care	V_{IH}	V_{CC}*	V_{CC}
Standby	High Z	V_{SS}	V_{IH}	Don't Care	V_{CC}	V_{CC}
Program	Data In	V_{SS}	Pulsed V_{IL} to V_{IH}	V_{IH}	V_{PPH}	V_{CC}
Program Verify	Data Out	V_{SS}	V_{IL}	V_{IL}	V_{PPH}	V_{CC}
Program Inhibit	High Z	V_{SS}	V_{IL}	V_{IH}	V_{PPH}	V_{CC}

*In the Read Mode if $V_{PP} \geq V_{IH}$, then $\overline{G}$ (active low)
$V_{PP} \leq V_{IL}$, then G (active high)

BLOCK DIAGRAM

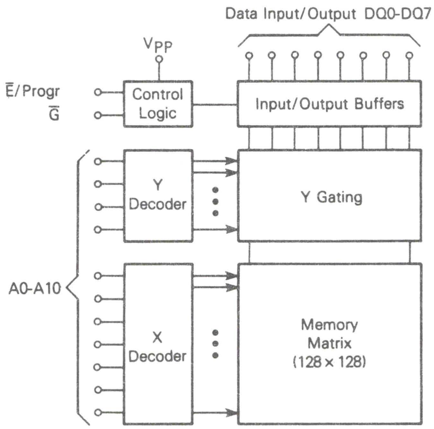
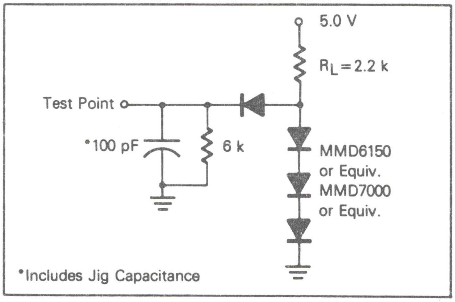

Data Input/Output DQ0-DQ7
V_{PP}
$\overline{E}$/Progr
$\overline{G}$
Control Logic
Input/Output Buffers
Y Decoder
Y Gating
A0-A10
X Decoder
Memory Matrix (128 × 128)

FIGURE 1 — AC TEST LOAD


5.0 V
$R_L = 2.2$ k
Test Point
*100 pF
6 k
MMD6150 or Equiv.
MMD7000 or Equiv.

*Includes Jig Capacitance

CAPACITANCE (f = 1.0 MHz, $T_A = 25°C$, periodically sampled rather than 100% tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance ($V_{in} = 0$ V)	C_{in}	4.0	6.0	pF
Output Capacitance ($V_{out} = 0$ V)	C_{out}	8.0	12	pF

Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = \frac{I\Delta t}{\Delta V}$.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED DC READ OPERATING CONDITIONS

Parameter		Symbol	Min	Nom	Max	Unit
Supply Voltage*	MCM2716	V_{CC} V_{PP}	4.75 4.75	5.0 5.0	5.25 5.25	V
Input High Voltage		V_{IH}	2.0	–	$V_{CC} + 1.0$	V
Input Low Voltage		V_{IL}	−0.1	–	0.8	V

RECOMMENDED DC OPERATING CHARACTERISTICS

Characteristic	Condition	Symbol	MCM2716			Units
			Min	Typ	Max	
Address, $\overline{G}$ and $\overline{E}$/Progr Input Sink Current	$V_{in} = 5.25$ V	I_{in}	–	–	10	μA
Output Leakage Current	$V_{out} = 5.25$ V $\overline{G} = 5.0$ V	I_{LO}	–	–	10	μA
V_{CC} Supply Current (Standby) 2716	$\overline{E}$/Progr = V_{IH} $\overline{G} = V_{IL}$	I_{CC1}	–	–	25	mA
V_{CC} Supply Current (Active) 2716 (Outputs Open)	$\overline{G}$ = $\overline{E}$/Progr = V_{IL}	I_{CC2}	–	–	100	mA
V_{PP} Supply Current*	$V_{PP} = 5.25$ V	I_{PP1}	–	–	5.0	mA
Output Low Voltage	$I_{OL} = 2.1$ mA	V_{OL}	–	–	0.45	V
Output High Voltage	$I_{OH} = -400$ μA	V_{OH}	2.4	–	–	V

***V_{CC} must be applied simultaneously or prior to V_{PP}. V_{CC} must also be switched off simultaneously with or after V_{PP}. With V_{PP} connected directly to V_{CC} during the read operation, the supply current would then be the sum of I_{PP1} and I_{CC}.**

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

Input Pulse Levels .... 0.8 Volt and 2.2 Volts

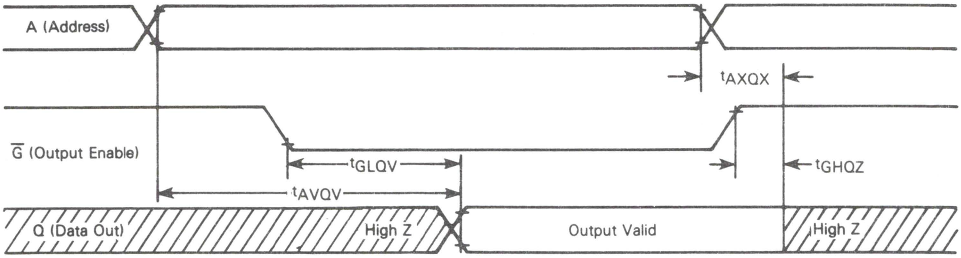
Input Rise and Fall Times .... 20 ns

Input and Output Timing Levels .... 2.0 and 0.8 Volts

Output Load .... See Figure 1

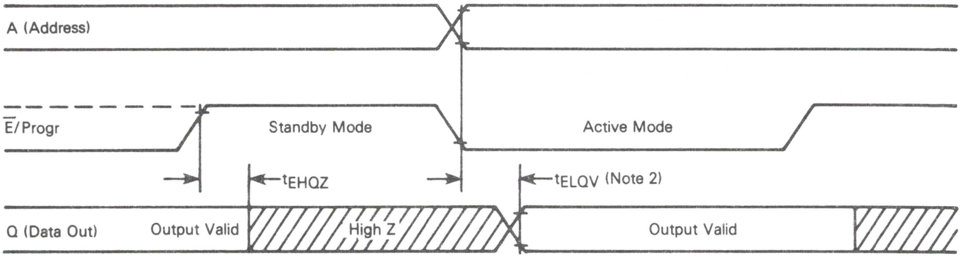
Characteristic	Condition	Symbol	MCM2716		Units
			Min	Max	
Address Valid to Output Valid	$\overline{E}$/Progr = $\overline{G}$ = V_{IL}	t_{AVQV}	–	450	ns
$\overline{E}$/Progr to Output Valid	(Note 2)	t_{ELQV}	–	450	
Output Enable to Output Valid	$\overline{E}$/Progr = V_{IL}	t_{GLQV}	–	150	
$\overline{E}$/Progr to High Z Output	–	t_{EHQZ}	0	100	
Output Disable to High Z Output	$\overline{E}$/Progr = V_{IL}	t_{GHQZ}	0	100	
Data Hold from Address	$\overline{E}$/Progr = G = V_{IL}	t_{AXDX}	0	–	

READ MODE TIMING DIAGRAMS ($\overline{E}$/Progr $= V_{IL}$)


A (Address)
t_{AXQX}
$\overline{G}$ (Output Enable)
t_{GLQV}
t_{AVQV}
t_{GHQZ}
Q (Data Out)
High Z
Output Valid
High Z

STANDBY MODE (Output Enable $= V_{IL}$)

Standby Mode ($\overline{E}$/Progr $= V_{IH}$)


A (Address)
$\overline{E}$/Progr
Standby Mode
Active Mode
t_{EHQZ}
t_{ELQV} (Note 2)
Q (Data Out)
Output Valid
High Z
Output Valid

NOTE 2: t_{ELQV} is referenced to $\overline{E}$/Progr or stable address, whichever occurs last.

DC PROGRAMMING CONDITIONS AND CHARACTERISTICS

($T_A = 25°C \pm 5°C$)

RECOMMENDED PROGRAMMING OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}, V_{PPL} V_{PPH}	4.75 24	5.0 25	5.25 26	V
Input High Voltage for Data	V_{IH}	2.2	–	V_{CC} + 1	V
Input Low Voltage for Data	V_{IL}	–0.1	–	0.8	V

PROGRAMMING OPERATION DC CHARACTERISTICS

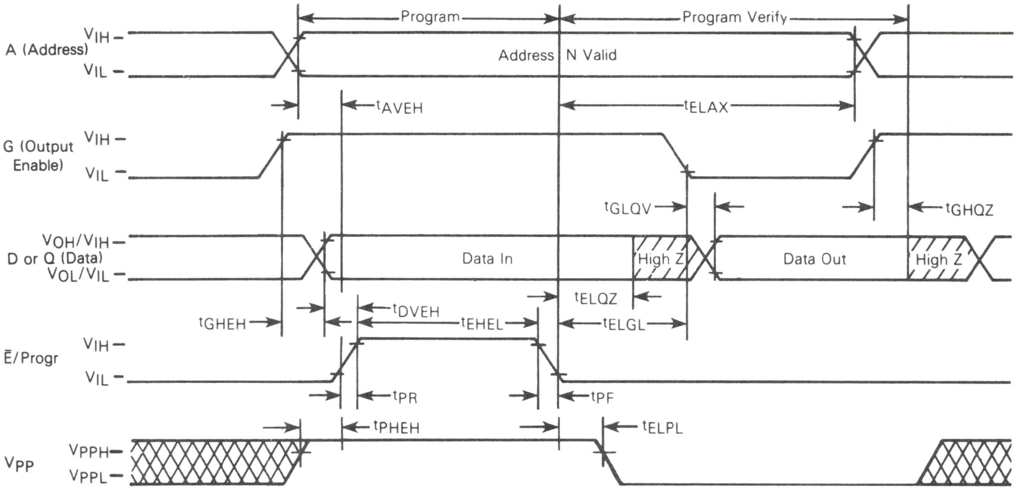
Characteristic	Condition	Symbol	Min	Typ	Max	Unit
Address, $\overline{G}$ and $\overline{E}$/Progr Input Sink Current	$V_{in} = 5.25$ V/0.45V	I_{LI}	–	–	10	μA
V_{PP} Programming Pulse Supply Current ($V_{PP} = 25$ V ± 1 V)	$\overline{E}$/Progr $= V_{IH}$	I_{PP2}	–	–	30	mA
V_{CC} Supply Current (Outputs Open)	–	I_{CC}	–	–	160	mA

AC PROGRAMMING OPERATING CONDITIONS AND CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Address Setup Time	t_{AVEH}	2.0	–	μs
Output Enable High to Program Pulse	t_{GHEH}	2.0	–	μs
Data Setup Time	t_{DVEH}	2.0	–	μs
Address Hold Time	t_{ELAX}	2.0	–	μs
Output Enable Hold Time	t_{ELGL}	2.0	–	μs
Data Hold Time	t_{ELQZ}	2.0	–	μs
V_{PP} Setup Time	t_{PHEH}	0	–	ns
V_{PP} to Enable Low Time	t_{ELPL}	0	–	ns
Output Disable to High Z Output	t_{GHQZ}	0	150	ns
Output Enable to Valid Data ($\overline{E}$/Progr $= V_{IL}$)	t_{GLQV}	–	150	ns
Program Pulse Width	t_{EHEL}	1*	55	ms
Program Pulse Rise Time	t_{PR}	5	–	ns
Program Pulse Fall Time	t_{PF}	5	–	ns

*If shorter than 45 ms (min) pulses are used, the same number of pulses should be applied after the specific data has been verified to ensure that good programming levels have been written.

PROGRAMMING OPERATION TIMING DIAGRAM



PROGRAMMING INSTRUCTIONS

Before programming, the memory should be submitted to a full ERASE operation to ensure every bit in the device is in the "1" state (represented by Output High). Data are entered by programming zeros (Output Low) into the required bits. The words are addressed the same way as in the READ operation. A programmed "0" can only be changed to a "1" by ultraviolet light erasure.

To set the memory up for Program Mode, the V_{PP} input (Pin 21) should be raised to +25 V. The V_{CC} supply voltage is the same as for the Read operation and $\overline{\text{G}}$ is at V_{IH}. Programming data is entered in 8-bit words through the data out (DQ) terminals. Only "0 s" will be programmed when "0's" and "1 s" are entered in the 8-bit data word.

After address and data setup, a program pulse (V_{IL} to V_{IH}) is applied to the $\overline{\text{E}}$/Progr input. A program pulse is applied to each address location to be programmed. To minimize programming time, a 2 ms pulse width is recommended. The maximum program pulse width is 55 ms; therefore, programming must not be attempted with a dc signal applied to the $\overline{\text{E}}$/Progr input.

Multiple MCM2716s may be programmed in parallel by connecting together like inputs and applying the program pulse to the $\overline{\text{E}}$/Progr inputs. Different data may be programmed into multiple MCM2716s connected in parallel by using the PROGRAM INHIBIT mode. Except for the $\overline{\text{E}}$/Progr pin, all like inputs (including Output Enable) may be common.

The PROGRAM VERIFY mode with V_{PP} at 25 V is used to determine that all programmed bits were correctly programmed.

READ OPERATION

After access time, data is valid at the outputs in the READ mode. With stable system addresses, effectively faster access time can be obtained by gating the data onto the bus with Output Enable.

The Standby mode is available to reduce active power dissipation. The outputs are in the high impedance state when the $\overline{\text{E}}$/Progr input pin is high (V_{IH}) independent of the Output Enable input.

ERASING INSTRUCTIONS

The MCM2716 can be erased by exposure to high intensity shortwave ultraviolet light, with a wavelength of 2537 angstroms. The recommended integrated dose (i.e., UV-intensity X exposure time) is 15 Ws/cm^2. As an example, using the "Model 30-000" UV-Eraser (Turner Designs, Mountain View, CA 94043) the ERASE-time is 36 minutes. The lamps should be used without shortwave filters and the MCM2716 should be positioned about one inch away from the UV-tubes.

RECOMMENDED OPERATING PROCEDURES

After erasure and reprogramming of the EPROM, it is recommended that the quartz window be covered with an opaque self-adhesive cover. It is important that the self-adhesive cover not leave any residue on the quartz if it is removed to allow another erasure.

TIMING PARAMETER ABBREVIATIONS

t X X X X

signal name from which interval is defined

transition direction for first signal

signal name to which interval is defined

transition direction for second signal

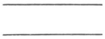
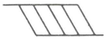
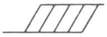
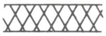
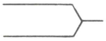
The transition definitions used in this data sheet are:

H = transition to high
L = transition to low
V = transition to valid
X = transition to invalid or don't care
Z = transition to off (high impedance)

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WAVEFORMS

Waveform Symbol	Input	Output
	Must Be Valid	Will Be Valid
	Change From H to L	Will Change From H to L
	Change From L to H	Will Change From L to H
	Don't Care: Any Change Permitted	Changing: State Unknown
		High Impedance

MOTOROLA

MCM2532

4096 × 8-BIT UV ERASABLE PROM

The MCM2532 is a 32,768-bit Erasable and Electrically Reprogrammable PROM designed for system debug usage and similar applications requiring nonvolatile memory that could be reprogrammed periodically. The transparent window in the package allows the memory content to be erased with ultraviolet light.

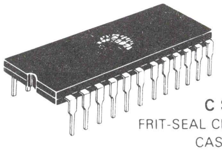
For ease of use, the device operates from a single power supply and has static power-down mode. Pin-for-pin compatible mask programmable ROMs are available for large volume production runs of systems initially using the MCM2532.

- Single +5 V Power Supply
- Organized as 4096 Bytes of 8 Bits
- Automatic Power-Down Mode (Standby)
- Fully Static Operation (No Clocks)
- TTL Compatible During Both Read and Program
- Maximum Access Time = 450 ns MCM2532
- Pin Compatible with MCM68A332 Mask Programmable ROMs
- Power MCM2532
  - Active — 150 mA Max
  - Standby — 25 mA Max

MOS

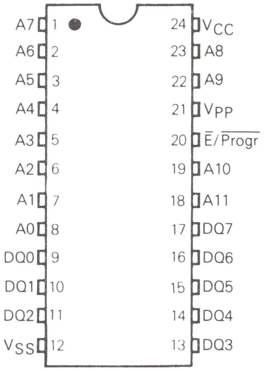
(N-CHANNEL, SILICON-GATE)

4096 × 8-BIT
UV ERASABLE PROM



C SUFFIX
FRIT-SEAL CERAMIC PACKAGE
CASE 623A-02

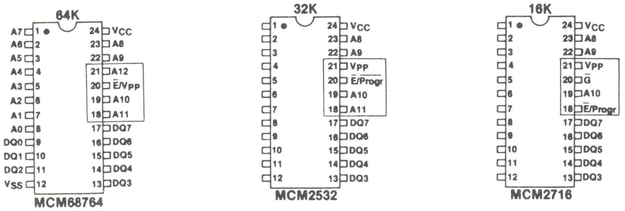
PIN ASSIGNMENT


A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
DQ0 9
DQ1 10
DQ2 11
VSS 12
24 VCC
23 A8
22 A9
21 VPP
20 E/Progr
19 A10
18 A11
17 DQ7
16 DQ6
15 DQ5
14 DQ4
13 DQ3

*PIN NAMES	
A	Address
DQ	Data Input/Output
E/Progr	Dual Function Enable (Power-Down/Program Pulse)

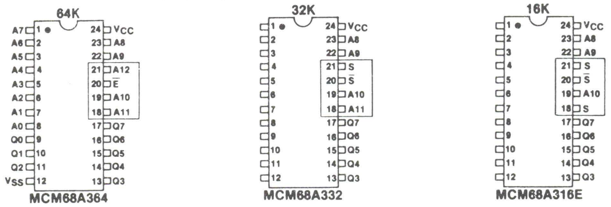
*New Industry standard nomenclature

MOTOROLA'S PIN-COMPATIBLE EPROM FAMILY


64K
32K
16K
21 A12
20 E/Vpp
19 A10
18 A11
21 VPP
20 E/Progr
19 A10
18 A11
21 VPP
20 G
19 A10
18 E/Progr

MCM68764 MCM2532 MCM2716

MOTOROLA'S PIN-COMPATIBLE ROM FAMILY


64K
32K
16K
21 A12
20 E
19 A10
18 A11
21 S
20 S
19 A10
18 A11
21 S
20 S
19 A10
18 S

MCM68A364 MCM68A332 MCM68A316E

INDUSTRY STANDARD PINOUTS

DS-9816/4-80

ABSOLUTE MAXIMUM RATINGS

Rating	Value	Unit
Temperature Under Bias ($V_{PP}=5$ V)	− 10 to + 80	°C
Operating Temperature Range	0 to + 70	°C
Storage Temperature	− 65 to + 125	°C
All Input/Output Voltages with Respect to V_{SS}	+ 6 to − 0.3	V
V_{PP} Supply Voltage with Respect to V_{SS}	+ 28 to − 0.3	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

MODE SELECTION

Mode	Pin Number				
	9-11, 13-17 DQ	12 V_{SS}	20 $\overline{E}/\overline{Progr}$	21 V_{PP}	24 V_{CC}
Read	Data Out	V_{SS}	V_{IL}	5 V	V_{CC}
Output Disable	High Z	V_{SS}	V_{IH}	5 to 25 V	V_{CC}
Standby	High Z	V_{SS}	V_{IH}	5 V	V_{CC}
Program	Data In	V_{SS}	Pulsed V_{IH} to V_{IL}	V_{PPH}	V_{CC}
Program Verify	Data Out	V_{SS}	V_{IL}	5 V	V_{CC}
Program Inhibit	High Z	V_{SS}	V_{IH}	V_{PPH}	V_{CC}

BLOCK DIAGRAM

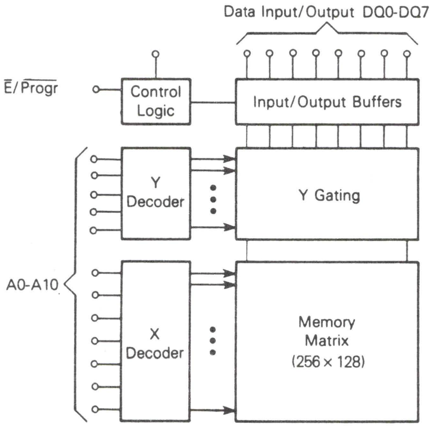
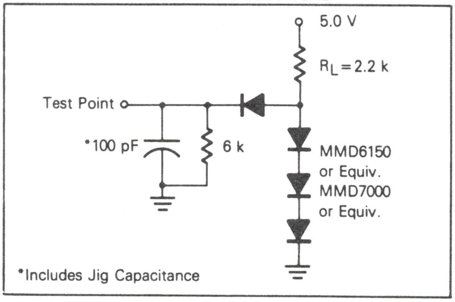

Data Input/Output DQ0-DQ7
E/Progr
Control Logic
Input/Output Buffers
Y Decoder
Y Gating
A0-A10
X Decoder
Memory Matrix (256 × 128)

FIGURE 1 — AC TEST LOAD


5.0 V
RL = 2.2 k
Test Point
*100 pF
6 k
MMD6150 or Equiv.
MMD7000 or Equiv.

*Includes Jig Capacitance

CAPACITANCE (f = 1.0 MHz, $T_A = 25°C$, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance ($V_{in} = 0$ V)	C_{in}	4.0	6.0	pF
Output Capacitance ($V_{out} = 0$ V)	C_{out}	8.0	12	pF

Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta_t / \Delta V$.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Fully operating voltage and temperature range unless otherwise noted)

RECOMMENDED DC OPERATING CONDITIONS

Parameter		Symbol	Min	Typ	Max	Unit
Supply Voltage*	MCM2532	V_{CC} V_{PP}	4.75 4.75	5.0 5.0	5.25 5.25	V
Input High Voltage		V_{IH}	2.2	–	$V_{CC} + 1.0$	V
Input Low Voltage		V_{IL}	−0.1	–	0.65	V

RECOMMENDED DC OPERATING CHARACTERISTICS

Characteristic		Condition	Symbol	Min	Max	Unit
Address and $\overline{E}$ Input Sink Current		$V_{in} = 5.25$ V	I_{in}	–	10	μA
Output Leakage Current		$V_{out} = 5.25$ V	I_{LO}	–	10	μA
V_{CC} Supply Current* (Standby)	MCM2532	$\overline{E} = V_{IH}$	I_{CC1}	–	25	mA
V_{CC} Supply Current* (Active)	MCM2532	$\overline{E} = V_{IL}$	I_{CC2}	–	150	mA
V_{PP} Supply Current*		$V_{PP} = 5.25$ V	I_{PP1}	–	5.0	mA
Output Low Voltage		$I_{OL} = 2.1$ mA	V_{OL}	–	0.45	V
Output High Voltage		$I_{OH} = -400$ μA	V_{OH}	2.4	–	V

*V_{CC} must be applied simultaneously or prior to V_{PP}. V_{CC} must also be switched off simultaneously with or after V_{PP}. With V_{PP} connected directly to V_{CC} during the read operation, the supply current would be the sum of I_{PP1} and I_{CC}.

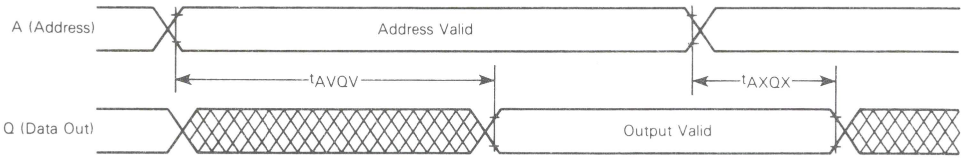
AC READ OPERATING CONDITIONS AND CHARACTERISTICS

(Full Operating Voltage and Temperature Range Unless Otherwise Noted)

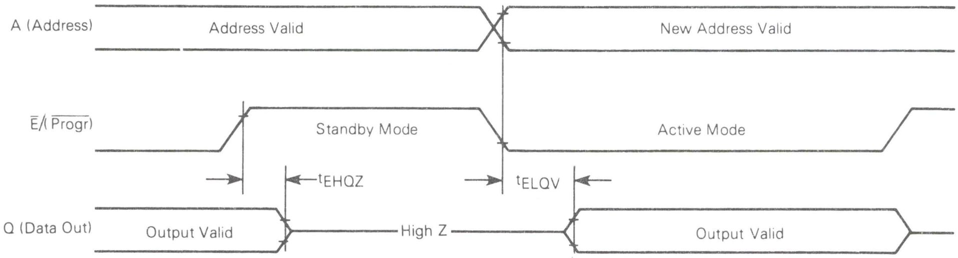
Input Pulse Levels. . . . . 0.65 Volt and 2.2 Volts
Input Rise and Fall Times. . . . . 20 ns
Input and Output Timing Levels. . . . . 0.8 and 2.0 Volts
Output Load. . . . . See Figure 1

Characteristic	Symbol	Min	Max	Unit
Address Valid to Output Valid ($\overline{E}/\overline{Progr} = V_{IL}$)	t_{AVQV}	–	450	ns
$\overline{E}$ to Output Valid	t_{ELQV}	–	450	ns
$\overline{E}$ to High Z Output	t_{EHQZ}	0	100	ns
Data Hold from Address ($\overline{E} = V_{IL}$)	t_{AXQX}	0	–	ns

READ MODE TIMING DIAGRAMS ($\overline{E}=V_{IL}$)


A (Address)
Address Valid
t_{AVQV}
t_{AXQX}
Q (Data Out)
Output Valid

STANDBY MODE


A (Address)
Address Valid
New Address Valid
$\overline{E}/\overline{Progr}$
Standby Mode
Active Mode
t_{EHQZ}
t_{ELQV}
Q (Data Out)
Output Valid
High Z
Output Valid

DC PROGRAMMING CONDITIONS AND CHARACTERISTICS

($T_A=25°C \pm 5°C$)

RECOMMENDED PROGRAMMING OPERATION CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}, V_{PPL} V_{PPH}	4.75 24	5.0 25	5.25 26	V
Input High Voltage for Data	V_{IH}	2.2	–	$V_{CC}+1$	V
Input Low Voltage for Data	V_{IL}	−0.1	–	0.65	V

*V_{CC} must be applied simultaneously or prior to V_{PP}. V_{CC} must also be switched off simultaneously with or after V_{PP}. The device must not be inserted into or removed from a board with V_{PP} at +25 V. V_{PP} must not exceed the +26 V maximum specifications.

PROGRAMMING OPERATION DC CHARACTERISTICS

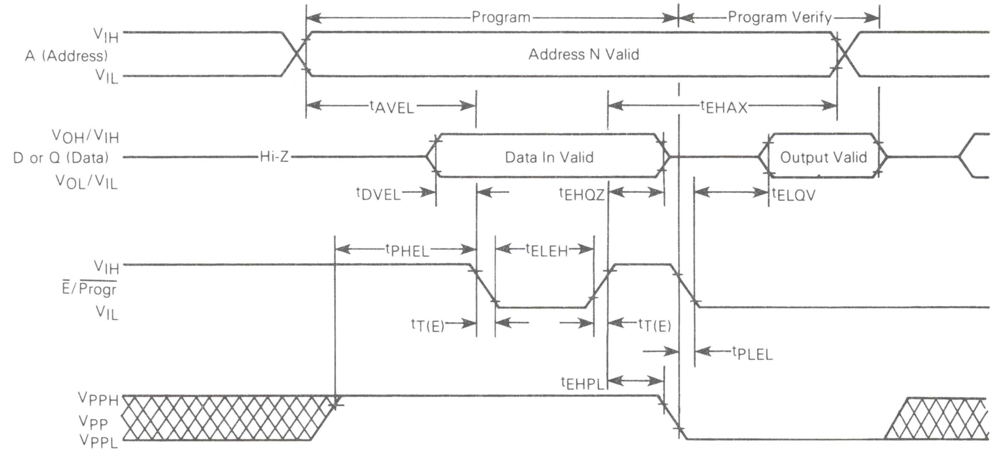
Characteristic	Condition	Symbol	Min	Typ	Max	Unit
Address and $\overline{E}/\overline{Progr}$ Input Sink Current	$V_{in}=5.25$ V/0.45 V	I_{LI}	–	–	10	μA
V_{PP} Programming Pulse Supply Current ($V_{PP}=25$ V ±1 V)	$\overline{E}/\overline{Progr}=V_{IL}$	I_{PP2}	–	–	30	mA
V_{CC} Supply Current – MCM2532	–	I_{CC}	–	–	160	mA

AC PROGRAMMING OPERATING CONDITIONS AND CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Address Setup Time	t_{AVEL}	2.0	–	μs
V_{PP} Setup Time	t_{PHEL}	0	–	ns
Data Setup Time	t_{DVEL}	2.0	–	μs
Address Hold Time	t_{EHAX}	2.0	–	μs
V_{PP} to Enable Low Time	t_{PLEL}	0	–	ns
Data Hold Time	t_{EHQZ}	2.0	–	μs
V_{PP} Hold Time	t_{EHPL}	0	–	ns
Enable (Program) Active Time	t_{ELEH}	1*	55	ms
Enable ($\overline{E}/\overline{Progr}$) Pulse Transition Time	$t_{T(PE)}$	5	–	ns
V_{PP} Rise and Fall Time from 5 to 25 V	t_R, t_F	0.5	2	μs

*If shorter than 45 ms (min) pulses are used, the same number of pulses should be applied after the specific data has been verified. To ensure that good programming levels have been written, see special programming.

PROGRAMMING OPERATION TIMING DIAGRAM



PROGRAMMING INSTRUCTIONS

Before programming, the memory should be submitted to a full ERASE operation to ensure every bit in the device is in the "1" state (represented by Output High). Data are entered by programming zeros (Output Low) into the required bits. The words are addressed the same way as in the READ operation. A programmed "0" can only be changed to a "1" by ultraviolet light erasure.

To set the memory up for PROGRAM mode, the V_{PP} input (pin 21) should be raised to +25 V. The V_{CC} supply voltage is the same as for the READ operation. Programming data is entered in 8-bit words through the data out (DQ) terminals while $\bar{E}/\overline{\text{Progr}}$ is high. Only "0's" will be programmed when "0's" and "1's" are entered in the data word.

After address and data setup, a 50 ms program pulse (V_{IH} to V_{IL}) is applied to the $\bar{E}/\overline{\text{Progr}}$ input. A program pulse is applied to each address location to be programmed. The maximum program pulse width is 55 ms; therefore, programming must not be attempted with a dc signal applied to the $\bar{E}/\overline{\text{Progr}}$ input.

Multiple MCM2532s may be programmed in parallel with the same data by connecting together like inputs and applying the program pulse to the $\bar{E}/\overline{\text{Progr}}$ inputs. Different data may be programmed into multiple MCM2532s connected in parallel by using the PROGRAM INHIBIT mode. Except for the $\bar{E}/\overline{\text{Progr}}$ pin, all like inputs may be common.

PROGRAM VERIFY for the MCM2532 is the read operation.

SPECIAL PROGRAMMING

The MCM2532 can be programmed with pulses as short as 2 milliseconds to minimize programming time. This can represent considerable cost savings when programming a large number of devices.

To take full advantage of the shorter programming pulses, an iterative algorithm is recommended. Actual programming algorithms can be varied provided the following conditions are met: 1) Program pulses will be applied one to each sequential location (no multiple pulses at one location); and 2) after the part programs successfully, five additional 2 millisecond pulses should be applied at each location.

Using this iterative method, the programming time per location becomes 12 milliseconds minimum to 50 milliseconds maximum.

READ OPERATION

After access time, data is valid at the outputs in the READ mode.

ERASING INSTRUCTIONS

The MCM2532 can be erased by exposure to high intensity shortwave ultraviolet light, with a wave-length of 2537 angstroms. The recommended integrated does (i.e., UV-intensity X exposure time) is 15 Ws/cm^2. As an example, using the "Model 30-000" UV-Eraser Turner Designs, Mountain View, CA 94043) the ERASE-time is 36 minutes. The lamps should be used without shortwave filters and the MCM2532 should be positioned about one inch away from the UV-tubes.

RECOMMENDED OPERATING PROCEDURES

After erasure and reprogramming of the EPROM, it is recommended that the quartz window be covered with an opaque self-adhesive cover. It is important that the self-adhesive cover not leave any residue on the quartz if it is removed to allow another erasure.

TIMING PARAMETER ABBREVIATIONS

t X X X X

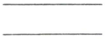
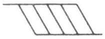
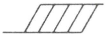
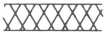
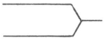
signal name from which interval is defined
transition direction for first signal
signal name to which interval is defined
transition direction for second signal

The transition definitions used in this data sheet are:
H = transition to high
L = transition to low
V = transition to valid
X = transition to invalid or don't care
Z = transition to off (high impedance)

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WAVEFORMS

Waveform Symbol	Input	Output
	Must Be Valid	Will Be Valid
	Change From H to L	Will Change From H to L
	Change From L to H	Will Change From L to H
	Don't Care: Any Change Permitted	Changing: State Unknown
		High Impedance

MOTOROLA

MCM68764

64K-BIT UV ERASABLE PROM

The MCM68764 is a 65,536-bit Erasable and Electrically Reprogrammable PROM designed for system debug usage and similar applications requiring nonvolatile memory that could be reprogrammed periodically, or for replacing 64K ROMs for fast turnaround time. The transparent window on the package allows the memory content to be erased with ultraviolet light.

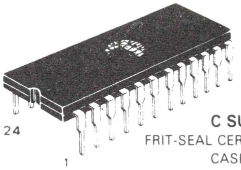
For ease of use, the device operates from a single power supply and has a static power-down mode. Pin-for-pin mask programmable ROMs are available for large volume production runs of systems initially using the MCM68764.

- Single +5 V Power Supply
- Automatic Power-down Mode (Standby) with Chip Enable
- Organized as 8192 Bytes of 8 Bits
- Power Dissipation
  120 mA Active Maximum
  25 mA Standby Maximum
- Fully TTL Compatible
- Maximum Access Time = 450 ns MCM68764
  350 ns MCM68764-35
- Standard 24-Pin DIP for EPROM Upgradability
- Pin Compatible to MCM68A364 Mask Programmable ROM

MOS

(N-CHANNEL, SILICON-GATE)

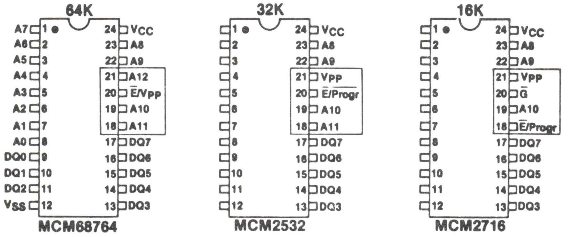
8192 × 8-BIT
UV ERASABLE
PROGRAMMABLE READ
ONLY MEMORY



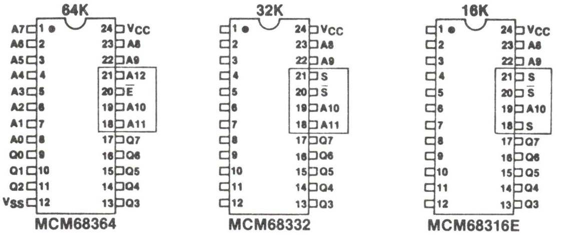
C SUFFIX
FRIT-SEAL CERAMIC PACKAGE
CASE 623A

L SUFFIX CERAMIC PACKAGE
ALSO AVAILABLE — CASE 716

MOTOROLA'S PIN-COMPATIBLE EPROM FAMILY


64K
A7 1 24 VCC
A6 2 23 A8
A5 3 22 A9
A4 4 21 A12
A3 5 20 E/Vpp
A2 6 19 A10
A1 7 18 A11
A0 8 17 DQ7
DQ0 9 16 DQ6
DQ1 10 15 DQ5
DQ2 11 14 DQ4
VSS 12 13 DQ3
MCM68764
32K
21 Vpp
20 E/Progr
19 A10
18 A11
MCM2532
16K
21 Vpp
20 G
19 A10
18 E/Progr
MCM2716

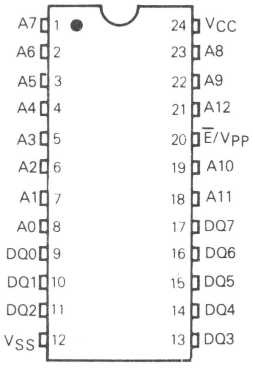
MOTOROLA'S PIN-COMPATIBLE ROM FAMILY


64K
A7 1 24 VCC
A6 2 23 A8
A5 3 22 A9
A4 4 21 A12
A3 5 20 E
A2 6 19 A10
A1 7 18 A11
A0 8 17 Q7
Q0 9 16 Q6
Q1 10 15 Q5
Q2 11 14 Q4
VSS 12 13 Q3
MCM68364
32K
21 S
20 S
19 A10
18 A11
MCM68332
16K
21 S
20 S
19 A10
18 S
MCM68316E

INDUSTRY STANDARD PINOUTS

AA00090-2

PIN ASSIGNMENT


A7 1 24 VCC
A6 2 23 A8
A5 3 22 A9
A4 4 21 A12
A3 5 20 E/VPP
A2 6 19 A10
A1 7 18 A11
A0 8 17 DQ7
DQ0 9 16 DQ6
DQ1 10 15 DQ5
DQ2 11 14 DQ4
VSS 12 13 DQ3

Pin Names	
A	Address
DQ	Data Input/Output
$\overline{E}$/V_{PP}	Chip Enable/Program

DS-9815R2/4-82

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Value	Unit
Temperature Under Bias	−10 to +80	°C
Operating Temperature Range	0 to +70	°C
Storage Temperature	−65 to +125	°C
All Input or Output Voltages with Respect to V_{SS}	+6 to −0.3	V
V_{PP} Supply Voltage with Respect to V_{SS}	+28 to −0.3	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

MODE SELECTION

Mode	Pin Number			
	9-11, 13-17, DQ	12 V_{SS}	20 $\overline{E}/V_{PP}$	24 V_{CC}
Read	Data out	V_{SS}	V_{IL}	V_{CC}
Output Disable	High-Z	V_{SS}	V_{IH}	V_{CC}
Standby	High-Z	V_{SS}	V_{IH}	V_{CC}
Program	Data in	V_{SS}	Pulsed V_{ILP} to V_{IHP}	V_{CC}

BLOCK DIAGRAM

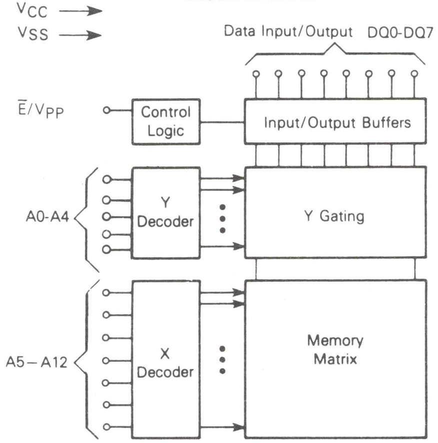
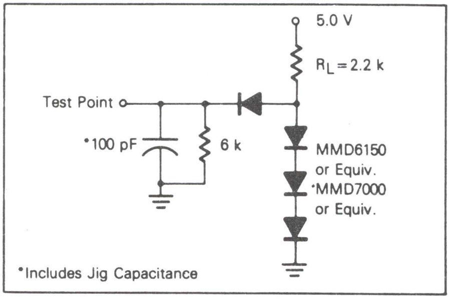

VCC
VSS
Data Input/Output DQ0-DQ7
E/VPP
Control Logic
Input/Output Buffers
A0-A4
Y Decoder
Y Gating
A5–A12
X Decoder
Memory Matrix

FIGURE 1 — AC TEST LOAD


5.0 V
RL = 2.2 k
Test Point
*100 pF
6 k
MMD6150 or Equiv.
*MMD7000 or Equiv.

*Includes Jig Capacitance

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

CAPACITANCE (f = 1.0 MHz, $T_A = 25°C$, $V_{CC} = 5$ V periodically sampled rather than 100% tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance ($V_{in} = 0$ V) Except $\overline{E}/V_{PP}$	C_{in}	4.0	6.0	pF
Input Capacitance $\overline{E}/V_{PP}$	C_{in}	60	100	pF
Output Capacitance ($V_{out} = 0$ V)	C_{out}	8.0	12	pF

Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta_t/\Delta V$.

RECOMMENDED DC OPERATING CONDITIONS

Parameter		Symbol	Min	Nom	Max	Unit
Supply Voltage	MCM68764, MCM68764-35	V_{CC}	4.75	5.0	5.25	V
Input High Voltage		V_{IH}	2.0	–	$V_{CC} + 1.0$	V
Input Low Voltage		V_{IL}	−0.1	–	0.8	V

RECOMMENDED DC OPERATING CHARACTERISTICS

Characteristic	Condition	Symbol	MCM68764			Units
			Min	Typ	Max	
Address Input Sink Current	$V_{in} = 5.25$ V	I_{in}	–	–	10	μA
Output Leakage Current	$V_{out} = 5.25$ V	I_{LO}	–	–	10	μA
$\overline{E}/V_{PP}$ Input Sink Current	$\overline{E}/V_{PP} = 0.4$	I_{EL}	–	–	100	μA
	$\overline{E}/V_{PP} = 2.4$	$I_{EH} = I_{PL}$	–	–	400	μA
V_{CC} Supply Current (Standby) MCM68764	$\overline{E}/V_{PP} = V_{IH}$	I_{CC1}	–	–	25	mA
V_{CC} Supply Current (Standby) MCM68764-35	$\overline{E}/V_{PP} = V_{IH}$	I_{CC1}	–	–	25	mA
V_{CC} Supply Current (Active) MCM68764 (Outputs Open)	$\overline{E}/V_{PP} = V_{IL}$	I_{CC2}	–	–	120	mA
V_{CC} Supply Current (Active) MCM68764-35 (Outputs Open)	$\overline{E}/V_{PP} = V_{IL}$	I_{CC2}	–	–	160	mA
Output Low Voltage	$I_{OL} = 2.1$ mA	V_{OL}	–	–	0.45	V
Output High Voltage	$I_{OH} = -400$ μA	V_{OH}	2.4	–	–	V

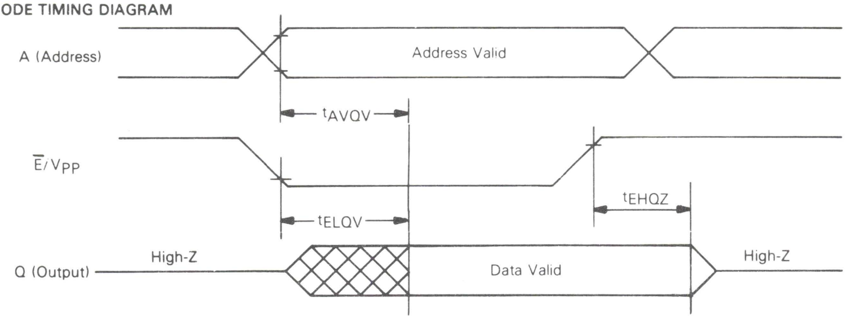
AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

Input Pulse Levels ....0.8 Volt and 2.2 Volts
Input Rise and Fall Times ....20 ns
Input Timing Levels ....1.0 and 2 Volts
Output Timing Levels..................................0.8 Volt and 2 Volts
Output Load ....See Figure 1

Characteristic	Condition	Symbol	MCM68764-35		MCM68764		Units
			Min	Max	Min	Max	
Address Valid to Output Valid	$\overline{E} = V_{IL}$	t_{AVQV}	–	350	–	450	ns
Chip Enable to Output Valid	–	t_{ELQV}	–	350	–	450	ns
Chip Enable to Output High Z	–	t_{EHQZ}	0	100	0	100	ns
Data Hold from Address	$\overline{E} = V_{IL}$	t_{AXDX}	0	–	0	–	ns

READ MODE TIMING DIAGRAM



DC PROGRAMMING CONDITIONS AND CHARACTERISTICS

($T_A = 25 \pm 5°C$)

RECOMMENDED PROGRAMMING OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input High Voltage for All Addresses and Data	V_{IH}	2.2	–	$V_{CC}+1$	V
Input Low Voltage for All Addresses and Data	V_{IL}	−0.1	–	0.8	V
Program Pulse Input High Voltage	V_{IHP}	24	25	26	V
Program Pulse Input Low Voltage	V_{ILP}	2.0	V_{CC}	6.0	V

PROGRAMMING OPERATION DC CHARACTERISTICS

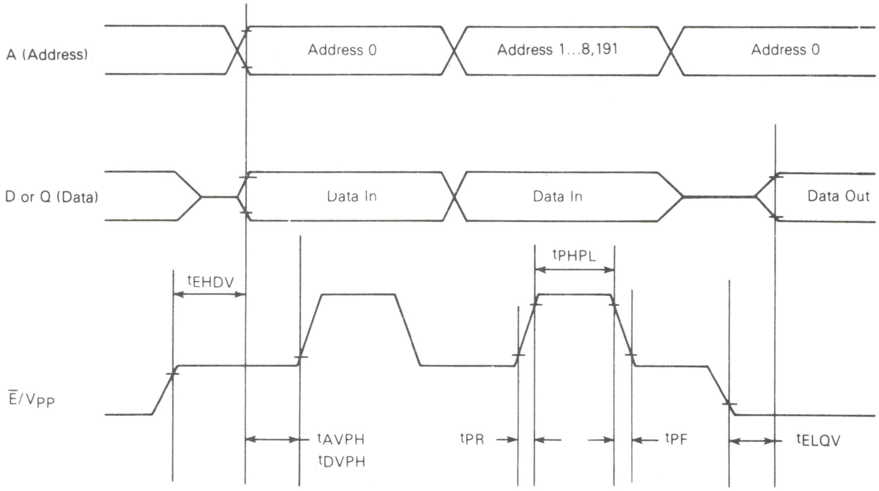
Characteristic	Condition	Symbol	Min	Typ	Max	Unit
Address Input Sink Current	$V_{in} = 5.25$ V	I_{LI}	–	–	10	μA
V_{PP} Program Pulse Supply Current ($V_{PP} = 25$ V ±1 V)	–	I_{PH}	–	–	30	mA
V_{PP} Supply Current ($V_{PP} = 2.4$ V)	–	$I_{PL} = I_{EH}$	–	–	400	μA
V_{CC} Supply Current ($V_{PP} = 5.0$ V)	–	I_{CC}	–	–	160	mA

AC PROGRAMMING OPERATING CONDITIONS AND CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Address Setup Time	t_{AVPH}	2.0	–	μs
Data Setup Time	t_{DVPH}	2.0	–	μs
Chip Enable to Valid Data	t_{ELQV}	450	–	ns
Chip Disable to Data In	t_{EHDV}	2.0	–	μs
Program Pulse Width	t_{PHPL}	1.9	2.1	ms
Program Pulse Rise Time	t_{PR}	0.5	2.0	μs
Program Pulse Fall Time	t_{PF}	0.5	2.0	μs
Cumulative Programming Time Per Word*	t_{CP}	12	50	ms

* Block mode programming must be used. Block mode programming is defined as one program pulse applied to each of the 8,192 address locations in sequence. Multiple blocks are used to accumulate programming time (t_{CP}). If less than 25 two millisecond pulses are required to verify programming, then 5 additional 2 millisecond pulses are required to ensure proper operating margins (i.e., 2 ms + 5 × 2 ms = 12 ms minimum t_{CP}).

PROGRAMMING OPERATION TIMING DIAGRAM



PROGRAMMING INSTRUCTIONS

Before programming, the memory should be submitted to a full erase operation to ensure that every bit is in the "1" state (represented by Output High). Data is entered by programming zeros (Output Low) into the required bits. The words are addressed the same way as in the READ operation. A programmed "0" can only be changed to a "1" by ultraviolet erasure.

To set the memory up for Program Mode, the $\overline{E}/V_{PP}$ input (Pin 20) should be between +2.0 and +6.0 V, which will three-state the outputs and allow data to be setup on the DQ terminals. The V_{CC} voltage is the same as for the Read operation. Only "0's" will be programmed when "0's" and "1's" are entered in the 8-bit data word.

After address and data setup, 25-volt programming pulse (V_{IH} to V_{IHP}) is applied to the $\overline{E}/V_{PP}$ input. The program pulse width is 2 ms and the maximum program pulse amplitude is 26 V.

Multiple MCM68764s may be programmed in parallel by connecting like inputs and applying the program pulse to the $\overline{E}/V_{PP}$ inputs. Different data may be programmed into multiple MCM68764s connected in parallel by selectively applying the programming pulse only to the MCM68764s to be programmed.

READ OPERATION

After access time, data is valid at the outputs in the Read mode. A single input ($\overline{E}/V_{PP}$) enables the outputs and puts the chip in active or standby mode. With $\overline{E}/V_{PP}$ = "0" the outputs are enabled and the chip is in active mode; with $\overline{E}/V_{PP}$ = "1" the outputs are three-stated and the chip is in standby mode. During standby mode, the power dissipation is reduced.

Multiple MCM68764s may share a common data bus with like outputs OR-tied together. In this configuration, only one $\overline{E}/V_{PP}$ input should be low and no other device outputs should be active on the same bus. This will prevent data contention on the bus.

ERASING INSRUCTIONS

The MCM68764 can be erased by exposure to high intensity shortwave ultraviolet light, with a wavelength of 2537 angstroms. The recommended integrated dose (i.e., UV-intensity X exposure time) is 15 Ws/cm^2. As an example, using the "Model 30-000" UV-Eraser (Turner Designs, Mountain View, CA 94043) the ERASE-time is 36 minutes. The lamps should be used without shortwave filters and the MCM68764 should be positioned about one inch away from the UV-tubes.

RECOMMENDED OPERATING PROCEDURES

After erasure and reprogramming of the EPROM, it is recommended that the quartz window be covered with an opaque self-adhesive cover. It is important that the self-adhesive cover not leave any residue on the quartz if it is removed to allow another erasure.

MOTOROLA

MCM68766

Advance Information

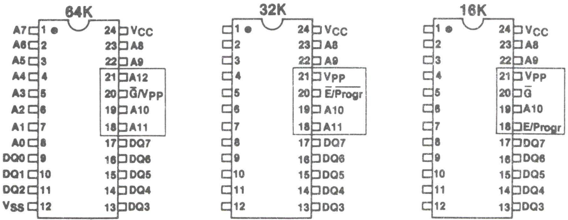
8192 × 8-BIT UV ERASABLE PROM

The MCM68766 is a 65,536-bit Erasable and Electrically Reprogrammable PROM designed for system debug usage and similar applications requiring nonvolatile memory that could be reprogrammed periodically, or for replacing 64K ROMs for fast turnaround time. The transparent window on the package allows the memory content to be erased with ultraviolet light.

For ease of use, the device operates from a single power supply that has an output enable control and is pin-for-pin compatible with the MCM68366 mask programmable ROMs, which are available for large volume production runs of systems initially using the MCM68766.

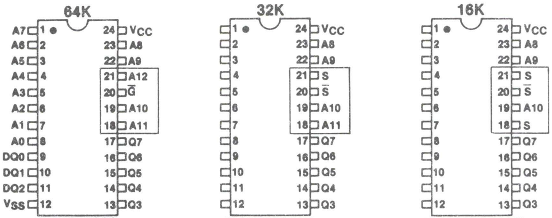
- Single +5 V Power Supply
- Organized as 8192 Bytes of 8 Bits
- Fully TTL Compatible
- Maximum Access Time = 450 ns MCM68766
  350 ns MCM68766-35
- Standard 24-Pin DIP for EPROM Upgradability
- Pin Compatible to MCM68366 Mask Programmable ROM
- Power Dissipation — 160 mA Maximum

MOTOROLA'S PIN-COMPATIBLE EPROM FAMILY


64K
A7 1 24 V$_{CC}$
A6 2 23 A8
A5 3 22 A9
A4 4 21 A12
A3 5 20 $\overline{G}$/V$_{PP}$
A2 6 19 A10
A1 7 18 A11
A0 8 17 DQ7
DQ0 9 16 DQ6
DQ1 10 15 DQ5
DQ2 11 14 DQ4
V$_{SS}$ 12 13 DQ3
32K
1 24 V$_{CC}$
2 23 A8
3 22 A9
4 21 V$_{PP}$
5 20 $\overline{E/Progr}$
6 19 A10
7 18 A11
8 17 DQ7
9 16 DQ6
10 15 DQ5
11 14 DQ4
12 13 DQ3
16K
1 24 V$_{CC}$
2 23 A8
3 22 A9
4 21 V$_{PP}$
5 20 $\overline{G}$
6 19 A10
7 18 E/Progr
8 17 DQ7
9 16 DQ6
10 15 DQ5
11 14 DQ4
12 13 DQ3

MCM68766 MCM2532 MCM2716

MOTOROLA'S PIN-COMPATIBLE ROM FAMILY


64K
A7 1 24 V$_{CC}$
A6 2 23 A8
A5 3 22 A9
A4 4 21 A12
A3 5 20 $\overline{G}$
A2 6 19 A10
A1 7 18 A11
A0 8 17 Q7
DQ0 9 16 Q6
DQ1 10 15 Q5
DQ2 11 14 Q4
V$_{SS}$ 12 13 Q3
32K
1 24 V$_{CC}$
2 23 A8
3 22 A9
4 21 S
5 20 $\overline{S}$
6 19 A10
7 18 A11
8 17 Q7
9 16 Q6
10 15 Q5
11 14 Q4
12 13 Q3
16K
1 24 V$_{CC}$
2 23 A8
3 22 A9
4 21 S
5 20 $\overline{S}$
6 19 A10
7 18 S
8 17 Q7
9 16 Q6
10 15 Q5
11 14 Q4
12 13 Q3

MCM68366 MCM68A332 MCM68A316E

INDUSTRY STANDARD PINOUTS

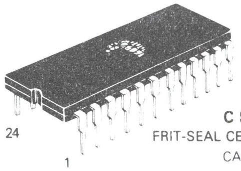
AA90-1A

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MOS

(N-CHANNEL, SILICON-GATE)

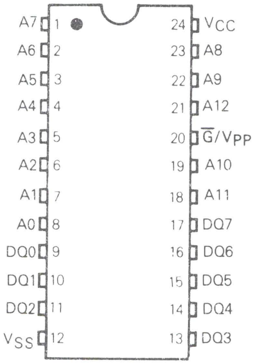
8192 × 8-BIT UV ERASABLE PROGRAMMABLE READ ONLY MEMORY



C SUFFIX
FRIT-SEAL CERAMIC PACKAGE
CASE 623A

L SUFFIX CERAMIC PACKAGE ALSO AVAILABLE — CASE 716

PIN ASSIGNMENT


A7 1 24 V$_{CC}$
A6 2 23 A8
A5 3 22 A9
A4 4 21 A12
A3 5 20 $\overline{G}$/V$_{PP}$
A2 6 19 A10
A1 7 18 A11
A0 8 17 DQ7
DQ0 9 16 DQ6
DQ1 10 15 DQ5
DQ2 11 14 DQ4
V$_{SS}$ 12 13 DQ3

*Pin Names	
A	Address
DQ	Data Input/Output
$\overline{G}$/V$_{PP}$	$\overline{\text{Output Enable}}$/ Program

*New industry standard nomenclature

ABSOLUTE MAXIMUM RATINGS

Rating	Value	Unit
Temperature Under Bias	− 10 to + 80	°C
Operating Temperature Range	0 to + 70	°C
Storage Temperature	− 65 to + 125	°C
All Input or Output Voltages with Respect to V_{SS}	+ 6 to − 0.3	Vdc
V_{PP} Supply Voltage with Respect to V_{SS}	+ 28 to − 0.3	Vdc

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

MODE SELECTION

Mode	Pin Number			
	9-11, 13-17, DQ	12 V_{SS}	20 $\overline{G}/V_{PP}$	24 V_{CC}
Read	Data Out	V_{SS}	V_{IL}	V_{CC}
Output Disable	High-Z	V_{SS}	V_{IH}	V_{CC}
Program	Data In	V_{SS}	Pulsed V_{ILP} to V_{IHP}	V_{CC}

BLOCK DIAGRAM

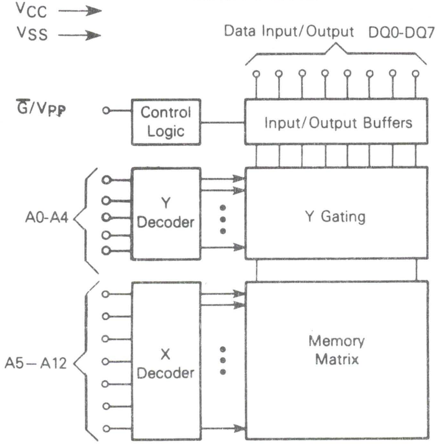
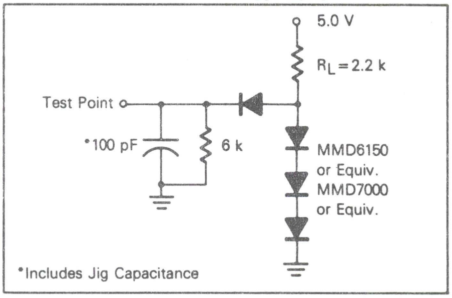

VCC
VSS
Data Input/Output DQ0-DQ7
G/VPP
Control Logic
Input/Output Buffers
A0-A4
Y Decoder
Y Gating
A5–A12
X Decoder
Memory Matrix

FIGURE 1 — AC TEST LOAD


5.0 V
RL = 2.2 k
Test Point
*100 pF
6 k
MMD6150 or Equiv.
MMD7000 or Equiv.

*Includes Jig Capacitance

CAPACITANCE ($f = 1.0$ MHz, $T_A = 25°C$, $V_{CC} = 5$ V periodically sampled rather than 100% tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance ($V_{in} = 0$ V) Except $\overline{G}/V_{PP}$	C_{in}	4.0	6.0	pF
Input Capacitance ($\overline{G}/V_{PP}$)	C_{in}	60	100	pF
Output Capacitance ($V_{out} = 0$ V)	C_{out}	8.0	12	pF

Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta_t/\Delta V$.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage MCM68766 and MCM68766-35	V_{CC}	4.75	5.0	5.25	V
Input High Voltage	V_{IH}	2.0	–	$V_{CC} + 1.0$	V
Input Low Voltage	V_{IL}	−0.1	–	0.8	V

DC OPERATING CHARACTERISTICS

Characteristic	Condition	Symbol	Min	Typ	Max	Units
Address Input Sink Current	$V_{in} = 5.25$ V	I_{in}	–	–	10	μA
Output Leakage Current	$V_{out} = 5.25$ V	I_{LO}	–	–	10	μA
$\overline{G}/V_{PP}$ Input Sink Current	$\overline{G}/V_{PP} = 0.4$ V	I_{GL}	–	–	100	μA
	$\overline{G}/V_{PP} = 2.4$ V	$I_{GH} = I_{PL}$	–	–	400	μA
V_{CC} Supply Current (Outputs Open)	$\overline{G}/V_{PP} = V_{IL}$	I_{CC}	–	–	160	mA
Output Low Voltage	$I_{OL} = 2.1$ mA	V_{OL}	–	–	0.45	V
Output High Voltage	$I_{OH} = -400$ μA	V_{OH}	2.4	–	–	V

AC OPERATING CONDITIONS AND CHARACTERISTICS

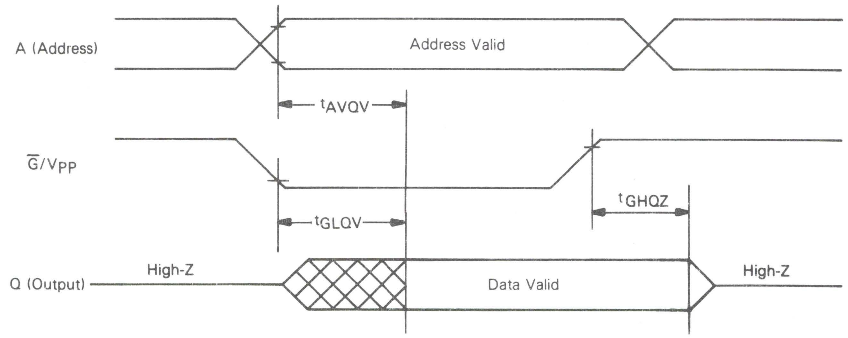
(Full operating voltage and temperature range unless otherwise noted)

Input Pulse Levels....................................0.8 Volt and 2.2 Volts
Input Rise and Fall Times..20 ns

Input Timing Levels.....................................1.0 Volt and 2 Volts
Output Timing Levels...................................0.8 Volt and 2 Volts
Output Load..See Figure 1

Characteristic	Condition	Symbol	MCM68766-35		MCM68766		Units
			Min	Max	Min	Max	
Address Valid to Output Valid	$\overline{G} = V_{IL}$	t_{AVQV}	–	350	–	450	ns
$\overline{G}$ to Output Valid	–	t_{GLQV}	–	150	–	150	ns
$\overline{G}$ to Hi-Z Output	–	t_{GHQZ}	0	100	0	100	ns
Data Hold from Address	$\overline{G} = V_{IL}$	t_{AXDX}	0	–	0	–	ns

READ MODE TIMING DIAGRAM



DC PROGRAMMING CONDITIONS AND CHARACTERISTICS

($T_A = 25 \pm 5°C$)

RECOMMENDED PROGRAMMING OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input High Voltage for All Addresses and Data	V_{IH}	2.2	–	$V_{CC} + 1$	V
Input Low Voltage for All Addresses and Data	V_{IL}	–0.1	–	0.8	V
Program Pulse Input High Voltage	V_{IHP}	24	25	26	V
Program Pulse Input Low Voltage	V_{ILP}	2.0	V_{CC}	6.0	V

PROGRAMMING OPERATION DC CHARACTERISTICS

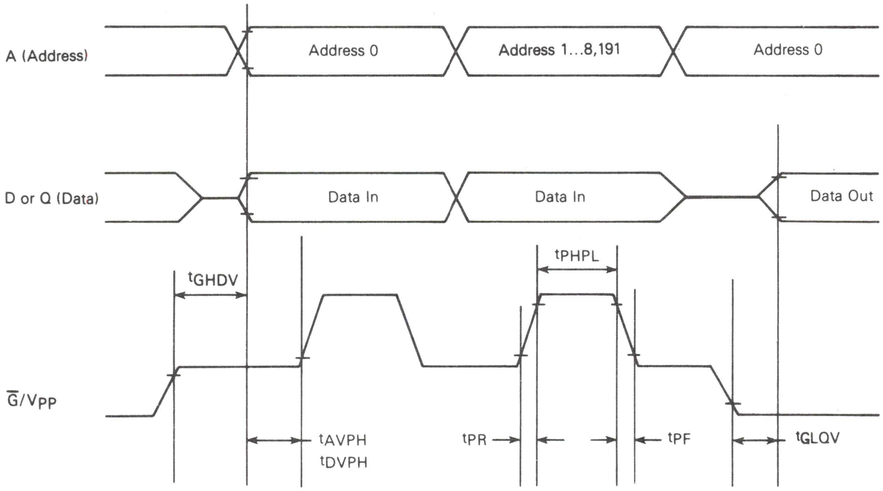
Characteristic	Condition	Symbol	Min	Typ	Max	Unit
Address Input Sink Current	$V_{in} = 5.25$ V	I_{LI}	–	–	10	μA
V_{PP} Program Pulse Supply Current ($V_{PP} = 25$ V ±1 V)	–	I_{PH}	–	–	30	mA
V_{PP} Supply Current ($V_{PP} = 2.4$ V)	–	$I_{PL} = I_{GH}$	–	–	400	μA
V_{CC} Supply Current ($V_{PP} = 5$ V)	–	I_{CC}	–	–	160	mA

AC PROGRAMMING OPERATING CONDITIONS AND CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Address Setup Time	t_{AVPH}	2.0	–	μs
Data Setup Time	t_{DVPH}	2.0	–	μs
Output Enable to Valid Data	t_{GLQV}	150	–	ns
Output Disable to Data In	t_{GHDV}	2.0	–	μs
Program Pulse Width	t_{PHPL}	1.9	2.1	ms
Program Pulse Rise Time	t_{PR}	0.5	2.0	μs
Program Pulse Fall Time	t_{PF}	0.5	2.0	μs
Cumulative Programming Time Per Word*	t_{CP}	12	50	ms

*Block mode programming must be used. Block mode programming is defined as one program pulse applied to each of the 8,192 address locations in sequence. Multiple blocks are used to accumulate programming time (t_{CP}).

PROGRAMMING OPERATION TIMING DIAGRAM



PROGRAMMING INSTRUCTIONS

After the completion of an ERASE operation, every bit in the device is in the "1" state (represented by Output High). Data are entered by programming zeros (Output Low) into the required bits. The words are addressed the same way as in the READ operation. A programmed "0" can only be changed to a "1" by ultraviolet light erasure.

To set the memory up for Program Mode, the $\overline{G}/V_{PP}$ input (Pin 20) should be between +2.0 and +6.0 V, which will three-state the outputs and allow data to be set up on the DQ terminals. The V_{CC} voltage is the same as for the Read operation. Only "0's" will be programmed when "0's" and "1's" are entered in the 8-bit data word.

After address and data setup, 25-volt programming pulse (V_{IH} to V_{IHP}) is applied to the G/V_{PP} input. The program pulse width is 2 ms and the maximum program pulse amplitude is 26 V.

Multiple MCM68766s may be programmed in parallel by connecting like inputs and applying the program pulse to the $\overline{G}/V_{PP}$ inputs. Different data may be programmed into multiple MCM68766s connected in parallel by selectively applying the programming pulse only to the MCM68766s to be programmed.

READ OPERATION

After access time, data is valid at the outputs in the Read mode. With $\overline{G}/V_{PP}$ = "0" the outputs are enabled; with $\overline{G}/V_{PP}$ = "1" the outputs are three-stated.

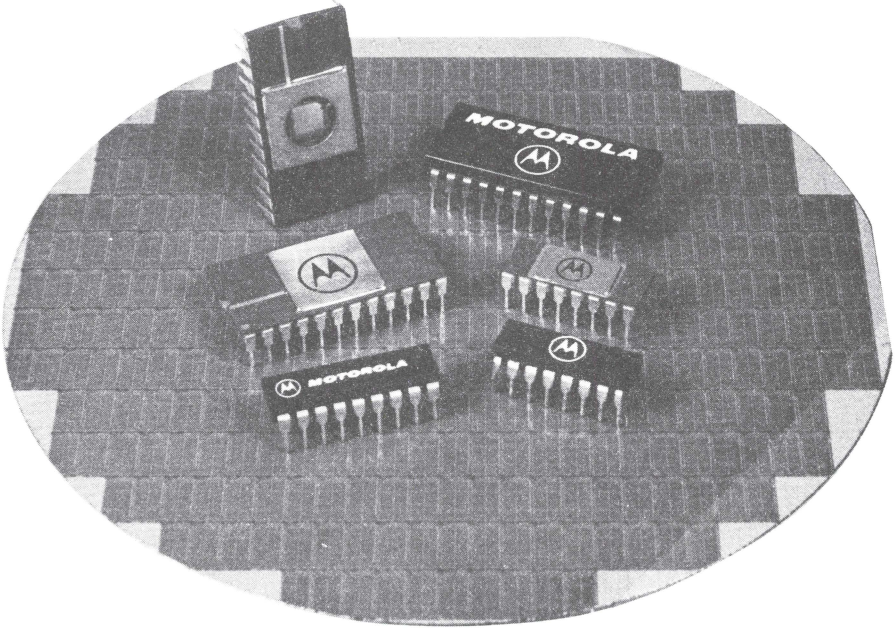
Multiple MCM68766s may share a common data bus with like outputs OR-tied together. In this configuration only one $\overline{G}/V_{PP}$ input should be low and no other device outputs should be active on the same bus. This will prevent data contention on the bus.

ERASING INSRUCTIONS

The MCM68766 can be erased by exposure to high intensity shortwave ultraviolet light, with a wavelength of 2537 angstroms. The recommended integrated dose (i.e., UV-intensity X exposure time) is 15 Ws/cm^2. As an example, using the "Model 30-000" UV Eraser (Turner Designs, Mountain View, CA 94043) the ERASE-time is 36 minutes. The lamps should be used without shortwave filters and the MCM68766 should be positioned about one inch away from the UV-tubes.

RECOMMENDED OPERATING PROCEDURES

After erasure and reprogramming of the EPROM, it is recommended that the quartz window be covered with an opaque self-adhesive cover. It is important that the self-adhesive cover not leave any residue on the quartz if it is removed to allow another erasure.


MOTOROLA
MOTOROLA

MOS EEPROM

MOTOROLA

MCM2801

Advance Information

16 × 16-BIT SERIAL ELECTRICALLY ERASABLE PROM

The MCM2801 is a 256-bit serial Electrically Erasable PROM designed for handling small amounts of data in applications requiring both nonvolatile memory and in-system information updates.

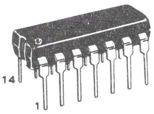
The MCM2801 offers in-system erase and reprogram capability. It has external control of timing functions and serial format for data and address. The MCM2801 is fabricated in floating gate technology for high reliability and producibility.

- Single +5 V Power Supply
- Organized as 16 Words of 16 Bits
- MPU Bus Compatible
- Single +25 V Power Supply for Erase and Program
- In-System Program/Erase Capability
- Both Word and Whole Array Erasable

MOS

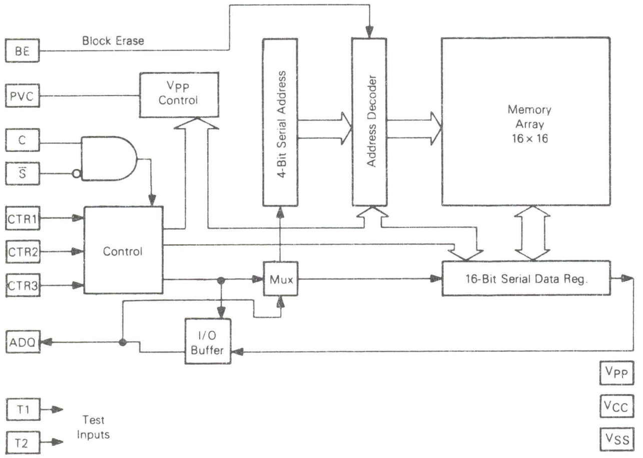
(N-CHANNEL, SILICON GATE)

16 × 16 BIT
ELECTRICALLY ERASABLE
PROGRAMMABLE READ
ONLY MEMORY

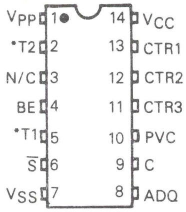


PLASTIC PACKAGE
CASE 646-05

BLOCK DIAGRAM


BE
Block Erase
PVC
Vpp Control
C
S̄
CTR1
CTR2
CTR3
Control
4-Bit Serial Address
Address Decoder
Memory Array 16 × 16
Mux
16-Bit Serial Data Reg.
ADQ
I/O Buffer
T1
T2
Test Inputs
Vpp
Vcc
Vss

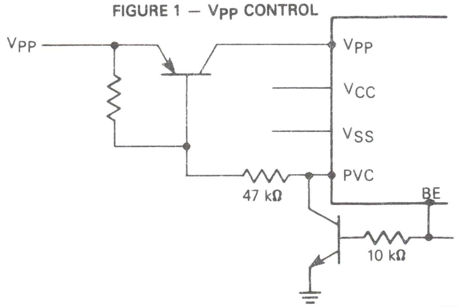
PIN ASSIGNMENT


VPP 1 ● 14 VCC
*T2 2 13 CTR1
N/C 3 12 CTR2
BE 4 11 CTR3
*T1 5 10 PVC
S̄ 6 9 C
VSS 7 8 ADQ

*For normal operation, these inputs should be hardwired to V_{SS}.

PIN NAMES	
ADQ	Multiplexed Address/ Data-In/Data-Out
C	Clock
PVC	Program Voltage Control
CTR1, 2, 3	Control
BE	Block Erase
S̄	Chip Select
T1, T2	Test Pins

FIGURE 1 — V_{PP} CONTROL


VPP
VPP
VCC
VSS
PVC
BE
47 kΩ
10 kΩ

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MODE SELECTION

Mode	Pin Number						
	1 V_{PP}	6 $\overline{S}$	7 V_{SS}	11 CTR3	12 CTR2	13 CTR1	14 V_{CC}
Standby	V_{SS} or V_{CC}	V_{IH}	V_{SS}	V_{IH}	V_{IH}	V_{IH}	V_{CC}
Word Erase	V_{PP}	V_{IL}	V_{SS}	V_{IH}	V_{IL}	V_{IL}	V_{CC}
Write	V_{PP}	V_{IL}	V_{SS}	V_{IL}	V_{IH}	V_{IL}	V_{CC}
Serial Data Out	V_{SS} or V_{CC}	V_{IL}	V_{SS}	V_{IH}	V_{IH}	V_{IL}	V_{CC}
Serial Address In	V_{SS} or V_{CC}	V_{IL}	V_{SS}	V_{IL}	V_{IL}	V_{IH}	V_{CC}
Serial Data In	V_{SS} or V_{CC}	V_{IL}	V_{SS}	V_{IH}	V_{IL}	V_{IH}	V_{CC}
Read	V_{SS} or V_{CC}	V_{IL}	V_{SS}	V_{IL}	V_{IH}	V_{IH}	V_{CC}
Standby	V_{SS} or V_{CC}	V_{IH}	V_{SS}	V_{IL}	V_{IL}	V_{IL}	V_{CC}

ABSOLUTE MAXIMUM RATINGS (1)

Rating	Value	Unit
Temperature Under Bias	−40 to +85	°C
Operating Temperature Range	0 to +70	°C
Storage Temperature	−55 to +150	°C
All Input or Output Voltages with Respect to V_{SS} (Except PVC)	+8 to −0.5	V
V_{PP} Supply Voltage with Respect to V_{SS}	+28 to −0.5	V
PVC Voltage with Respect to V_{SS}	+28 to −0.5	V

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS (Full operating voltage and temperature range unless otherwise noted.)

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC} V_{PP}	4.5 24.0	5.0 25	5.5 26.0	V
Input High Voltage	V_{IH}	2.4	–	$V_{CC}+1.0$	V
Input Low Voltage	V_{IL}	−0.1	–	0.8	V

OPERATING DC CHARACTERISTICS

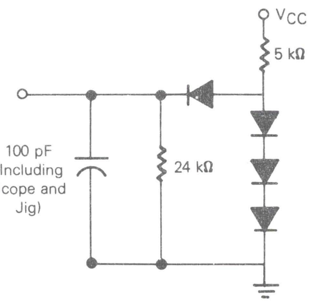
Characteristic	Condition	Symbol	Min	Typ	Max	Units
Input Sink Current	$0 < V_{in} < V_{CC}$	I_{in}	–	–	10	μA
V_{CC} Supply Current	$V_{CC} = 5.5$ V	I_{CC}	–	–	30	mA
V_{PP} Supply Current	$V_{PP} = 26.0$ V	I_{PP}	–	–	4.0	mA
Output Low Voltage	$I_{OL} = 1.0$ mA	V_{OL}	–	–	0.5	V
Output High Voltage	$I_{OH} = -0.1$ mA	V_{OH}	2.4	–	–	V
PVC Current (Write or Word Erase)	PVCL = 1 V	PVC_{ON}	200	–	–	μA
PVC Leakage	PVCH = 26 V	PVC_{OFF}	–	–	5	μA

CAPACITANCE (f = 1.0 MHz, $T_A = 25°C$, $V_{CC} = +5$ V, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance ($V_{in} = 0$ V)	C_{in}	–	6.0	pF
Output Capacitance ($V_{out} = 0$ V)	C_{out}	–	12	pF

Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta_t/\Delta V$.

FIGURE 2 — OUTPUT LOAD



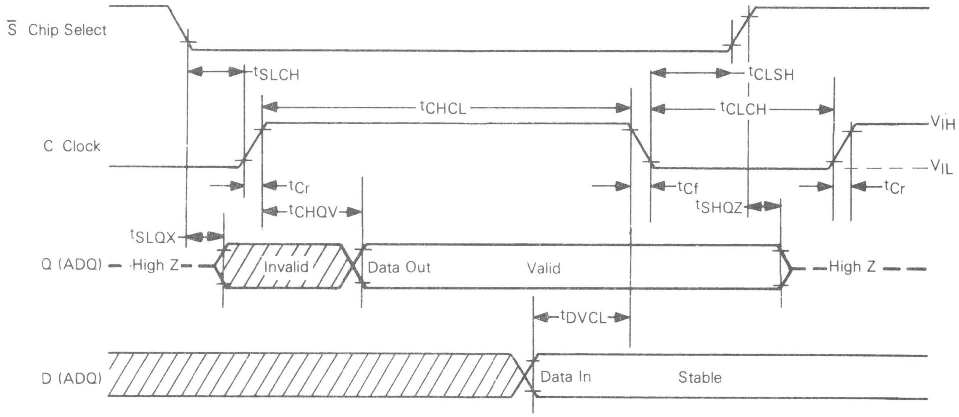
AC OPERATING CONDITIONS AND CHARACTERISTICS

Input Pulse Levels .... 0.65 Volts and 2.6 Volts
Input Rise and Fall Times .... 20 ns
Input Timing Levels .... 1.0 Volt and 3.8 Volts
Output Timing Levels .... 1.0 Volt and 2 Volts
Output Load .... See Figure 2

Characteristic	Symbol	Min	Max	Unit
Erase Time	t_{ERASE}	100	–	ms
Write Time	t_{WRITE}	10	–	ms
Clock High Level Hold Time	t_{CHCL}	4	10	μs
Clock Low Level Hold Time	t_{CLCH}	4	–	μs
Clock Rise Time	t_{Cr}	5	1000	ns
Clock Fall Time	t_{Cf}	5	1000	ns
Chip Select Setup	t_{SLCH}	1	–	μs
Chip Select Hold	t_{CLSH}	1	–	μs
Data Out Delay	t_{CHQV}	–	1	μs
Address In Setup	t_{AVCL}	1	–	μs
Data In Setup	t_{DVCL}	1	–	μs
Control Setup Time	t_{CtrVCH}	1	–	μs
Control Hold Time	t_{CtrX}	50	–	ns
Data-Off Time (from the Clock)	t_{CHQZ}	–	3.0	μs
Chip Select Low to Output Active Time	t_{SLQX}	–	2.0	μs
Data-Off Time (from Chip Select)	t_{SHQZ}	–	2.0	μs

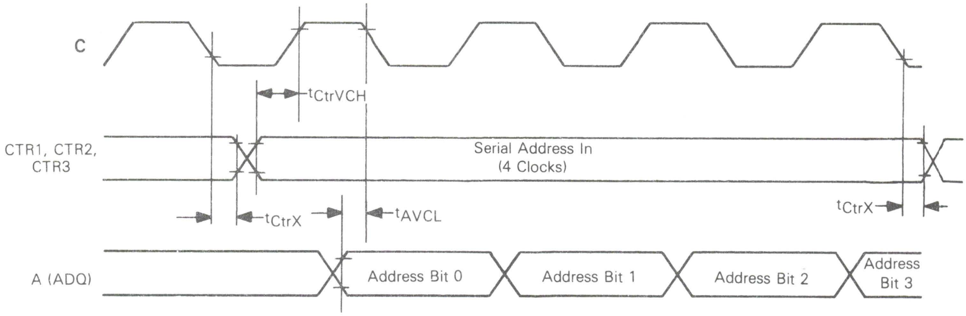
TIMING DIAGRAMS

Clock Cycle Detail

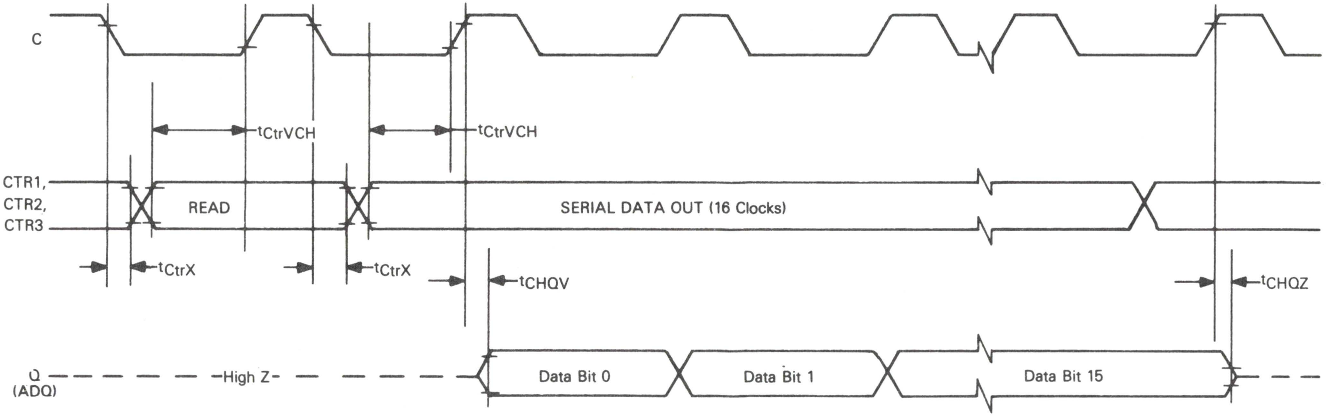

$\overline{S}$ Chip Select
t_{SLCH}
t_{CLSH}
t_{CHCL}
t_{CLCH}
C Clock
V_{IH}
V_{IL}
t_{Cr}
t_{CHQV}
t_{Cf}
t_{SHQZ}
t_{Cr}
t_{SLQX}
Q (ADQ)
High Z
Invalid
Data Out
Valid
High Z
t_{DVCL}
D (ADQ)
Data In
Stable

All times defined at 10% or 90% points.

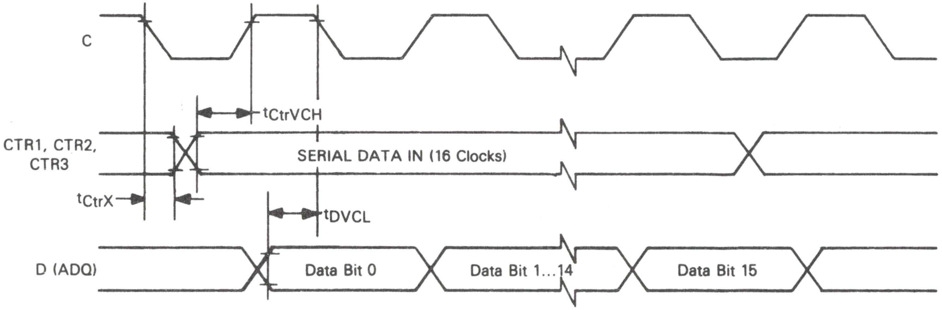
Serial Address In


C
t_{CtrVCH}
CTR1, CTR2, CTR3
Serial Address In
(4 Clocks)
t_{CtrX}
t_{AVCL}
t_{CtrX}
A (ADQ)
Address Bit 0
Address Bit 1
Address Bit 2
Address Bit 3

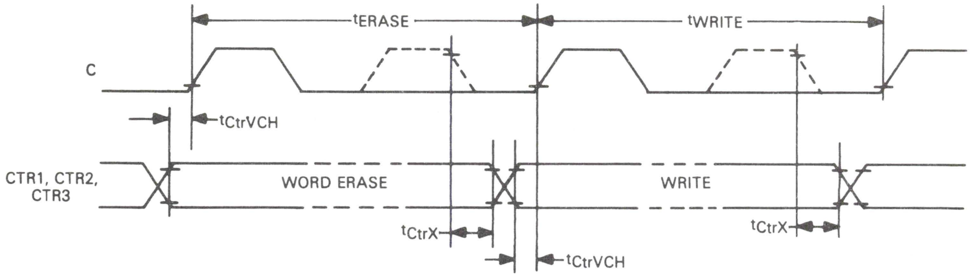
READ AND SERIAL DATA OUT


C
tCtrVCH
tCtrVCH
CTR1,
CTR2,
CTR3
READ
SERIAL DATA OUT (16 Clocks)
tCtrX
tCtrX
tCHQV
tCHQZ
Q
(ADQ)
High Z
Data Bit 0
Data Bit 1
Data Bit 15

SERIAL DATA IN


C
tCtrVCH
CTR1, CTR2,
CTR3
SERIAL DATA IN (16 Clocks)
tCtrX
tDVCL
D (ADQ)
Data Bit 0
Data Bit 1...14
Data Bit 15

ERASE-WRITE SEQUENCE



NOTE: One clock pulse is sufficient to load a new control code.

FUNCTIONAL DESCRIPTION

The memory stores sixteen words, each of sixteen bits. All functions are selected by a 3-bit parallel control code. The clock line is used to strobe these codes and to serially shift data and addresses.

Read-Out

1. The 4-bit serial address is shifted on the ADQ line while the SERIAL ADDRESS-IN code is applied on the three control pins.
2. The READ instruction is strobed with one clock pulse. This reads the word from the new address in the memory array and parallel loads it into the data register.
3. While the SERIAL DATA-OUT code is being applied, data is shifted out on the ADQ pin with 16 clock pulses. In this mode, the ADQ pin output buffer is active.

Writing

1. The address is changed, if necessary, in the same manner as in the readout.
2. While the SERIAL DATA-IN code is being applied, data is shifted in on the ADQ pin with 16 clock pulses. If the data to be written has already been shifted into the data register, it is not necessary to re-enter the 16 bits, so this step may be omitted.
3. The WORD ERASE code is strobed in with one clock pulse. After the specified ERASE time, the addressed word is erased.
4. The WRITE code is strobed in with one clock pulse. After the specified WRITE time, a STANDBY code can be strobed in to stop writing. Data will be programmed at the specified address.

It is also possible to change the sequence by erasing a memory location before starting a write sequence.

Standby

Either of the two STANDBY codes, when strobed in with a clock pulse, puts the memory in a quiescent state. The output is then in the high-impedance state and the absence or presence of the clock will not affect the device.

Pin Description

The active high clock signal (C) is used for shifting addresses and data into or out of the chip. It is also used for strobing control codes.

The I/O pin (ADQ) is used for entering addresses and data-in. It is in the output state only for shifting output data.

The active low Chip Select pin ($\overline{S}$) is only used to block the clock and put the ADQ buffer into the high-impedance mode. It has no influence on the operating status of the device and does not force a standby condition.

The programming voltage control pin (PVC) is an open-drain output that is active when a WORD ERASE or WRITE control code is strobed in. As shown in Figure 1, it can be used to control the V_{PP} supply applied to the circuit. The BLOCK ERASE (BE) pin can be used to clear the whole array. As the PVC output is not active in this state, the programming voltage should be directly applied to the V_{PP} pin for the specified erase time.

The Test inputs (TEST1 and TEST2) are provided for testing purpose only and should be connected to V_{SS} in any application.

Data Protection

When V_{PP} is turned off, data stored in the array is protected. The programming voltage should not be applied to the V_{PP} pin if V_{CC} is not present. Therefore, use of the PVC control output, which is controlled by the V_{CC} supply is recommended. Using this feature, V_{PP} and V_{CC} can be turned on or off in any sequence without disturbing data in the array. However, to avoid spurious control codes being strobed into the device, all inputs should be stable when V_{PP} is on.

General Comments

The erased state corresponds to a logical zero at the ADQ output.

WRITE (for any address) must be preceded by an ERASE at the same address.

V_{PP} is necessary for WRITE, WORD ERASE or BLOCK ERASE. In all other cases, it can be switched to high impedance, V_{CC} or V_{SS}.

MOTOROLA

MCM2802

Advance Information

MOS
(N-CHANNEL, SILICON GATE)

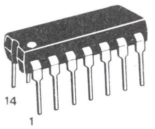
32 × 32 BIT ELECTRICALLY ERASABLE PROGRAMMABLE READ ONLY MEMORY

1K-BIT SERIAL ELECTRICALLY ERASABLE PROM

The MCM2802 is a 1K-bit serial Electrically Erasable PROM designed for applications requiring both nonvolatile memory and in-system information updates.

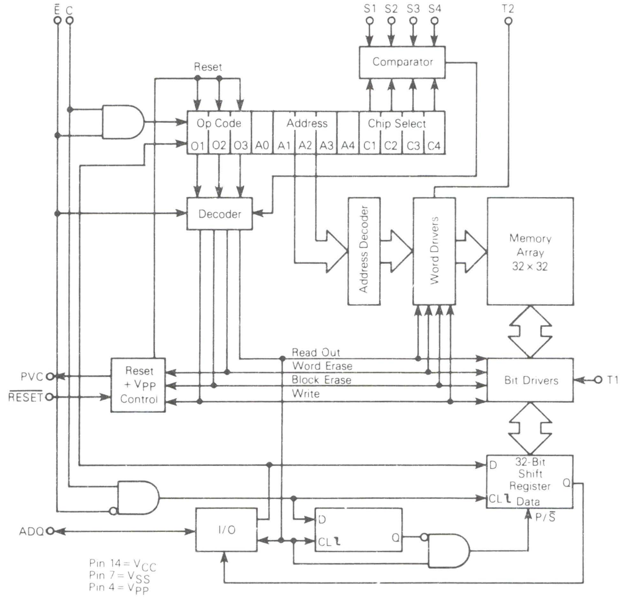
The MCM2802 offers in-system erase and reprogram capability. In digital tuning systems, it provides storage for up to 32 channels. It has external control of timing functions and serial format for data and address. The MCM2802 is fabricated in floating gate technology for high reliability and producibility.

- Single +5 V Power Supply in Read Mode
- Organized as 32 Bytes of 32 Bits
- MPU Bus Compatible
- 0-100 kHz Clock Rate
- +25 V Power Supply for Erase and Program
- In-system Program/Erase Capability
- Both Word and Array Erasable
- Expandable to 16K-bit Systems

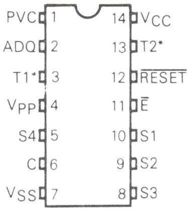


P SUFFIX
PLASTIC PACKAGE
CASE 646

BLOCK DIAGRAM


Ē
C
S1 S2 S3 S4
T2
Comparator
Reset
Op Code
Address
Chip Select
O1 O2 O3 A0 A1 A2 A3 A4 C1 C2 C3 C4
Decoder
Address Decoder
Word Drivers
Memory Array 32 × 32
Read Out
Word Erase
Block Erase
Write
PVC
RESET
Reset + Vpp Control
Bit Drivers
T1
D
32-Bit Shift Register
Q
CL
Data
P/S̄
ADQ
I/O
D
CL
Q
Pin 14 = V_{CC}
Pin 7 = V_{SS}
Pin 4 = V_{PP}

PIN ASSIGNMENTS


PVC 1
ADQ 2
T1* 3
VPP 4
S4 5
C 6
VSS 7
14 VCC
13 T2*
12 RESET
11 Ē
10 S1
9 S2
8 S3

*For Normal Operation, Hardwire to V_{SS}

PIN NAMES	
PVC	Program Voltage Control
ADQ	Multiplexed Address/Data-In/ Data-Out
T1, T2	Test Pins
S1, S2, S3, S4	Chip Select
C	Clock
Ē	Chip Enable
$\overline{\text{RESET}}$	Reset

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MOTOROLA

MCM2816

Advance Information

2048 × 8-BIT ELECTRICALLY ERASABLE PROM

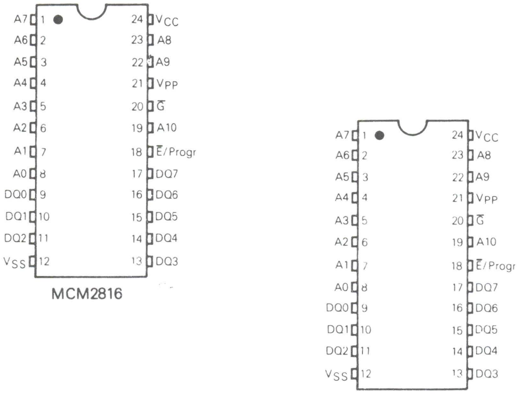
The MCM2816 is a 16,384-bit Electrically Erasable Programmable Read Only Memory designed for handling data in applications requiring both nonvolatile memory and in-system reprogramming. The industry standard pinout in a 24-pin dual-in-line package makes the MCM2816 EEPROM compatible with the popular MCM2716 EPROM.

The MCM2816 saves time and money because of the in-system erase and reprogram capability. While V_{PP} is at 25 V and $\overline{G}$ is at V_{IL}, a 100 ms active high TTL erase pulse applied to the $\overline{E}$/Progr pin allows the entire memory to be erased to the "1" state. In addition to in-system programmability, this new-generation PROM is programmable on the standard EPROM programmer.

For ease of use, the device operates in the read mode from a single power supply and has a static power-down mode. The MCM2816 is fabricated in floating gate technology for high reliaiblity and producibility.

- Single +5 V Power Supply
- Automatic Power-Down Mode (Standby)
- Single +25 V Power Supply for Erase and Program
- Organized as 2048 Bytes of 8 Bits
- Maximum Access Time = 450 ns MCM2816
- Pin Compatible to MCM68316E and MCM2716
- In-System Program/Erase Capability
- Chip Erase Time of 10 ms

PINOUT COMPARISON 2816 AND 2716


A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
DQ0 9
DQ1 10
DQ2 11
VSS 12
24 VCC
23 A8
22 A9
21 VPP
20 G
19 A10
18 E/Progr
17 DQ7
16 DQ6
15 DQ5
14 DQ4
13 DQ3

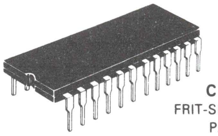
MCM2816 MCM2716

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MOS

(N-CHANNEL, SILICON GATE)

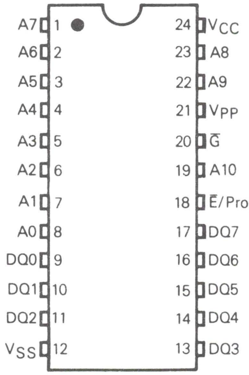
2048 × 8-BIT ELECTRICALLY ERASABLE PROGRAMMABLE READ ONLY MEMORY



C SUFFIX
FRIT-SEAL CERAMIC
PACKAGE
CASE 623-05

L SUFFIX CERAMIC PACKAGE ALSO AVAILABLE — CASE 716-06

PIN ASSIGNMENT


A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
DQ0 9
DQ1 10
DQ2 11
VSS 12
24 VCC
23 A8
22 A9
21 VPP
20 G
19 A10
18 E/Progr
17 DQ7
16 DQ6
15 DQ5
14 DQ4
13 DQ3

*Pin Names	
A	Address
DQ	Data Input/Output
$\overline{E}$/Progr	Chip Enable/Program-Erase
$\overline{G}$	Output Enable

*New industry standard nomenclature

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Value	Unit
Temperature Under Bias	−10 to +80	°C
Operating Temperature Range	0 to +70	°C
Storage Temperature	−65 to +125	°C
All Input or Output Voltages with Respect to V_{SS}	+6 to −0.3	V
V_{PP} Supply Voltage with Respect to V_{SS}	+28 to −0.3	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

MODE SELECTION

Mode	Pin Number					
	9-11, 13-17 DQ	12 V_{SS}	18 $\overline{E}$/Progr	20 G	21 V_{PP}	24 V_{CC}
Read	Data Out	V_{SS}	V_{IL}	V_{IL}	V_{CC}**	V_{CC}
Output Disable	High Z	V_{SS}	Don't Care	V_{IH}	V_{CC}**	V_{CC}
Standby	High Z	V_{SS}	V_{IH}	Don't Care	V_{CC}**	V_{CC}
Program	Data In	V_{SS}	Pulsed V_{IL} to V_{IH}	V_{IH}	V_{IHP}	V_{CC}
Program Verify	Data Out	V_{SS}	V_{IL}	V_{IL}	V_{IHP}	V_{CC}
Program Inhibit	High Z	V_{SS}	V_{IL}	V_{IH}	V_{IHP}	V_{CC}
Erase	High Z*	V_{SS}	Pulsed V_{IL} to V_{IH}	V_{IL}	V_{IHP}	V_{CC}

*Outputs momentarily active before going to High Z at $\overline{E}=V_{IH}$.
**or V_{SS}

BLOCK DIAGRAM

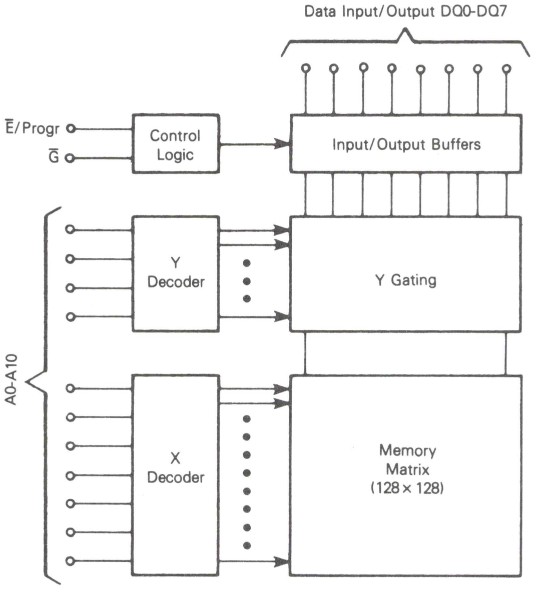
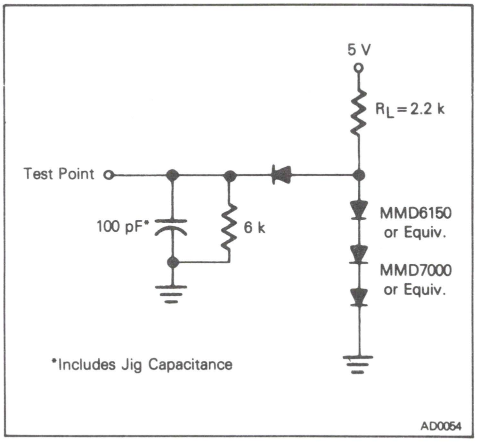

Data Input/Output DQ0-DQ7
$\overline{E}$/Progr
$\overline{G}$
Control Logic
Input/Output Buffers
Y Decoder
Y Gating
A0-A10
X Decoder
Memory Matrix (128 × 128)
AD0053

FIGURE 1 — AC TEST LOAD


5 V
R_L = 2.2 k
Test Point
100 pF*
6 k
MMD6150 or Equiv.
MMD7000 or Equiv.
*Includes Jig Capacitance
AD0054

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED DC OPERATING CONDITIONS

Parameter		Symbol	Min	Nom	Max	Unit
Supply Voltage	MCM2816-45	V_{CC} V_{PP}	4.75 V_{SS}	5.0 5.0	5.25 $V_{CC}+0.6$	V
Input High Voltage		V_{IH}	2.0	–	$V_{CC}+1.0$	V
Input Low Voltage		V_{IL}	−0.1	–	0.8	V

RECOMMENDED DC OPERATING CHARACTERISTICS

Characteristic	Condition	Symbol	Min	Typ	Max	Units
Address, $\overline{G}$ and $\overline{E}$/Progr Input Sink Current	$V_{in}=5.25$ V	I_{in}	–	–	10	μA
Output Leakage Current	$V_{out}=5.25$ V $\overline{G}=5.0$ V	I_{LO}	–	–	10	μA
V_{CC} Supply Current (Standby) (Outputs Open)	$\overline{E}$/Progr $=V_{IH}$ $\overline{G}=V_{IL}$	I_{CC1}	–	–	25	mA
V_{CC} Supply Current (Active) (Outputs Open)	$\overline{G}=\overline{E}$/Progr $=V_{IL}$	I_{CC2}	–	–	100	mA
V_{PP} Supply Current*	$V_{PP}=5.25$ V	I_{PP1}	–	1.0	5.0	mA
Output Low Voltage	$I_{OL}=2.1$ mA	V_{OL}	–	–	0.45	V
Output High Voltage	$I_{OH}=-400$ μA	V_{OH}	2.4	–	–	V

*V_{CC} must be applied simultaneously or prior to V_{PP}. V_{CC} must also be switched off simultaneously with or after V_{PP}. With V_{PP} connected directly to V_{CC} during the read operation, the supply current would then be the sum of I_{PP1} and I_{CC}. Typical values are for $T_A=25°C$ and nominal supply voltages.

CAPACITANCE (f = 1.0 MHz, $T_A=25°C$, $V_{CC}=5$ V, periodically sampled rather than 100% tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance ($V_{in}=0$ V)	C_{in}	4.0	6.0	pF
Output Capacitance ($V_{out}=0$ V)	C_{out}	8.0	12	pF

Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C=I_{\Delta t}/\Delta V$.

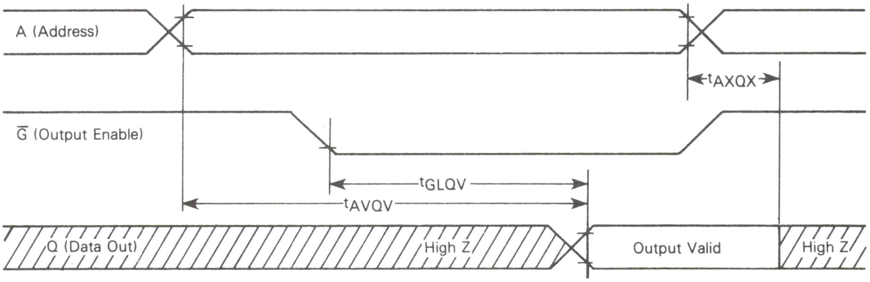
AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

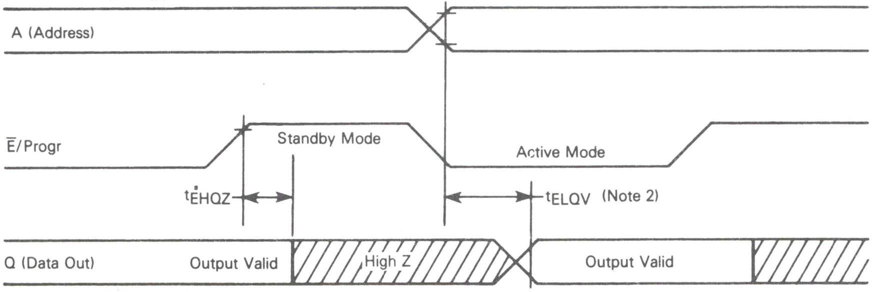
Input Pulse Levels....................................0.8 Volt and 2.2 Volts
Input Rise and Fall Times..20 ns
Input Timing level...1.0 and 2.0 V
Output Timing Levels.....................................2.0 and 0.8 Volts
Output Load...See Figure 1

Characteristic	Condition	Symbol	Min	Max	Unit
Address Valid to Output Valid	$\overline{E}$/Progr $=\overline{G}=V_{IL}$	t_{AVQV}	–	450	ns
$\overline{E}$/Progr to Output Valid	(Note 2)	t_{ELQV}	–	450	
Output Enable to Output Valid	$\overline{E}$/Progr $=V_{IL}$	t_{GLQV}	–	120	
$\overline{E}$/Progr to High Z Output	–	t_{EHQZ}	0	100	
Output Disable to High Z Output	$\overline{E}$/Progr $=V_{IL}$	t_{GHQZ}	0	100	
Data Hold from Address	$\overline{E}$/Progr $=\overline{G}=V_{IL}$	t_{AXQX}	0	–	

READ MODE TIMING DIAGRAMS ($\overline{E}$/Progr $=V_{IL}$)



STANDBY MODE (Output Enable = V_{IL})
Standby Mode ($\overline{E}$/Progr = V_{IH})



Note 2: t_{ELQV} is referenced to $\overline{E}$/Progr or stable address, whichever occurs last.

DC PROGRAMMING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED PROGRAMMING OPERATING CONDITIONS

Parameter		Symbol	Min	Nom	Max	Unit
Supply Voltage	MCM2816-45	V_{CC} V_{PP}	4.75 24	5.0 25	5.25 26	V
Input High Voltage for Data		V_{IH}	2.2	–	$V_{CC}+1$	V
Input Low Voltage for Data		V_{IL}	−0.1	–	0.8	V

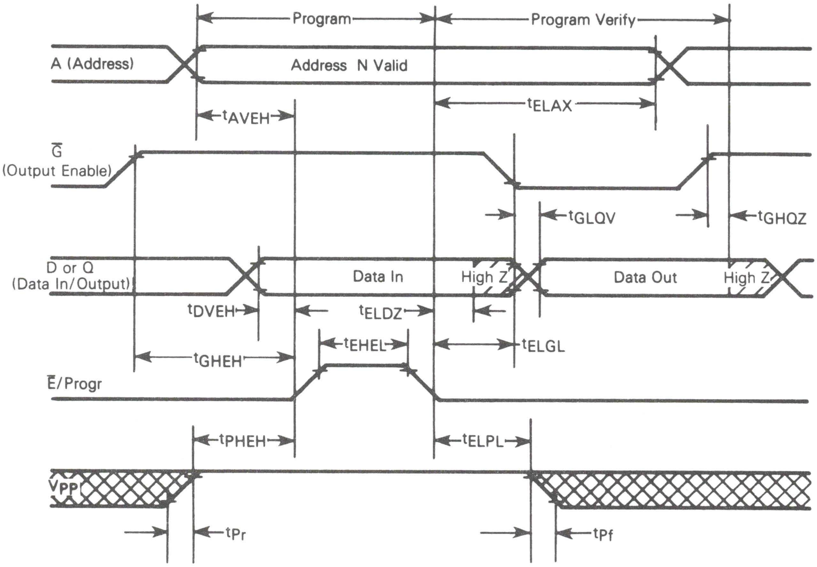
PROGRAMMING OPERATION DC CHARACTERISTICS

Characteristic	Condition	Symbol	Min	Typ	Max	Unit
Address, $\overline{G}$ and $\overline{E}$/Progr Input Sink Current	V_{in} = 5.25 V/0.45 V	I_{L1}	–	–	10	μA
V_{PP} Supply Current (V_{PP} = 25 V ± 1 V)	$\overline{E}$/Progr = V_{IL}	I_{PP1}	–	–	10	mA
V_{PP} Programming Pulse Supply Current (V_{PP} = 25 V ± 1 V)	$\overline{E}$/Progr = V_{IH}	I_{PP2}	–	–	10	mA
V_{CC} Supply Current	–	I_{CC}	–	–	100	mA

AC PROGRAMMING OPERATING CONDITIONS AND CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Address Setup Time	t_{AVEH}	2.0	–	μs
Output Enable High to Program Pulse	t_{GHEH}	2.0	–	μs
Data Setup Time	t_{DVEH}	2.0	–	μs
Address Hold Time	t_{ELAX}	2.0	–	μs
Output Enable Hold Time	t_{ELGL}	2.0	–	μs
Data Hold Time	t_{ELDZ}	2.0	–	μs
V_{PP} Setup Time	t_{PHEH}	2.0	–	μs
V_{PP} to Enable Low Time	t_{ELPL}	2.0	–	μs
Output Disable to High Z Output	t_{GHQZ}	0	150	ns
Output Enable to Valid Data ($\overline{E}$/Progr = V_{IL})	t_{GLQV}	–	150	ns
Progam Pulse Width	t_{EHEL}	1	10	ms
V_{PP} Rise Time	t_{Pr}	50	–	ns
V_{PP} Fall Time	t_{Pf}	50	–	ns

PROGRAMMING OPERATING TIMING DIAGRAM


Program
Program Verify
A (Address)
Address N Valid
t_{AVEH}
t_{ELAX}
$\overline{G}$ (Output Enable)
t_{GLQV}
t_{GHQZ}
D or Q (Data In/Output)
Data In
High Z
Data Out
High Z
t_{DVEH}
t_{ELDZ}
t_{EHEL}
t_{ELGL}
t_{GHEH}
$\overline{E}$/Progr
t_{PHEH}
t_{ELPL}
V_{PP}
t_{Pr}
t_{Pf}

ERASE OPERATION

(Full operating voltage and temperature range unless otherwise noted)

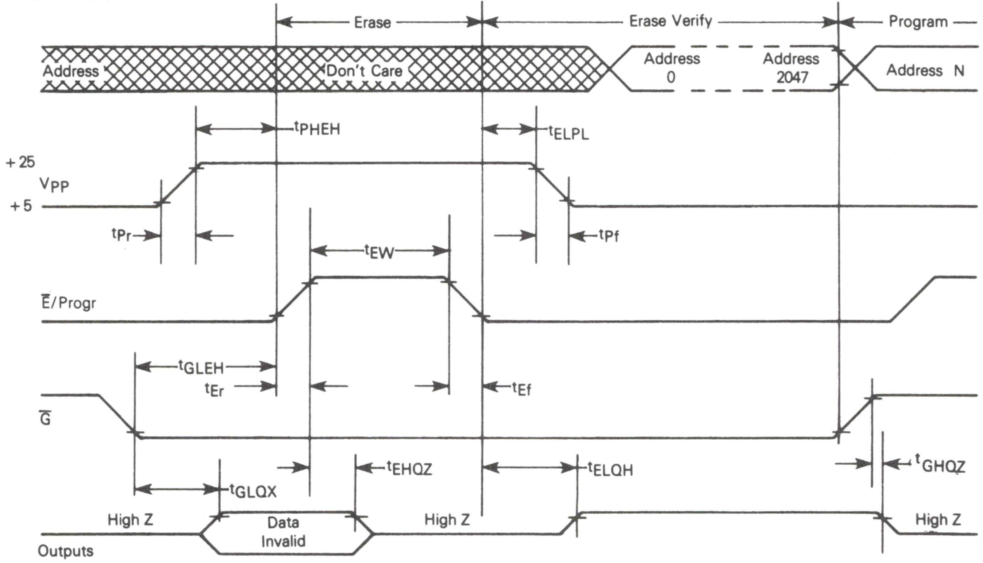
DC ERASING CHARACTERISTICS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Current (for any input)	I_{LI}	V_{in} = 5.5 V	–	–	10	μA
V_{CC} Supply Current (Outputs Open)	I_{CC}	V_{PP} = 25 V ± 1 V $\overline{E}$ = V_{IH}	–	–	50	mA
V_{PP} Supply Current	I_{PP}	V_{PP} = 25 V ± 1 V $\overline{E}$ = V_{IH}	–	5	10	mA
Input Low Level	V_{IL}	–	−0.1	–	0.8	V
Input High Level	V_{IH}	–	2.0	–	$V_{CC}+1$	V

AC ERASING CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{G}$ Setup Time	t_{GLEH}	2	–	–	μs
$\overline{E}$/Progr to Output Delay	t_{ELQH}	2	–	–	μs
Erase Pulse Width	t_{EW}	1	10	100	ms
Erase Pulse Rise Time	t_{Er}	5	–	–	ns
Erase Pulse Fall Time	t_{Ef}	5	–	–	ns
V_{PP} Rise Time	t_{Pr}	50	–	–	ns
V_{PP} Fall Time	t_{Pf}	50	–	–	ns
V_{PP} Setup Time	t_{PHEH}	2	–	–	μs
V_{PP} to Enable Low Time	t_{ELPL}	2	–	–	μs
Output Enable to Invalid Data ($\overline{E}$/Progr = V_{IH})	t_{GLQX}	–	–	150	ns
Output Disable to High Z Output	t_{GHQZ}	0	–	150	ns
Data Hold Time	t_{EHQZ}	2	–	–	μs

ERASING WAVEFORMS



FUNCTIONAL DESCRIPTION

All inputs for the operating modes are TTL levels. The power supplies are a +5 V_{CC} and a V_{PP}. The V_{PP} power supply must be at +25 V during Program, Verify, Program Inhibit and Erase, and must be at 0 or +5 V during Read and Deselect.

READ MODE

Data is available at the outputs in the read mode 450 ns (t_{AVQV}) from valid addresses with $\overline{G}$ low or 120 ns (t_{GLQV}) from $\overline{G}$ with addresses stable.

DESELECT MODE

The outputs of two or more EEPROMs may be OR-tied to the same data bus. Only one EEPROM should have its outputs selected ($\overline{G}$ low) to prevent data bus contention between two devices in this configuration. The outputs of other EEPROMs should be deselected with the $\overline{G}$ input at a high TTL level.

PROGRAMMING

After each erasure, all bits of the EEPROM are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by electrical erasure.

The EEPROM is in the programming mode when the V_{PP} power supply is at 25 V and $\overline{G}$ is at V_{IH}. The data to be programmed is applied 8 bits in parallel to the data output pins.

When the addresses and data are stable, a 10 ms, active high, TTL Program pulse is applied to the $\overline{E}$/Progr pin. A program pulse must be applied at each address location to be programmed. The program pulse has a maximum width of 10 ms. The EEPROM must not be programmed with a DC signal applied to the Progr input.

PROGRAM INHIBIT

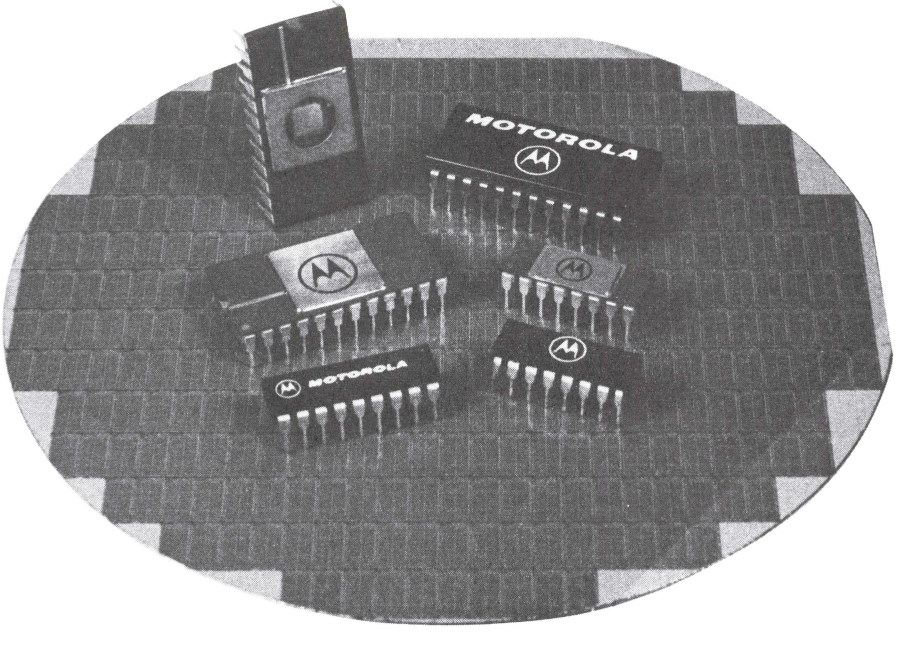
Programming of multiple EEPROMs in parallel is easily accomplished. Except for $\overline{E}$/Progr, all like inputs of the parallel devices may be common. A low level on the $\overline{E}$/Progr input inhibits the EEPROM from being programmed.

VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. This is accomplished by performing a read cycle with V_{PP} at 25 V and $\overline{E}$/Progr at V_{IL}.

ERASE

The EEPROM is electrically erased in nearly the same manner as it is programmed. The V_{PP} is at 25 V and $\overline{G}$ is at V_{IL}. A 100 ms active high, TTL erase pulse is applied to the $\overline{E}$/Progr pin and the entire memory is erased to the "1" state.


MOTOROLA
MOTOROLA

MOS ROM

MOTOROLA

MCM6670
MCM6674

128c X 7 X 5 CHARACTER GENERATOR

The MCM6670 is a mask-programmable horizontal-scan (row select) character generator containing 128 characters in a 5 X 7 matrix. A 7-bit address code is used to select one of the 128 available characters, and a 3-bit row select code chooses the appropriate row to appear at the outputs. The rows are sequentially displayed, providing a 7-word sequence of 5 parallel bits per word for each character selected by the address inputs.

The MCM6674 is a preprogrammed version of the MCM6670. The complete pattern of this device is contained in this data sheet.

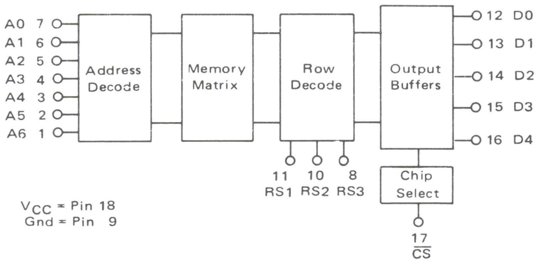
- Fully Static Operation
- TTL Compatibility
- Single ±10% +5 Volt Power Supply
- 18-Pin Package
- Diagonal Corner Power Supply Pins
- Fast Access Time, 350 ns (max)

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

BLOCK DIAGRAM


A0 7
A1 6
A2 5
A3 4
A4 3
A5 2
A6 1
Address Decode
Memory Matrix
Row Decode
Output Buffers
12 D0
13 D1
14 D2
15 D3
16 D4
11 RS1
10 RS2
8 RS3
Chip Select
17 CS

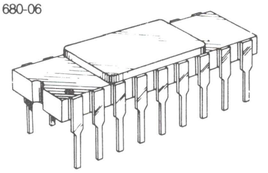
V_{CC} = Pin 18
Gnd = Pin 9

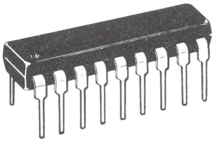
MOS

(N-CHANNEL, SILICON GATE)

128c x 7 x 5
HORIZONTAL-SCAN
CHARACTER GENERATOR

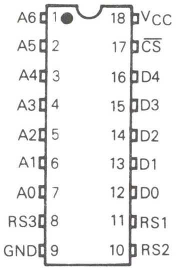
L SUFFIX
CERAMIC PACKAGE
CASE 680-06





P SUFFIX
PLASTIC PACKAGE
CASE 707

PIN ASSIGNMENT


A6 1
A5 2
A4 3
A3 4
A2 5
A1 6
A0 7
RS3 8
GND 9
18 VCC
17 CS
16 D4
15 D3
14 D2
13 D1
12 D0
11 RS1
10 RS2

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

DS9459/12-77

DC OPERATING CONDITIONS AND CHARACTERISITCS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	Vdc
Input High Voltage	V_{IH}	2.0	–	5.5	Vdc
Input Low Voltage	V_{IL}	-0.3	–	0.8	Vdc

DC CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current (V_{in} = 0 to 5.5 V)	I_{in}	–	–	2.5	µAdc
Output High Voltage (I_{OH} = -205 µA)	V_{OH}	2.4	–	V_{CC}	Vdc
Output Low Voltage (I_{OL} = 1.6 mA)	V_{OL}	–	–	0.4	Vdc
Output Leakage Current (Three-State) (CS = 2.0 V or $\overline{CS}$ = 0.8 V, V_{out} = 0.4 V to 2.4 V)	I_{LO}	–	–	10	µAdc
Supply Current (V_{CC} = 5.5 V, T_A = 0°C)	I_{CC}	–	–	130	mAdc

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

Characteristic	Symbol	Typ	Unit
Input Capacitance	C_{in}	5.0	pF
Output Capacitance	C_{out}	5.0	pF

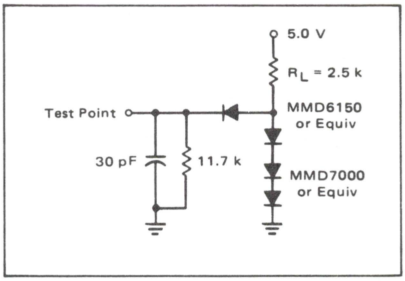
AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

AC TEST CONDITIONS

Condition	Value
Input Pulse Levels	0.8 V to 2.0 V
Input Rise and Fall Times	20 ns
Output Load	1 TTL Gate and C_L = 30 pF

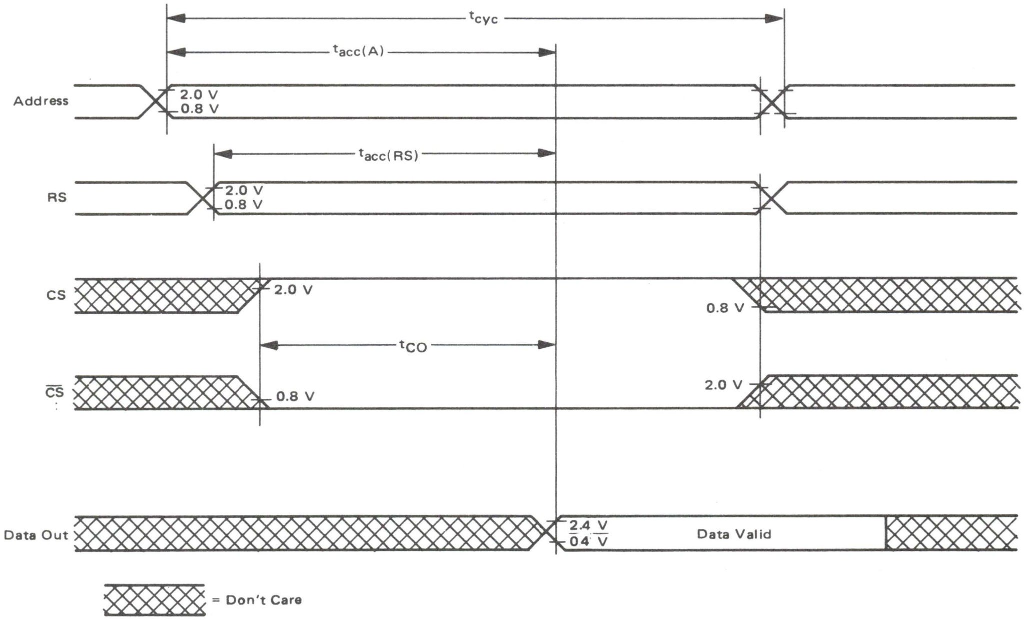
AC TEST LOAD


5.0 V
R_L = 2.5 k
MMD6150 or Equiv
Test Point
30 pF
11.7 k
MMD7000 or Equiv

AC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Cycle Time	t_{cyc}	350	–	ns
Address Access Time	$t_{acc(A)}$	–	350	ns
Row Select Access Time	$t_{acc(RS)}$	–	350	ns
Chip Select to Output Delay	t_{CO}	–	150	ns

TIMING DIAGRAM


t_{cyc}
$t_{acc(A)}$
Address
2.0 V
0.8 V
$t_{acc(RS)}$
RS
2.0 V
0.8 V
CS
2.0 V
0.8 V
t_{CO}
$\overline{CS}$
0.8 V
2.0 V
Data Out
2.4 V
0.4 V
Data Valid
= Don't Care

CUSTOM PROGRAMMING FOR MCM6670

By the programming of a single photomask, the customer may specify the content of the MCM6670. Encoding of the photomask is done with the aid of a computer to provide quick, efficient implementation of the custom bit pattern while reducing the cost of implementation.

Information for the custom memory content may be sent to Motorola in the following forms, in order of preference:

1. Hexadecimal coding using IBM Punch Cards (Figures 3 and 4).
2. Hexadecimal coding using ASCII Paper Tape Punch (Figure 5).

Programming of the MCM6670 can be achieved by using the following sequence:

1. Create the 128 characters in a 5 x 7 font using the format shown in Figure 1. Note that information at output D4 appears in column one, D3 in column two, thru D0 information in column five. The dots filled in and programmed as a logic "1" will appear at the outputs as V_{OH}; the dots left blank will be at V_{OL}. RO is always programmed to be blank (V_{OL}). (Blank formats appear at the end of this data sheet for your convenience; they are not to be submitted to Motorola, however.)

2. Convert the characters to hexadecimal coding treating dots as ones and blanks as zeros, and enter this information in the blocks to the right of the character font format. The information for D4 must be a hex one or zero, and is entered in the left block. The information for D3 thru D0 is entered in the right block, with D3 the most significant bit for the hex coding, and D0 the least significant.

3. Transfer the hexadecimal figures either to punched cards (Figure 3) or to paper tape (Figure 5).

4. Transmit this data to Motorola, along with the customer name, customer part number and revision, and an indication that the source device is the MCM6670.

5. Information should be submitted on an organizational data form such as that shown in Figure 2.

FIGURE 1 – CHARACTER FORMAT

ROW SELECT
TRUTH TABLE

RS3	RS2	RS1	OUTPUT
0	0	0	R0
0	0	1	R1
0	1	0	R2
0	1	1	R3
1	0	0	R4
1	0	1	R5
1	1	0	R6
1	1	1	R7

Character Number (CUSTOMER INPUT)

		MSB			LSB	HEX	
R0	☐	☐	☐	☐	☐	0	0
R1	☐	☐	☒	☐	☐	0	4
R2	☐	☒	☐	☒	☐	0	A
R3	☒	☐	☐	☐	☒	1	1
R4	☒	☐	☐	☐	☒	1	1
R5	☒	☒	☒	☒	☒	1	F
R6	☒	☐	☐	☐	☒	1	1
R7	☒	☐	☐	☐	☒	1	1
	D4	D3			D0		

Character Number (CUSTOMER INPUT)

		MSB			LSB	HEX	
R0	☐	☐	☐	☐	☐	0	0
R1	☒	☒	☒	☒	☒	1	F
R2	☒	☐	☐	☐	☐	1	0
R3	☒	☐	☐	☐	☐	1	0
R4	☒	☒	☒	☐	☐	1	C
R5	☒	☐	☐	☐	☐	1	0
R6	☒	☐	☐	☐	☐	1	0
R7	☒	☒	☒	☒	☒	1	F
	D4	D3			D0		

FIGURE 2 – FORMAT FOR PROGRAMMING GENERAL OPTIONS

ORGANIZATIONAL DATA
MCM6670 MOS READ ONLY MEMORY

Customer:

Company ____________________

Part No. ____________________

Originator ____________________

Phone No. ____________________

Motorola Use Only:

Quote: ____________________

Part No.: ____________________

Specif. No.: ____________________

Chip-Select Options:

	Active High 1	Active Low 0	No-Connect
CS	☐	☐	☐

FIGURE 3 – CARD PUNCH FORMAT

Columns	
1-9	Blank
10-25	Hex coding for first character
26	Slash (/)
27-42	Hex coding for second character
43	Slash (/)
44-59	Hex coding for third character
60	Slash (/)
61-76	Hex coding for fourth character
77-78	Blank
79-80	Card number (starting 01; thru 32)

Column 10 on the first card contains either a zero or a one to program D4 of row R0 for the first character. Column 11 contains the hex character for D3 thru D0. Columns 12 and 13 contain the information to program R1. The entire first character is coded in columns 10 thru 25. Each card contains the coding for four characters; 32 cards are required to program the entire 128 characters. The characters must be programmed in sequence from the first character to the last in order to establish proper addressing for the part. Figure 3 provides an illustration of the correct format.

FIGURE 4 – EXAMPLE OF CARD PUNCH FORMAT
(First 12 Characters of MCM6670P4)

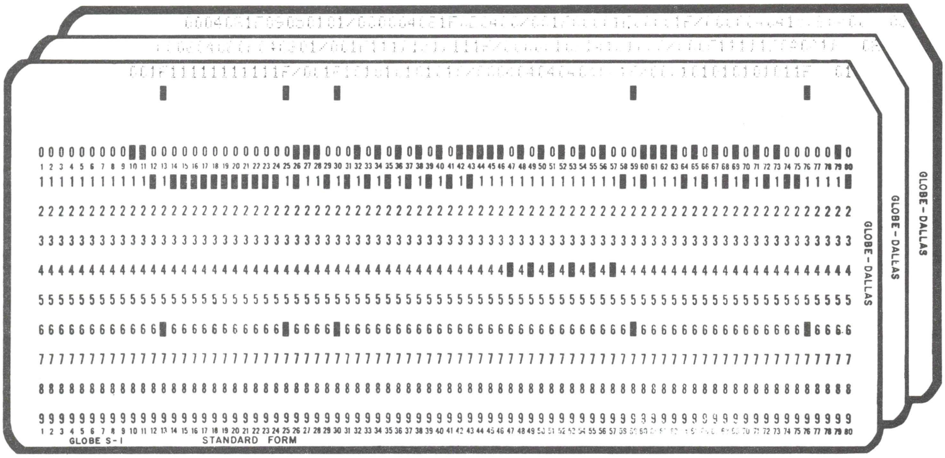


FIGURE 5 – PAPER TAPE FORMAT

Frames	
Leader	Blank Tape
1 to M	Allowed for customer use (M ⩽ 64)
M + 1, M + 2	CR; LF (Carriage Return; Line Feed)
M + 3 to M + 66	First line of pattern information (64 hex figures per line)
M + 67, M + 68	CR; LF
M + 69 to M + 2114	Remaining 31 lines of hex figures, each line followed by a Carriage Return and Line Feed
	Blank Tape

Frames 1 to M are left to the customer for internal identification, where M ⩽ 64. Any combination of alphanumerics may be used. This information is terminated with a Carriage Return and Line Feed, delineating the start of data entry. (Note that the tape cannot begin with a CR and/or LF, or the customer identification will be assumed to be programming data.)

Frame M + 3 contains a zero or a one to program D4 of row R0 for the first character. Frame M + 4 contains the hex character for D3 thru D0, completing the programming information for R0. Frames M + 5 and M + 6 contain the information to program R1. The entire first character is coded in Frames M + 3 thru M + 18. Four complete characters are programmed with each line. A total of 32 lines program all 128 characters (32 x 4). The characters must be programmed in sequence from the first character to the last in order to establish proper addressing for the part.

The formats below are given for your convenience in preparing character information for MCM6670 programming. THESE FORMATS ARE NOT TO BE USED TO TRANSMIT THE INFORMATION TO MOTOROLA. Refer to the Custom Programming instructions for detailed procedures.

Character Number ____________

		MSB			LSB	HEX	
R0	☐	☐	☐	☐	☐	0	0
R1	☐	☐	☐	☐	☐		
R2	☐	☐	☐	☐	☐		
R3	☐	☐	☐	☐	☐		
R4	☐	☐	☐	☐	☐		
R5	☐	☐	☐	☐	☐		
R6	☐	☐	☐	☐	☐		
R7	☐	☐	☐	☐	☐		
	D4	D3			D0		

Character Number ____________

		MSB			LSB	HEX	
R0	☐	☐	☐	☐	☐	0	0
R1	☐	☐	☐	☐	☐		
R2	☐	☐	☐	☐	☐		
R3	☐	☐	☐	☐	☐		
R4	☐	☐	☐	☐	☐		
R5	☐	☐	☐	☐	☐		
R6	☐	☐	☐	☐	☐		
R7	☐	☐	☐	☐	☐		
	D4	D3			D0		

Character Number ____________

		MSB			LSB	HEX	
R0	☐	☐	☐	☐	☐	0	0
R1	☐	☐	☐	☐	☐		
R2	☐	☐	☐	☐	☐		
R3	☐	☐	☐	☐	☐		
R4	☐	☐	☐	☐	☐		
R5	☐	☐	☐	☐	☐		
R6	☐	☐	☐	☐	☐		
R7	☐	☐	☐	☐	☐		
	D4	D3			D0		

Character Number ____________

		MSB			LSB	HEX	
R0	☐	☐	☐	☐	☐	0	0
R1	☐	☐	☐	☐	☐		
R2	☐	☐	☐	☐	☐		
R3	☐	☐	☐	☐	☐		
R4	☐	☐	☐	☐	☐		
R5	☐	☐	☐	☐	☐		
R6	☐	☐	☐	☐	☐		
R7	☐	☐	☐	☐	☐		
	D4	D3			D0		

Character Number ____________

		MSB			LSB	HEX	
R0	☐	☐	☐	☐	☐	0	0
R1	☐	☐	☐	☐	☐		
R2	☐	☐	☐	☐	☐		
R3	☐	☐	☐	☐	☐		
R4	☐	☐	☐	☐	☐		
R5	☐	☐	☐	☐	☐		
R6	☐	☐	☐	☐	☐		
R7	☐	☐	☐	☐	☐		
	D4	D3			D0		

Character Number ____________

		MSB			LSB	HEX	
R0	☐	☐	☐	☐	☐	0	0
R1	☐	☐	☐	☐	☐		
R2	☐	☐	☐	☐	☐		
R3	☐	☐	☐	☐	☐		
R4	☐	☐	☐	☐	☐		
R5	☐	☐	☐	☐	☐		
R6	☐	☐	☐	☐	☐		
R7	☐	☐	☐	☐	☐		
	D4	D3			D0		

Character Number ____________

		MSB			LSB	HEX	
R0	☐	☐	☐	☐	☐	0	0
R1	☐	☐	☐	☐	☐		
R2	☐	☐	☐	☐	☐		
R3	☐	☐	☐	☐	☐		
R4	☐	☐	☐	☐	☐		
R5	☐	☐	☐	☐	☐		
R6	☐	☐	☐	☐	☐		
R7	☐	☐	☐	☐	☐		
	D4	D3			D0		

Character Number ____________

		MSB			LSB	HEX	
R0	☐	☐	☐	☐	☐	0	0
R1	☐	☐	☐	☐	☐		
R2	☐	☐	☐	☐	☐		
R3	☐	☐	☐	☐	☐		
R4	☐	☐	☐	☐	☐		
R5	☐	☐	☐	☐	☐		
R6	☐	☐	☐	☐	☐		
R7	☐	☐	☐	☐	☐		
	D4	D3			D0		

Character Number ____________

		MSB			LSB	HEX	
R0	☐	☐	☐	☐	☐	0	0
R1	☐	☐	☐	☐	☐		
R2	☐	☐	☐	☐	☐		
R3	☐	☐	☐	☐	☐		
R4	☐	☐	☐	☐	☐		
R5	☐	☐	☐	☐	☐		
R6	☐	☐	☐	☐	☐		
R7	☐	☐	☐	☐	☐		
	D4	D3			D0		

Character Number ____________

		MSB			LSB	HEX	
R0	☐	☐	☐	☐	☐	0	0
R1	☐	☐	☐	☐	☐		
R2	☐	☐	☐	☐	☐		
R3	☐	☐	☐	☐	☐		
R4	☐	☐	☐	☐	☐		
R5	☐	☐	☐	☐	☐		
R6	☐	☐	☐	☐	☐		
R7	☐	☐	☐	☐	☐		
	D4	D3			D0		

Character Number ____________

		MSB			LSB	HEX	
R0	☐	☐	☐	☐	☐	0	0
R1	☐	☐	☐	☐	☐		
R2	☐	☐	☐	☐	☐		
R3	☐	☐	☐	☐	☐		
R4	☐	☐	☐	☐	☐		
R5	☐	☐	☐	☐	☐		
R6	☐	☐	☐	☐	☐		
R7	☐	☐	☐	☐	☐		
	D4	D3			D0		

Character Number ____________

		MSB			LSB	HEX	
R0	☐	☐	☐	☐	☐	0	0
R1	☐	☐	☐	☐	☐		
R2	☐	☐	☐	☐	☐		
R3	☐	☐	☐	☐	☐		
R4	☐	☐	☐	☐	☐		
R5	☐	☐	☐	☐	☐		
R6	☐	☐	☐	☐	☐		
R7	☐	☐	☐	☐	☐		
	D4	D3			D0		

Character Number ____________

		MSB			LSB	HEX	
R0	☐	☐	☐	☐	☐	0	0
R1	☐	☐	☐	☐	☐		
R2	☐	☐	☐	☐	☐		
R3	☐	☐	☐	☐	☐		
R4	☐	☐	☐	☐	☐		
R5	☐	☐	☐	☐	☐		
R6	☐	☐	☐	☐	☐		
R7	☐	☐	☐	☐	☐		
	D4	D3			D0		

Character Number ____________

		MSB			LSB	HEX	
R0	☐	☐	☐	☐	☐	0	0
R1	☐	☐	☐	☐	☐		
R2	☐	☐	☐	☐	☐		
R3	☐	☐	☐	☐	☐		
R4	☐	☐	☐	☐	☐		
R5	☐	☐	☐	☐	☐		
R6	☐	☐	☐	☐	☐		
R7	☐	☐	☐	☐	☐		
	D4	D3			D0		

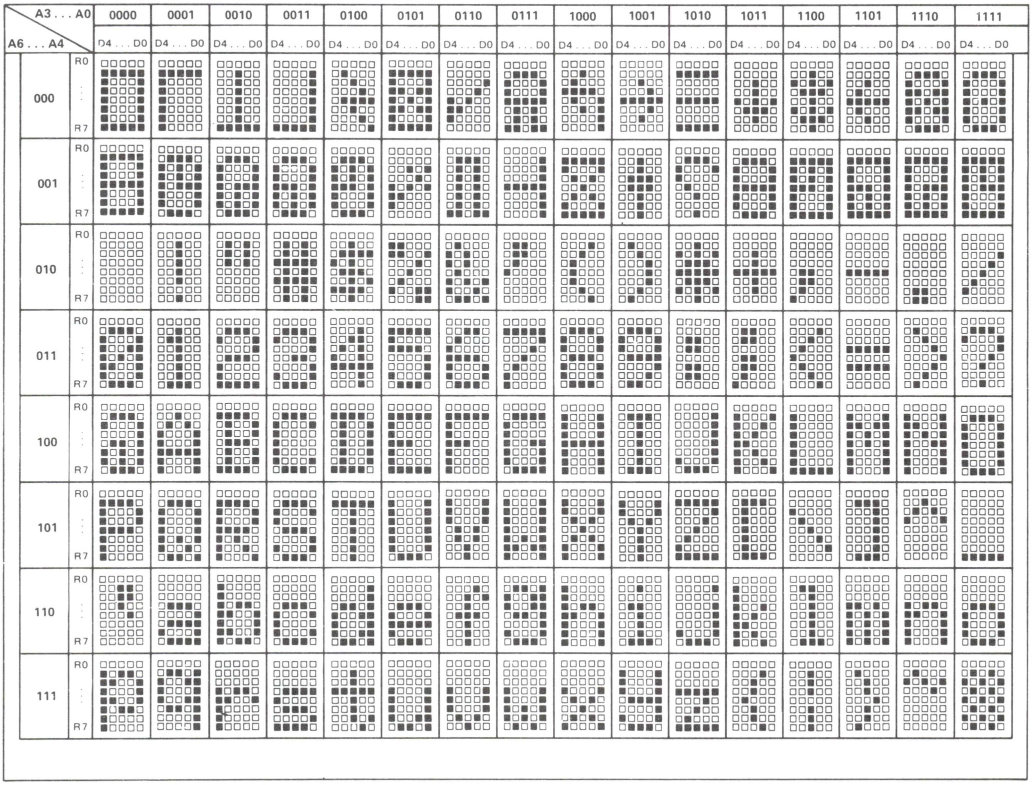
Character Number ____________

		MSB			LSB	HEX	
R0	☐	☐	☐	☐	☐	0	0
R1	☐	☐	☐	☐	☐		
R2	☐	☐	☐	☐	☐		
R3	☐	☐	☐	☐	☐		
R4	☐	☐	☐	☐	☐		
R5	☐	☐	☐	☐	☐		
R6	☐	☐	☐	☐	☐		
R7	☐	☐	☐	☐	☐		
	D4	D3			D0		

Character Number ____________

		MSB			LSB	HEX	
R0	☐	☐	☐	☐	☐	0	0
R1	☐	☐	☐	☐	☐		
R2	☐	☐	☐	☐	☐		
R3	☐	☐	☐	☐	☐		
R4	☐	☐	☐	☐	☐		
R5	☐	☐	☐	☐	☐		
R6	☐	☐	☐	☐	☐		
R7	☐	☐	☐	☐	☐		
	D4	D3			D0		

FIGURE 6 – MCM6674 PATTERN


A3 . . . A0
A6 . . . A4
0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111
D4 . . . D0
000
001
010
011
100
101
110
111
R0
R7

MOTOROLA

MCM66700 MCM66710
MCM66714 MCM66720
MCM66730 MCM66734
MCM66740 MCM66750
MCM66751 MCM66760
MCM66770 MCM66780
MCM66790

8192-BIT READ ONLY MEMORIES
ROW SELECT CHARACTER GENERATORS

The MCM66700 is a mask-programmable 8192-bit horizontal-scan (row select) character generator. It contains 128 characters in a 7 X 9 matrix, and has the capability of shifting certain characters that normally extend below the baseline such as j, y, g, p, and q. Circuitry is supplied internally to effectively lower the whole matrix for this type of character—a feature previously requiring external circuitry.

A seven-bit address code is used to select one of the 128 available characters. Each character is defined as a specific combination of logic 1s and 0s stored in a 7 X 9 matrix. When a specific four-bit binary row select code is applied, a word of seven parallel bits appears at the output. The rows can be sequentially selected, providing a nine-word sequence of seven parallel bits per word for each character selected by the address inputs. As the row select inputs are sequentially addressed, the devices will automatically place the 7 X 9 character in one of two preprogrammed positions on the 16-row matrix, with the positions defined by the four row select inputs. Rows that are not part of the character are automatically blanked.

The devices listed are preprogrammed versions of the MCM66700. They contain various sets of characters to meet the requirements of diverse applications. The complete patterns of these devices are contained in this data sheet.

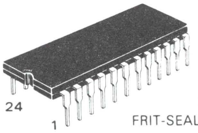
- Fully Static Operation
- Fully TTL Compatible with Three-State Outputs
- CMOS and MPU Compatible, Single ±10% 5 Volt Supply
- Shifted Character Capability
  (Except MCM66720, MCM66730, and MCM66734)
- Maximum Access Time = 350 ns
- 4 Programmable Chip Selects (0, 1, or X)
- Pin-for-Pin Replacement for the MCM6570, Including All Standard Patterns

MOS

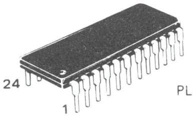
(N-CHANNEL, SILICON-GATE)

8K READ ONLY MEMORIES

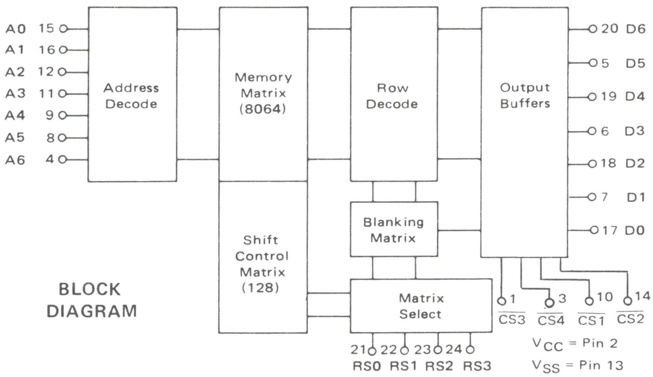
HORIZONTAL-SCAN
CHARACTER GENERATORS
WITH SHIFTED CHARACTERS



C SUFFIX
FRIT-SEAL CERAMIC PACKAGE
CASE 623

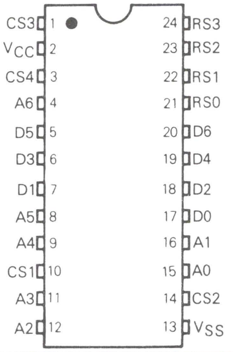


P SUFFIX
PLASTIC PACKAGE
CASE 709


A0 15
A1 16
A2 12
A3 11
A4 9
A5 8
A6 4
Address Decode
Memory Matrix (8064)
Shift Control Matrix (128)
Row Decode
Blanking Matrix
Matrix Select
Output Buffers
20 D6
5 D5
19 D4
6 D3
18 D2
7 D1
17 D0
1 CS3
3 CS4
10 CS1
14 CS2
21 RS0
22 RS1
23 RS2
24 RS3
VCC = Pin 2
VSS = Pin 13

BLOCK DIAGRAM

PIN ASSIGNMENT


CS3 1
VCC 2
CS4 3
A6 4
D5 5
D3 6
D1 7
A5 8
A4 9
CS1 10
A3 11
A2 12
24 RS3
23 RS2
22 RS1
21 RS0
20 D6
19 D4
18 D2
17 D0
16 A1
15 A0
14 CS2
13 VSS

ABSOLUTE MAXIMUM RATINGS (See Note 1, Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
Supply Voltages	V_{CC}	−0.3 to 7.0	Vdc
Input Voltage	V_{in}	−0.3 to 7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher-than-recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED DC OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	Vdc
Input Logic "1" Voltage	V_{IH}	2.0	–	V_{CC}	Vdc
Input Logic "0" Voltage	V_{IL}	-0.3	–	0.8	Vdc

DC CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IH} = 5.5 Vdc, V_{CC} = 4.5 Vdc)	I_{IH}	–	–	2.5	μAdc
Output Low Voltage (Blank) (I_{OL} = 1.6 mAdc)	V_{OL}	0	–	0.4	Vdc
Output High Voltage (Dot) (I_{OH} = −205 μAdc)	V_{OH}	2.4	–	–	Vdc
Power Supply Current	I_{CC}	–	–	80	mAdc
Power Dissipation	P_D	–	200	440	mW

CAPACITANCE (Periodically sampled rather than 100% tested)

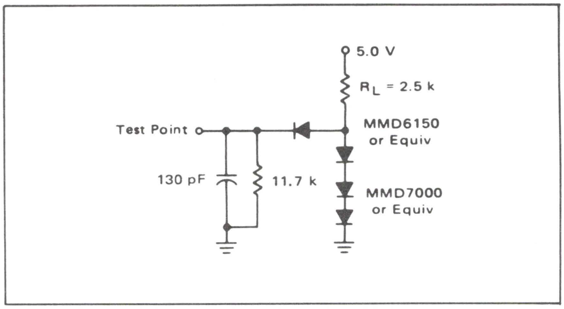
Input Capacitance (f = 1.0 MHz)	C_{in}	–	4.0	7.0	pF
Output Capacitance (f = 1.0 MHz)	C_{out}	–	4.0	7.0	pF

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

AC TEST LOAD


5.0 V
R_L = 2.5 k
Test Point
MMD6150
or Equiv
130 pF
11.7 k
MMD7000
or Equiv

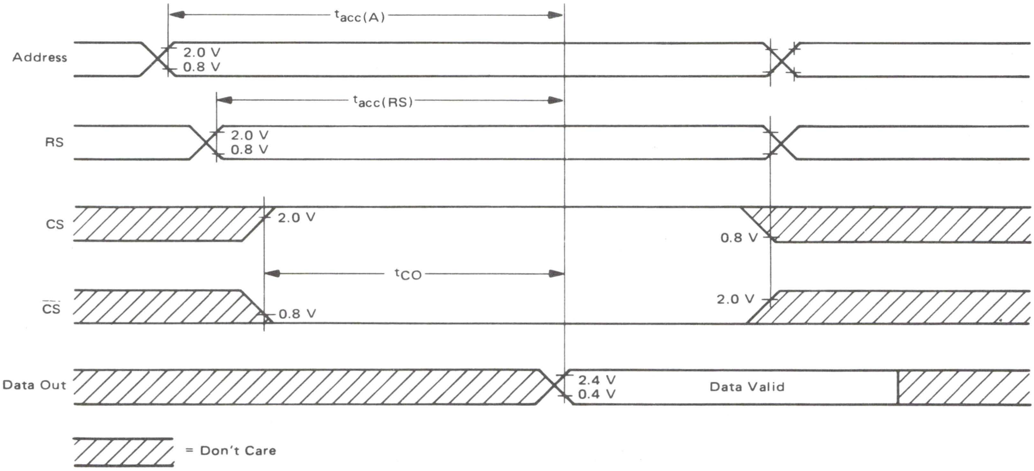
AC TEST CONDITIONS

Condition	Value
Input Pulse Levels	0.8 V to 2.0 V
Input Rise and Fall Times	20 ns
Output Load	1 TTL Gate and C_L = 130 pF

AC CHARACTERISTICS

Characteristic	Symbol	Typ	Max	Unit
Address Access Time	$t_{acc(A)}$	250	350	ns
Row Select Access Time	$t_{acc(RS)}$	250	350	ns
Chip Select to Output Delay	t_{CO}	100	150	ns

TIMING DIAGRAM


$t_{acc(A)}$
Address
2.0 V
0.8 V
$t_{acc(RS)}$
RS
2.0 V
0.8 V
CS
2.0 V
0.8 V
t_{CO}
$\overline{CS}$
0.8 V
2.0 V
Data Out
2.4 V
0.4 V
Data Valid
= Don't Care

MEMORY OPERATION (Using Positive Logic)

Most positive level = 1, most negative level = 0.

Address

To select one of the 128 characters, apply the appropriate binary code to the Address inputs (A0 through A6).

Row Select

To select one of the rows of the addressed character to appear at the seven output lines, apply the appropriate binary code to the Row Select inputs (RS0 through RS3).

Shifted Characters

These devices have the capability of displaying characters that descend below the bottom line (such as lowercase letters j, y, g, p, and q). Internal circuitry effectively drops the whole matrix for this type of character. Any character can be programmed to occupy either of the two positions in a 7 X 16 matrix. (Shifted characters are not available on MCM66720, MCM66730, or MCM66734.)

Output

For these devices, an output dot is defined as a logic 1 level, and an output blank is defined as a logic 0 level.

Programmable Chip Select

The MCM66700 has four Chip Select inputs that can be programmed with a 1, 0, or don't care (not connected). A don't care must always be the highest chip select pin or pins. All standard patterns have Don't Care Chip Select—except MCM66751.

DISPLAY FORMAT

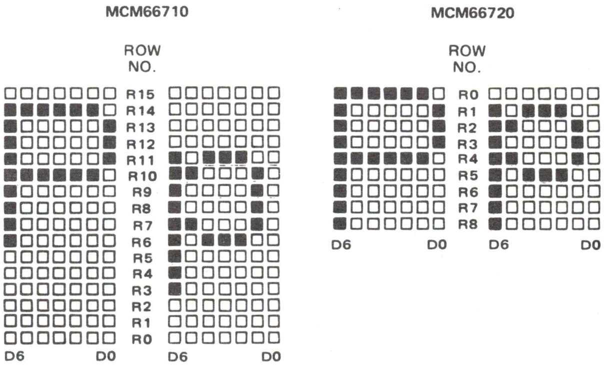
Figure 1 shows the relationship between the logic levels at the row select inputs and the character row at the outputs. The MCM66700 allows the user to locate the basic 7 X 9 font anywhere in the 7 X 16 array. In addition, a shifted font can be placed anywhere in the same 7 X 16 array. For example, the basic MCM66710 font is established in rows R14 through R6. All other rows are automatically blanked. The shifted font is established in rows R11 through R3, with all other rows blanked. Thus, while any one character is contained in a 7 X 9 array, the MCM66710 requires a 7 X 12 array on the CRT screen to contain both normal and descending characters. Other uses of the shift option may require as much as the full 7 X 16 array, or as little as the basic 7 X 9 array (when no shifting occurs, as in the MCM66720).

The MCM66700 can be programmed to be scanned either from bottom to top or from top to bottom. This is achieved through the option of assigning row numbers in ascending or descending count, as long as both the basic font and the shifted font are the same. For example, an up counter will scan the MCM66710 from bottom to top, whereas an up counter will scan the MCM66714 from top to bottom (see Figures 7 and 8 for row designation).

FIGURE 1 — ROW SELECT INPUT CODE AND SAMPLE CHARACTERS FOR MCM66710 AND MCM66720

ROW SELECT TRUTH TABLE

RS3	RS2	RS1	RS0	OUTPUT
0	0	0	0	R0
0	0	0	1	R1
0	0	1	0	R2
0	0	1	1	R3
0	1	0	0	R4
0	1	0	1	R5
0	1	1	0	R6
0	1	1	1	R7
1	0	0	0	R8
1	0	0	1	R9
1	0	1	0	R10
1	0	1	1	R11
1	1	0	0	R12
1	1	0	1	R13
1	1	1	0	R14
1	1	1	1	R15



CUSTOM PROGRAMMING FOR MCM66700

By the programming of a single photomask, the customer may specify the content of the MCM66700. Encoding of the photomask is done with the aid of a computer to provide quick, efficient implementation of the custom bit pattern while reducing the cost of implementation.

Information for the custom memory content may be sent to Motorola in the following forms, in order of preference:*

1. Hexadecimal coding using IBM Punch Cards (Figures 3 and 4)
2. Hexadecimal coding using ASCII Paper Tape Punch (Figure 5)

Programming of the MCM66700 can be achieved by using the follow sequence:

1. Create the 128 characters in a 7 X 9 font using the format shown in Figure 2. Note that information at output D6 appears in column one, D5 in column two, through D0 information in column seven. The dots filled in and programmed as a logic 1 will appear at the outputs as V_{OH}; the dots left blank will be at V_{OL}. (Blank formats appear at the end of this data sheet for your convenience; they are not to be submitted to Motorola, however.)

2. Indicate which characters are shifted by filling in the extra square (dot) in the top row, at the left (column S).

3. Convert the characters to hexadecimal coding treating dots as 1s and blanks as 0s, and enter this information in the blocks to the right of the character font format. High order bits are at the left, in columns S and D3. For the bottom eight rows, the bit in Column S must be 0, so these locations have been omitted. For the top row, the bit in Column S will be 0 for an unshifted character, and 1 for a shifted character.

4. Transfer the hexadecimal figures either to punched cards (Figure 3) or to paper tape (Figure 5).

5. Assign row numbers to the unshifted font. These must be nine sequential numbers (values 0 through 15) assigned consecutively to the rows. The shifted font is similarly placed in any position in the 16 rows.

6. Provide, in writing, the information indicated in Figure 6 (a copy of Figure 10 may be used for this purpose). Submit this information to Motorola together with the punched cards or paper tape.

FIGURE 2 – CHARACTER FORMAT

NON-SHIFTED

Character Number (CUSTOMER INPUT)

MSB LSB HEX

	S	D6		D4	D3			D0	HEX	
R 14	☐	☐	☐	☐	☐	☐	☐	☐	0	0
R 13		☐	☐	☐	☐	☐	☐	☐	0	0
R 12		☐	☐	☐	☐	☐	☐	☐	0	0
R 11		☐	☐	☐	☐	☐	☐	☐	0	0
R 10		☐	☒	☒	☐	☐	☐	☒	3	1
R 9		☒	☐	☐	☒	☐	☒	☐	4	A
R 8		☒	☐	☐	☐	☒	☐	☐	4	4
R 7		☒	☐	☐	☒	☐	☒	☐	4	A
R 6		☐	☒	☒	☐	☐	☐	☒	3	1

SHIFTED

Character Number (CUSTOMER INPUT)

MSB LSB HEX

	S	D6		D4	D3			D0	HEX	
R 11	☒	☐	☒	☒	☒	☒	☐	☐	B	C
R 10		☐	☒	☐	☐	☐	☒	☐	2	2
R 9		☐	☒	☒	☒	☒	☐	☐	3	C
R 8		☐	☒	☐	☐	☐	☒	☐	2	2
R 7		☐	☒	☐	☐	☐	☒	☐	2	2
R 6		☐	☒	☒	☒	☒	☐	☐	3	C
R 5		☐	☒	☐	☐	☐	☐	☐	2	0
R 4		☐	☒	☐	☐	☐	☐	☐	2	0
R 3		☒	☐	☐	☐	☐	☐	☐	4	0

FIGURE 3 – CARD PUNCH FORMAT

Columns	
1 – 10	Blank
11	Asterisk (*)
12 – 29	Hex coding for first character
30	Slash (/)
31 – 48	Hex coding for second character
49	Slash (/)
50 – 67	Hex coding for third character
68	Slash (/)
69 – 76	Blank
77 – 78	Card number (starting 01; through 43)
79 – 80	Blank

Column 12 on the first card contains the hexadecimal equivalent of column S and D6 through D4 for the top row of the first character. Column 13 contains D3 through D0. Columns 14 and 15 contain the information for the next row. The entire first character is coded in columns 12 through 29. Each card contains the coding for three characters. 43 cards are required to program the entire 128 characters, the last card containing only two characters. The characters must be programmed in sequence from the first character to the last in order to establish proper addressing for the part. As an example, the first nine characters of the MCM66710 are correctly coded and punched in Figure 4.

---

*NOTE: Motorola can accept magnetic tape and truth table formats. For further information contact your local Motorola sales representative.

FIGURE 4 – EXAMPLE OF CARD PUNCH FORMAT
(First 9 Characters of MCM66710)

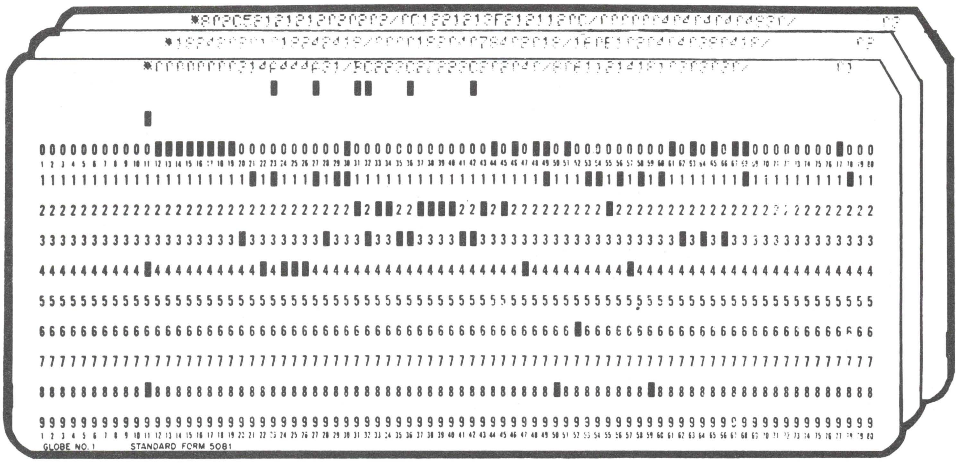


FIGURE 5 – PAPER TAPE FORMAT

Frames	
Leader	Blank Tape
1 to M	Allowed for customer use (M ⩽ 64)
M + 1, M + 2	CR; LF (Carriage Return; Line Feed)
M + 3 to M + 66	First line of pattern information (64 hex figures per line)
M + 67, M + 68	CR; LF
M + 69 to M + 2378	Remaining 35 lines of hex figures, each line followed by a Carriage Return and Line Feed

Blank Tape

Frames 1 to M are left to the customer for internal identification, where M ⩽ 64. Any combination of alphanumerics may be used. This information is terminated with a Carriage Return and Line Feed, delineating the start of data entry. (Note that the tape cannot begin with a CR and/or LF, or the customer identification will be assumed to be programming data.)

Frame M + 3 contains the hexadecimal equivalent of column S and D6 thru D4 for the top row of the first character. Frame M + 4 contains D3 thru D0. Frames M + 5 and M + 6 program the second row of the first character. Frames M + 3 to M + 66 comprise the first line of the printout. The line is terminated with a CR and LF.

The remaining 35 lines of data are punched in sequence using the same format, each line terminated with a CR and LF. The total 36 lines of data contain 36 x 64 or 2304 hex figures. Since 18 hex figures are required to program each 7 x 9 character, the full 128 (2304 ÷ 18) characters are programmed.

FIGURE 6 – FORMAT FOR ORGANIZATIONAL DATA

ORGANIZATIONAL DATA
MCM66700 MOS READ ONLY MEMORY

Customer ______________________________

Customer Part No. ______________________ Rev. __________

Row Number for top row of non-shifted font ______________________

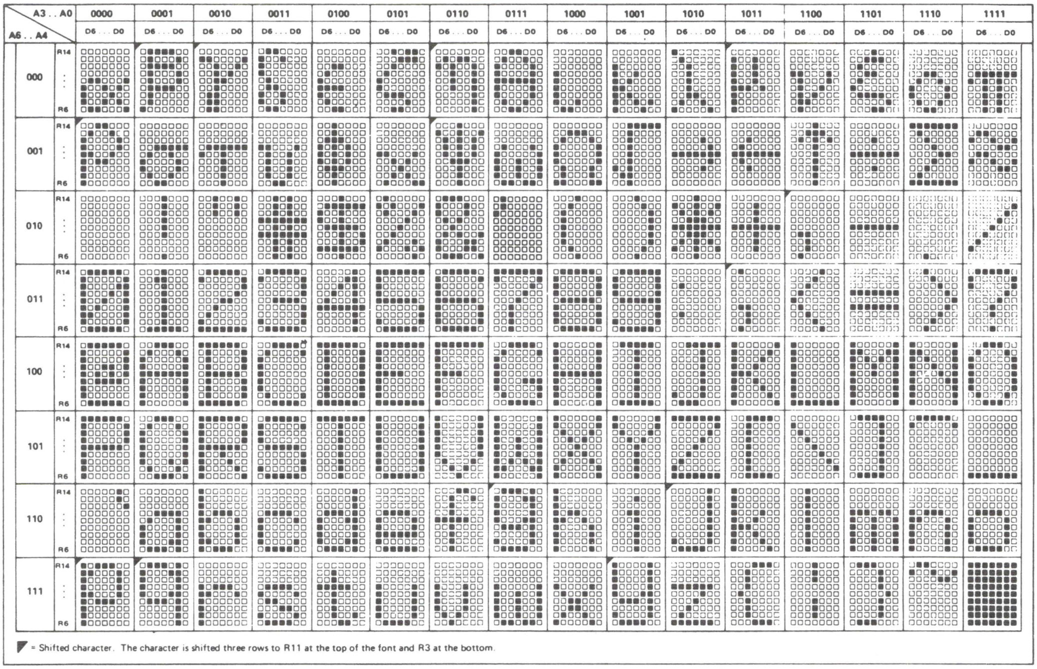
Row Number for bottom row of non-shifted font ______________________

Row Number for top row of shifted font ______________________

Programmable Chip Select information: 1 = Active High 0 = Active Low X = Don't Care (Not Connected)

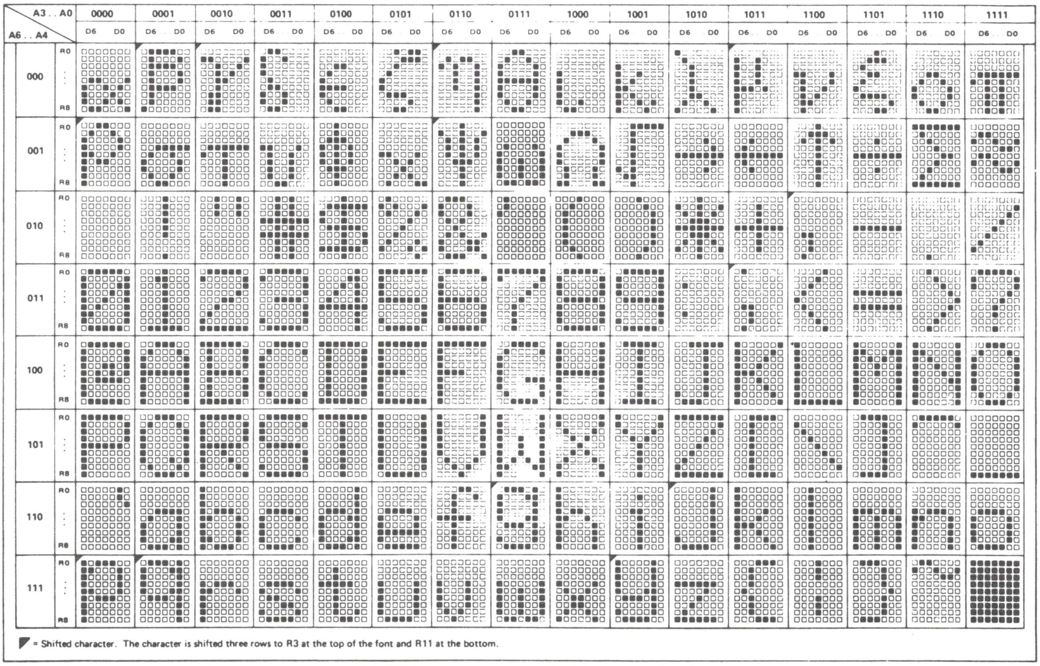
CS1____ CS2____ CS3____ CS4____

FIGURE 7 — MCM66710 PATTERN


A3 . . A0
A6 . . A4
0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111
D6 . . . D0
000
001
010
011
100
101
110
111
R14
R6

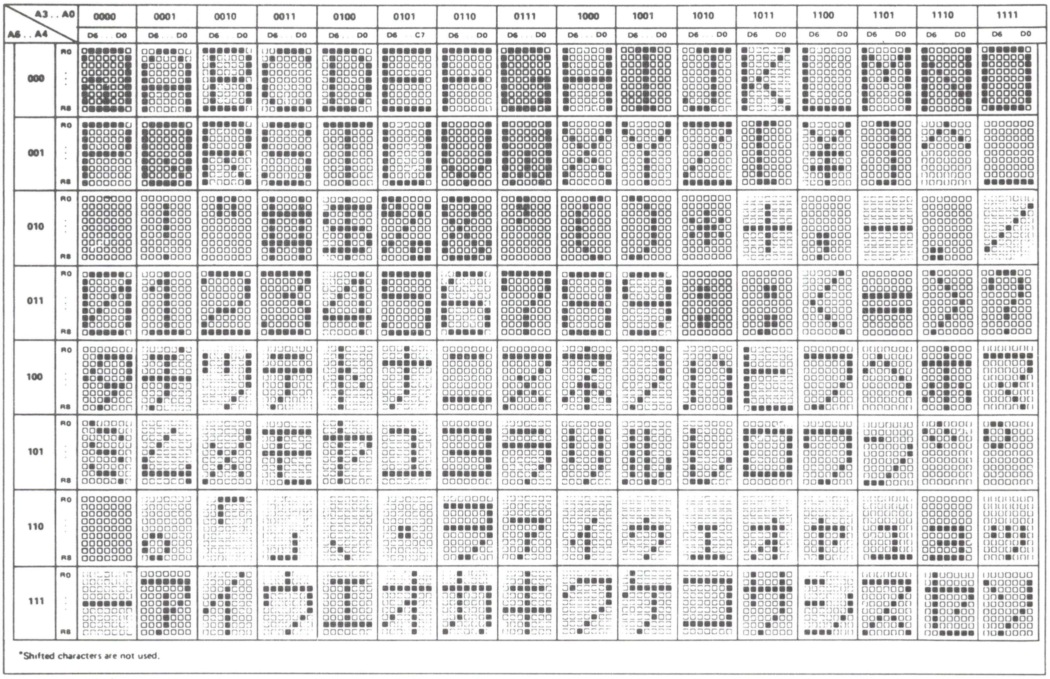
◤ = Shifted character. The character is shifted three rows to R11 at the top of the font and R3 at the bottom.

FIGURE 8 — MCM66714 PATTERN


A3 . . A0
A6 . . A4
0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111
D6 D0
000
001
010
011
100
101
110
111
R0
R8

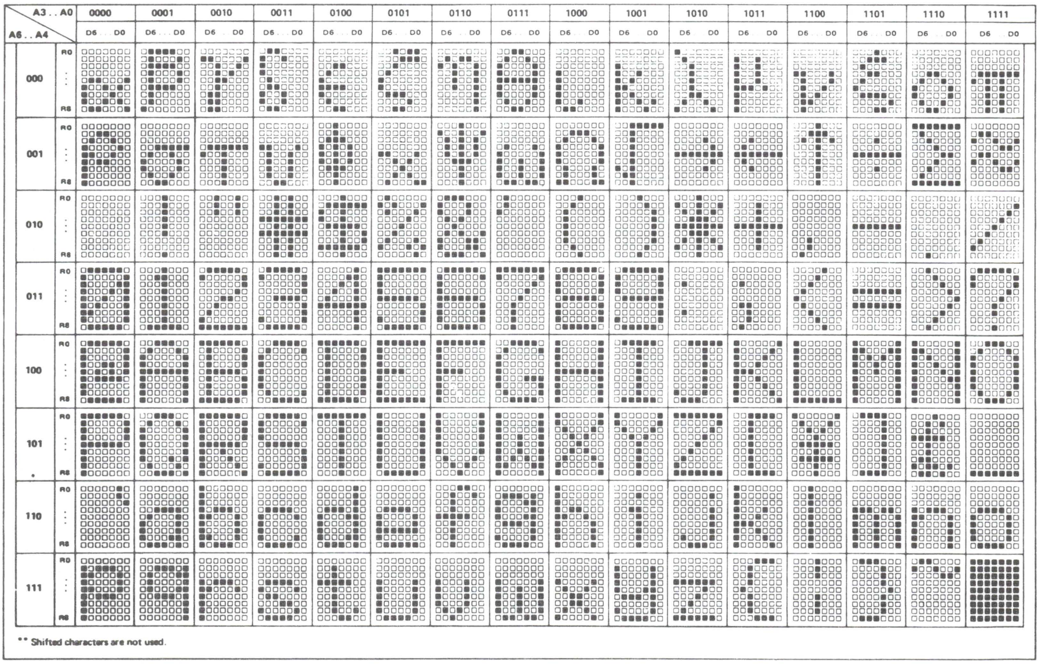
◤ = Shifted character. The character is shifted three rows to R3 at the top of the font and R11 at the bottom.

FIGURE 9 — MCM66734 PATTERN*


A3 .. A0
A6 .. A4
0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111
D6 ... D0
000
001
010
011
100
101
110
111
R0
R8

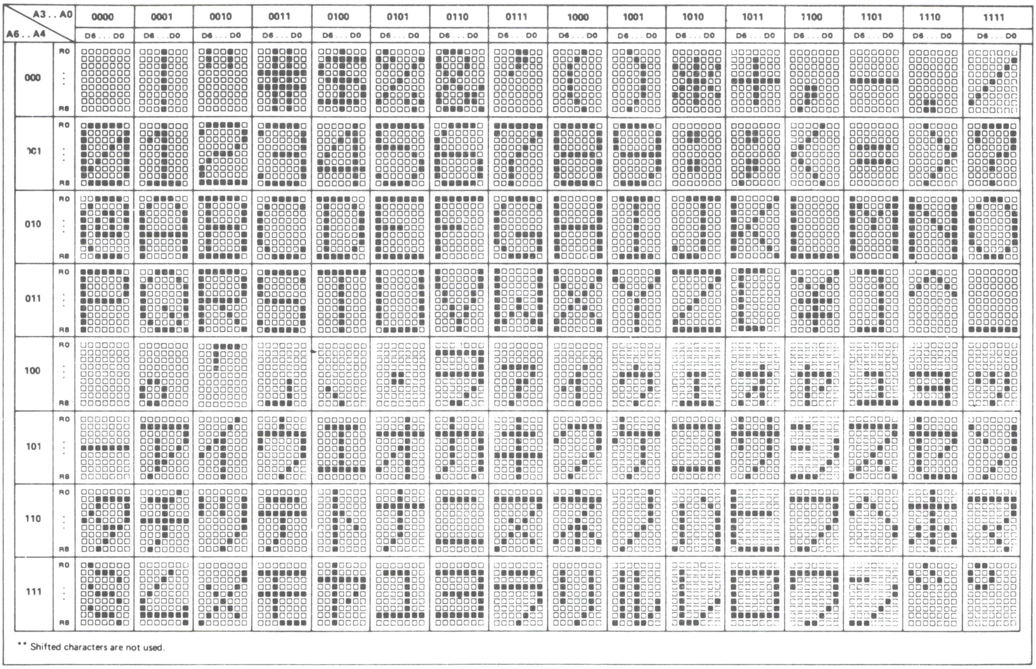
*Shifted characters are not used.

FIGURE 10 — MCM66720 PATTERN**


A3 .. A0
A6 .. A4
0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111
D6 ... D0
000
001
010
011
100
101
110
111
R0
R8

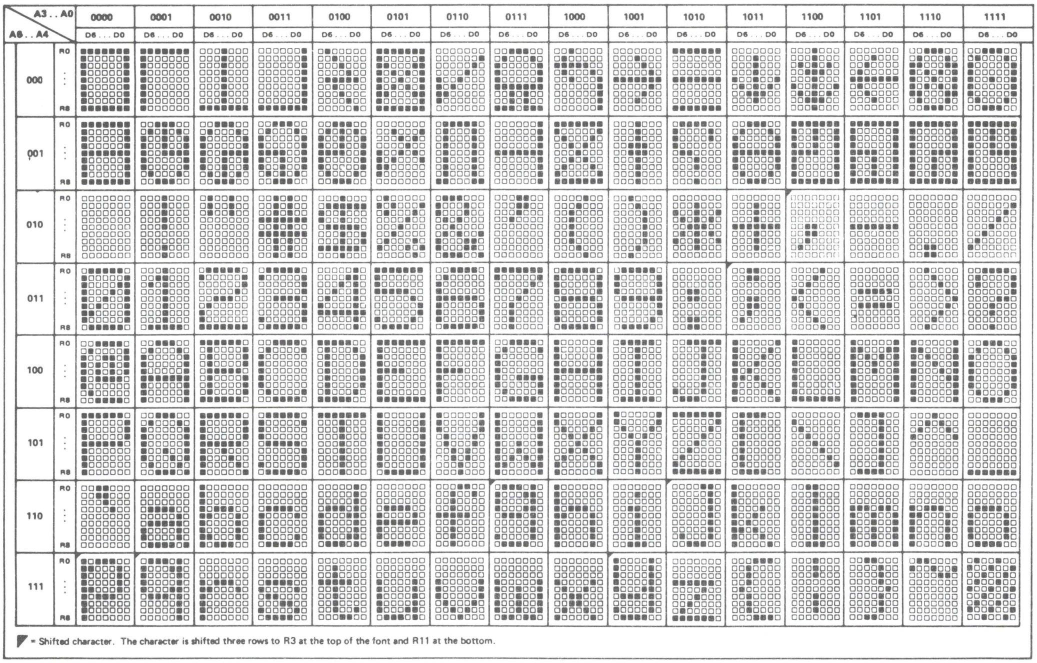
** Shifted characters are not used.

FIGURE 11 — MCM66730 PATTERN**


A3 . . A0
A6 . . A4
0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111
D6 . . . D0
000
001
010
011
100
101
110
111
R0
R8

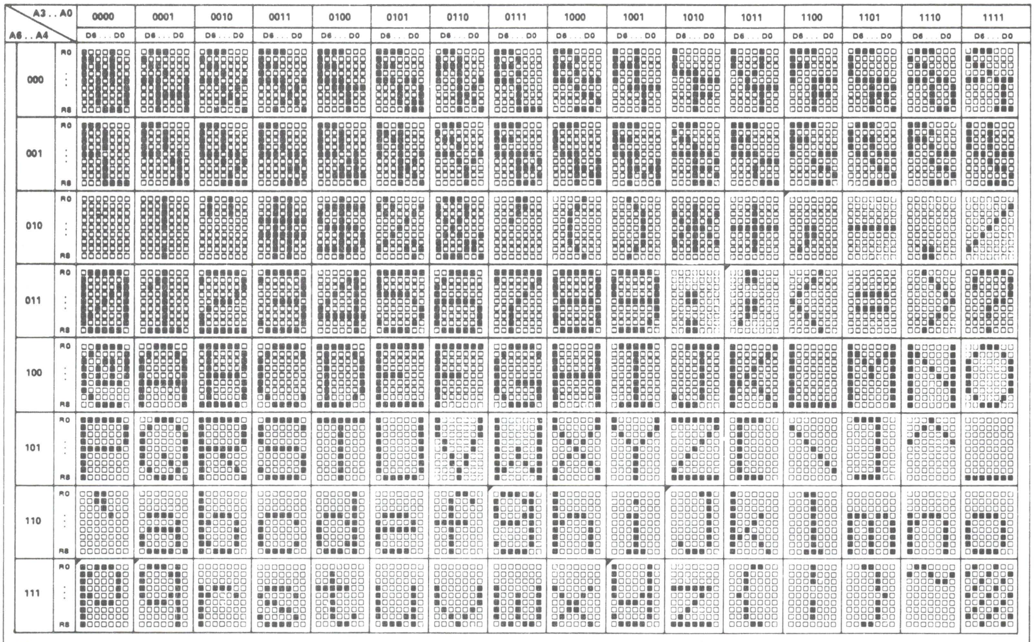
** Shifted characters are not used.

FIGURE 12 — MCM66740 PATTERN


A3 . . A0
A6 . . A4
0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111
D6 . . . D0
000
001
010
011
100
101
110
111
R0
R8

◤ = Shifted character. The character is shifted three rows to R3 at the top of the font and R11 at the bottom.

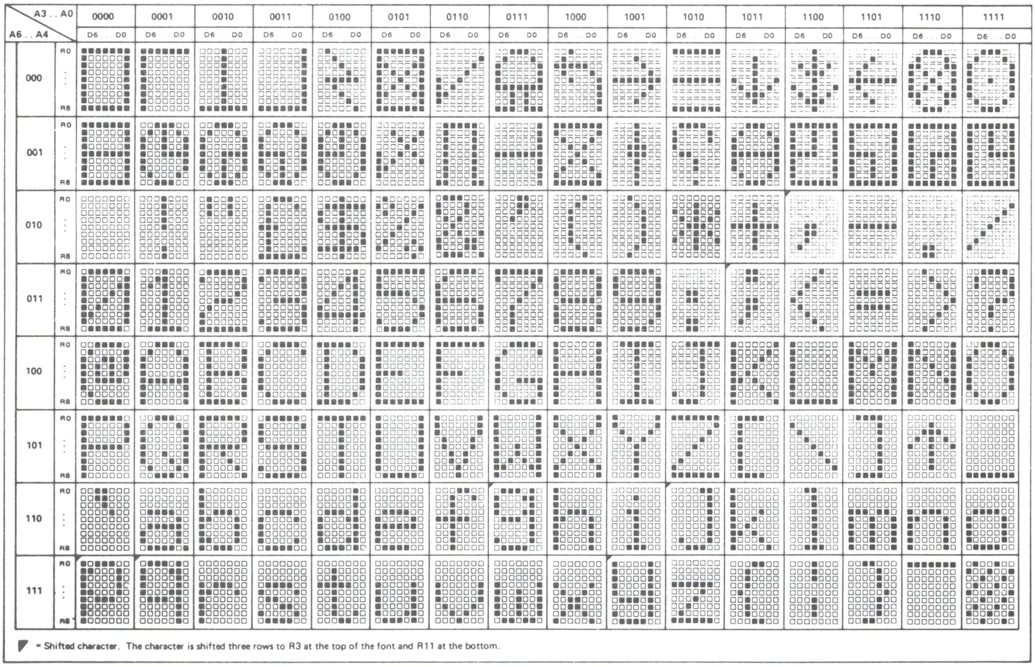
FIGURE 13 — MCM66750 PATTERN


A3 . . A0
A6 . . A4
0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111
D6 . . . D0
000
001
010
011
100
101
110
111
R0
R8

◤ = Shifted character. The character is shifted three rows to R3 at the top of the font and R11 at the bottom.

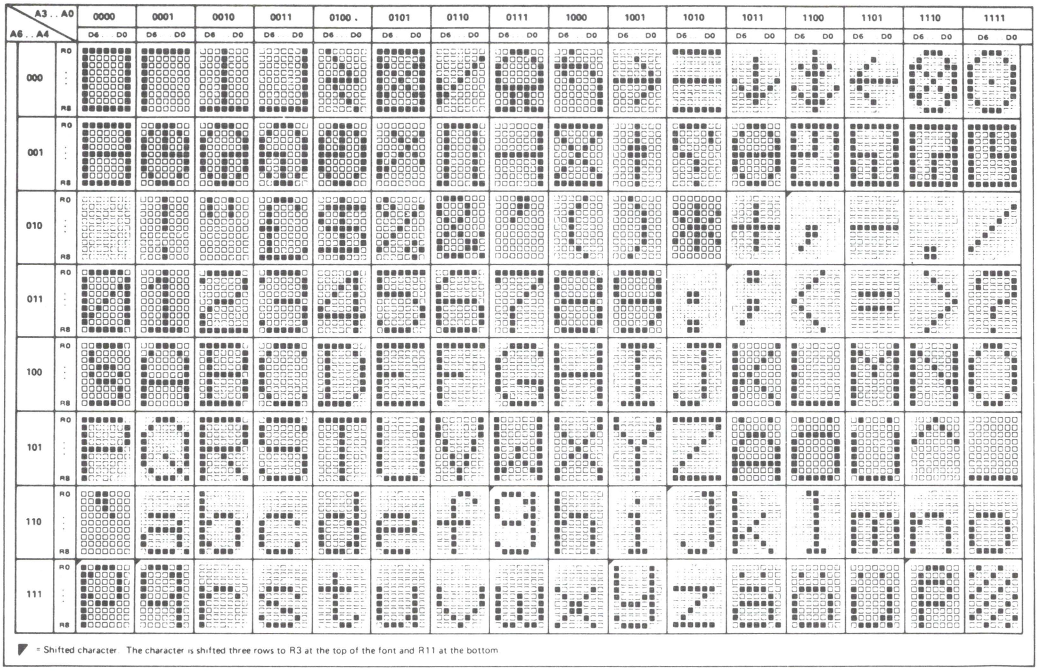
MCM66751 — Same as MCM66750 except CS1 = 0, CS2 = 0, CS3 = X, and CS4 = X.

FIGURE 14 — MCM66760 PATTERN


A3 . . A0
A6 . . A4
0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111
D6 . . . D0
000
001
010
011
100
101
110
111
R0
R8

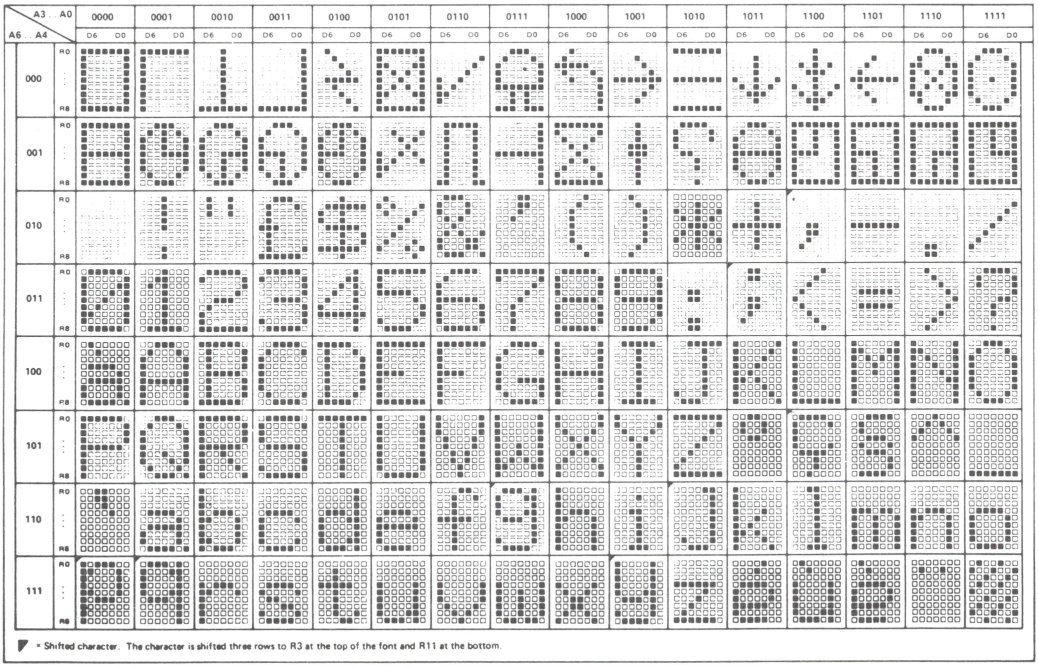
◤ = Shifted character. The character is shifted three rows to R3 at the top of the font and R11 at the bottom.

FIGURE 15 — MCM66770 PATTERN


A3 . . A0
A6 . . A4
0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111
D6 D0
000
001
010
011
100
101
110
111
R0
R8

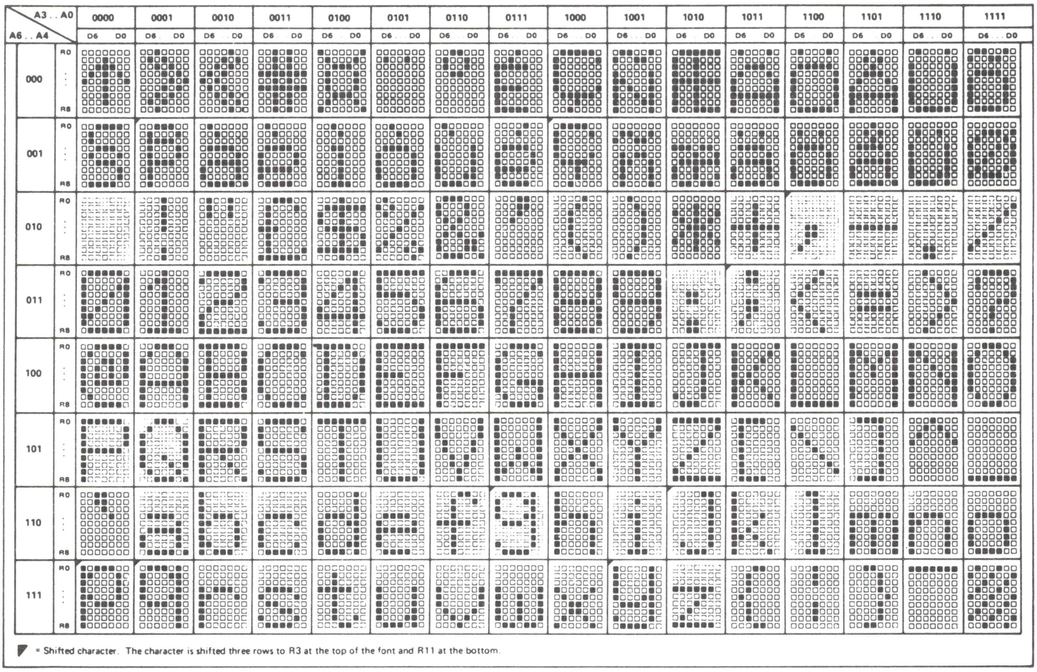
◤ = Shifted character. The character is shifted three rows to R3 at the top of the font and R11 at the bottom.

FIGURE 16 — MCM66780 PATTERN


A3 . . A0
A6 . . A4
0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111
D6 D0
000
001
010
011
100
101
110
111
R0
R8

◤ = Shifted character. The character is shifted three rows to R3 at the top of the font and R11 at the bottom.

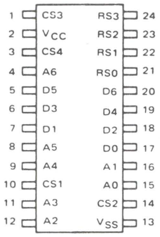
FIGURE 17 — MCM66790 PATTERN


A3 . . A0
A6 . . A4
0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111
D6 . . D0
000
001
010
011
100
101
110
111
R0
R8

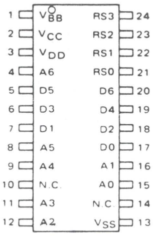
◤ = Shifted character. The character is shifted three rows to R3 at the top of the font and R11 at the bottom.

MCM6570 Series	MCM66700 Equivalent	Description
MCM6571	MCM66710	ASCII, shifted
MCM6571A	MCM66714	ASCII, shifted
MCM6572	MCM66720	ASCII
MCM6573	MCM66730	Japanese
MCM6573A	MCM66734	Japanese
MCM6574	MCM66740	Math Symbols
MCM6575	MCM66750	Alphanumeric Control
MCM6576	MCM66760	British, shifted
MCM6577	MCM66770	German, shifted
MCM6578	MCM66780	French, shifted
MCM6579	MCM66790	European, shifted

MCM66700 Series
Pin Assignment


1 CS3
2 VCC
3 CS4
4 A6
5 D5
6 D3
7 D1
8 A5
9 A4
10 CS1
11 A3
12 A2
24 RS3
23 RS2
22 RS1
21 RS0
20 D6
19 D4
18 D2
17 D0
16 A1
15 A0
14 CS2
13 VSS

MCM6570 Series
Pin Assignment

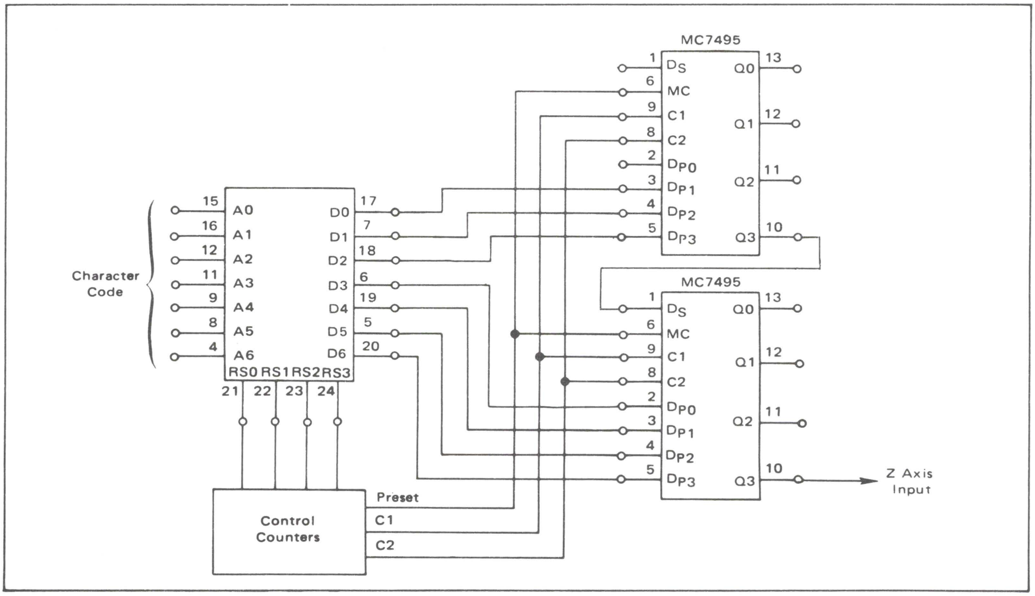

1 VBB
2 VCC
3 VDD
4 A6
5 D5
6 D3
7 D1
8 A5
9 A4
10 N.C.
11 A3
12 A2
24 RS3
23 RS2
22 RS1
21 RS0
20 D6
19 D4
18 D2
17 D0
16 A1
15 A0
14 N.C.
13 VSS

APPLICATIONS INFORMATION

One important application for the MCM66700 series is in CRT display systems (Figure 18). A set of buffer shift registers or random access memories applies a 7-bit character code to the input of the character generator, which then supplies one row of the character according to the count at the four row select inputs. As each row is available, it is put into the TTL MC7495 shift registers. The parallel information in these shift registers is clocked serially out to the Z-axis where it modulates the raster to form the character.

The MCM66700 series require one power supply of +5.0 volts. When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit spikes or glitches on their outputs when the ac power is switched on and off.

FIGURE 18 – CRT DISPLAY APPLICATION USING MCM66710


Character Code
15 A0
16 A1
12 A2
11 A3
9 A4
8 A5
4 A6
D0 17
D1 7
D2 18
D3 6
D4 19
D5 5
D6 20
RS0 RS1 RS2 RS3
21 22 23 24
Control Counters
Preset
C1
C2
MC7495
1 DS
6 MC
9 C1
8 C2
2 DP0
3 DP1
4 DP2
5 DP3
Q0 13
Q1 12
Q2 11
Q3 10
MC7495
Z Axis Input

The formats below are given for your convenience in preparing character information for MCM66700 programming. **THESE FORMATS ARE NOT TO BE USED TO TRANSMIT THE INFORMATION TO MOTOROLA.** Refer to the Custom Programming instructions for detailed procedures.

Character Number ______________

	MSB							LSB	HEX	
R	☐	☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
	S	D6		D4	D3			D0		

Character Number ______________

	MSB							LSB	HEX	
R	☐	☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
	S	D6		D4	D3			D0		

Character Number ______________

	MSB							LSB	HEX	
R	☐	☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
	S	D6		D4	D3			D0		

Character Number ______________

	MSB							LSB	HEX	
R	☐	☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
	S	D6		D4	D3			D0		

Character Number ______________

	MSB							LSB	HEX	
R	☐	☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
	S	D6		D4	D3			D0		

Character Number ______________

	MSB							LSB	HEX	
R	☐	☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
	S	D6		D4	D3			D0		

Character Number ______________

	MSB							LSB	HEX	
R	☐	☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
	S	D6		D4	D3			D0		

Character Number ______________

	MSB							LSB	HEX	
R	☐	☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
	S	D6		D4	D3			D0		

Character Number ______________

	MSB							LSB	HEX	
R	☐	☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
R		☐	☐	☐	☐	☐	☐	☐		
	S	D6		D4	D3			D0		

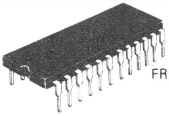
MOTOROLA

MCM68A30A
MCM68B30A

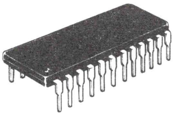
MOS

(N-CHANNEL, SILICON-GATE)

1024 X 8-BIT
READ ONLY MEMORY



C SUFFIX
FRIT-SEAL CERAMIC PACKAGE
CASE 623



P SUFFIX
PLASTIC PACKAGE
CASE 709

1024 X 8-BIT READ ONLY MEMORY

The MCM68A30A/MCM68B30A are mask-programmable byte-organized memories designed for use in bus-organized systems. They are fabricated with N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, has compatibility with TTL and DTL, and needs no clocks or refreshing because of static operation.

The memory is compatible with the M6800 Microcomputer Family, providing read only storage in byte increments. Memory expansion is provided through multiple Chip Select inputs. The active level of the Chip Select inputs and the memory content are defined by the customer.

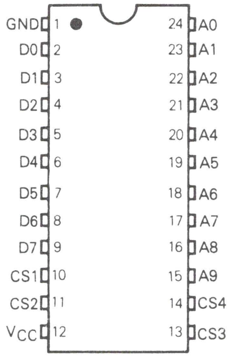
- Organized as 1024 Bytes of 8 Bits
- Static Operation
- Three-State Data Output
- Four Chip Select Inputs (Programmable)
- Single ±10% 5-Volt Power Supply
- TTL Compatible
- Maximum Access Time = 350 ns – MCM68A30A
  250 ns – MCM68B30A

ABSOLUTE MAXIMUM RATINGS (See Note 1)

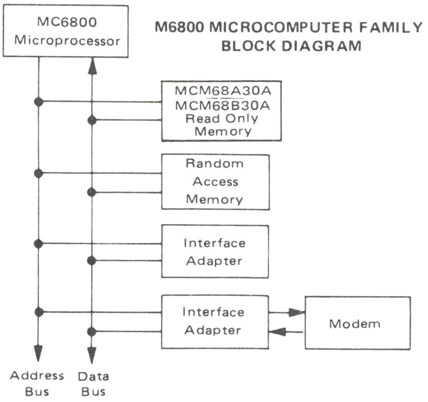
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

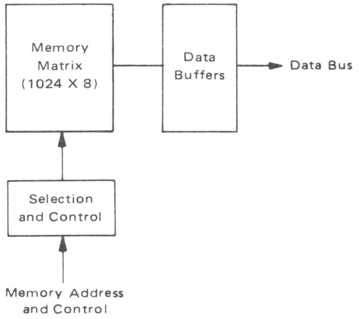
PIN ASSIGNMENT


GND 1
D0 2
D1 3
D2 4
D3 5
D4 6
D5 7
D6 8
D7 9
CS1 10
CS2 11
VCC 12
24 A0
23 A1
22 A2
21 A3
20 A4
19 A5
18 A6
17 A7
16 A8
15 A9
14 CS4
13 CS3

M6800 MICROCOMPUTER FAMILY BLOCK DIAGRAM


MC6800 Microprocessor
MCM68A30A MCM68B30A Read Only Memory
Random Access Memory
Interface Adapter
Interface Adapter
Modem
Address Bus
Data Bus

MCM68A30A/MCM68B30A READ ONLY MEMORY BLOCK DIAGRAM


Memory Matrix (1024 X 8)
Data Buffers
Data Bus
Selection and Control
Memory Address and Control

DS9456 R1/6-78

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	Vdc
Input High Voltage	V_{IH}	2.0	–	5.5	Vdc
Input Low Voltage	V_{IL}	-0.3	–	0.8	Vdc

DC CHARACTERISTICS

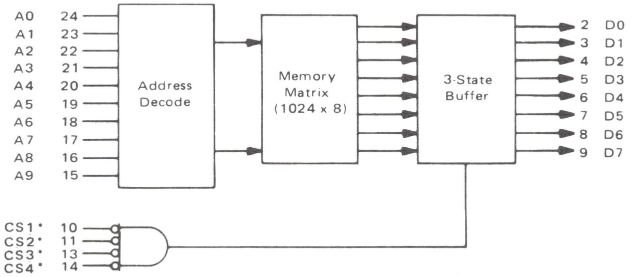
Characteristic	Symbol	Min	Typ	Max	Unit
Input Current (V_{in} = 0 to 5.5 V)	I_{in}	–	–	2.5	μAdc
Output High Voltage (I_{OH} = −205μA)	V_{OH}	2.4	–	–	Vdc
Output Low Voltage (I_{OL} = 1.6 mA)	V_{OL}	–	–	0.4	Vdc
Output Leakage Current (Three-State) (CS = 0.8 V or $\overline{CS}$ = 2.0 V, V_{out} = 0.4 V to 2.4 V)	I_{LO}	–	–	10	μAdc
Supply Current (V_{CC} = 5.5 V, T_A = 0°C)	I_{CC}	–	–	130	mAdc

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Max	Unit
Input Capacitance	C_{in}	7.5	pF
Output Capacitance	C_{out}	12.5	pF

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

BLOCK DIAGRAM



A0 24
A1 23
A2 22
A3 21
A4 20
A5 19
A6 18
A7 17
A8 16
A9 15
Address Decode
Memory Matrix (1024 x 8)
3-State Buffer
2 D0
3 D1
4 D2
5 D3
6 D4
7 D5
8 D6
9 D7
CS1* 10
CS2* 11
CS3* 13
CS4* 14

V_{CC} = Pin 12
Gnd = Pin 1

*Active level defined by the customer.

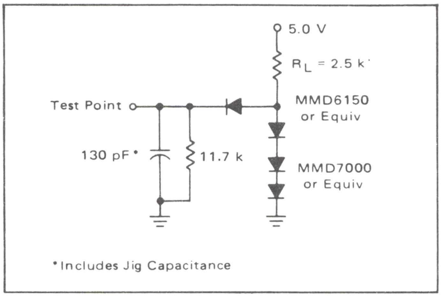
AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted.)

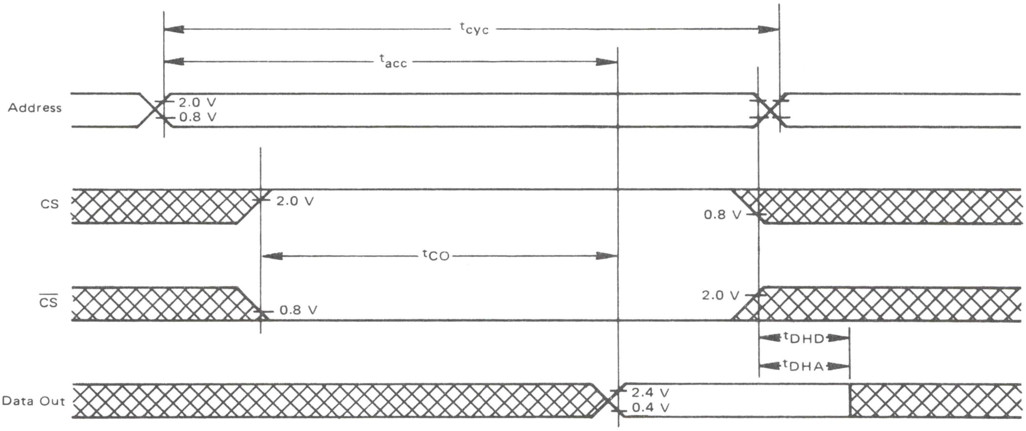
(All timing with $t_r = t_f$ = 20 ns, Load of Figure 1)

Characteristic	Symbol	MCM68A30AL		MCM68B30AL		Unit
		Min	Max	Min	Max	
Cycle Time	t_{cyc}	350	–	250	–	ns
Access Time	t_{acc}	–	350	–	250	ns
Chip Select to Output Delay	t_{CO}	–	150	–	125	ns
Data Hold from Address	t_{DHA}	10	–	10	–	ns
Data Hold from Deselection	t_{DHD}	10	150	10	125	ns

FIGURE 1 – AC TEST LOAD


5.0 V
R_L = 2.5 k
Test Point
MMD6150
or Equiv
130 pF*
11.7 k
MMD7000
or Equiv
*Includes Jig Capacitance

TIMING DIAGRAM


t_{cyc}
t_{acc}
Address
2.0 V
0.8 V
CS
2.0 V
0.8 V
t_{CO}
$\overline{CS}$
0.8 V
2.0 V
t_{DHD}
t_{DHA}
Data Out
2.4 V
0.4 V

CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM68A30A/MCM68B30A, the customer may specify the content of the memory and the method of enabling the outputs.

Information on the general options of the MCM68A30A/MCM68B30A should be submitted on an Organizational Data form such as that shown in Figure 3. ("No Connect" must always be the highest order Chip Select pin(s).)

Information for custom memory content may be sent to Motorola in one of four forms (shown in order of preference):

1. Paper tape output of the Motorola M6800 Software.
2. Hexadecimal coding using IBM Punch Cards.
3. EPROM (MCM2708, MCM27A08, or MCM68708).
4. Hand-punched paper tape (Figure 3).

PAPER TAPE

Included in the software packages developed for the M6800 Microcomputer Family is the ability to produce a paper tape output for computerized mask generation. The assembler directives are used to control allocation of memory, to assign values for stored data, and for controlling the assembly process. The paper tape must specify the full 1024 bytes.

FIGURE 2 – BINARY TO HEXADECIMAL CONVERSION

Binary Data				Hexadecimal Character
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	A
1	0	1	1	B
1	1	0	0	C
1	1	0	1	D
1	1	1	0	E
1	1	1	1	F

IBM PUNCH CARDS

The hexadecimal equivalent (from Figure 2) may be placed on 80 column IBM punch cards as follows:

Step	Column	
1	12	Byte "0" Hexadecimal equivalent for outputs D7 thru D4 (D7 = M.S.B.)
2	13	Byte "0" Hexadecimal equivalent for outputs D3 thru D0 (D3 = M.S.B.)
3	14-75	Alternate steps 1 and 2 for consecutive bytes.
4	77-80	Card number (starting 0001)

FIGURE 3 — HAND-PUNCHED PAPER TAPE FORMAT

Frames	
Leader	Blank Tape
1 to M	Allowed for customer use ($M \leqslant 64$)
$M + 1$, $M + 2$	CR; LF (Carriage Return; Line Feed)
$M + 3$ to $M + 66$	First line of pattern information (64 hex figures per line)
$M + 67$, $M + 68$	CR; LF
$M + 69$ to $M + 2112$	Remaining 31 lines of hex figures, each line followed by a Carriage Return and Line Feed
Blank Tape	

Frames 1 to M are left to the customer for internal identification, where $M \leqslant 64$. Any combination of alphanumerics may be used. This information is terminated with a Carriage Return and Line Feed, delineating the start of data entry. (Note that the tape cannot begin with a CR and/or LF, or the customer identification will be assumed to be programming data.)

Option A (1024 x 8)

Frame $M + 3$ contains the hexadecimal equivalent of bits D7 thru D4 of byte 0. Frame $M + 4$ contains bits D3 thru D0. These two hex figures together program byte 0. Likewise, frames $M + 5$ and $M + 6$ program byte 1, while $M + 7$ and $M + 8$ program byte 2. Frames $M + 3$ to $M + 66$ comprise the first line of the printout and program, in sequence, the first 32 bytes of storage. The line is terminated with a CR and LF.

Option B (2048 x 4)

Frame $M + 3$ contains the hexadecimal equivalent of byte 0, bits D3 thru D0. Frame $M + 4$ contains byte 1, frame $M + 5$ byte 2, and so on. Frames $M + 3$ to $M + 66$ sequentially program bytes 0 to 31 (the first 32 bytes). The line is terminated with a CR and LF.

Both Options

The remaining 31 lines of data are punched in sequence using the same format, each line terminated with a CR and LF. The total 32 lines of data contain 32 x 64 or 2048 characters. Since each character programs 4 bits of information, a full 8192 bits are programmed.

As an example, a printout of the punched tape for Figure 13 would read as shown in Figure 10 (a CR and LF is implicit at the end of each line).

FIGURE 4 — FORMAT FOR PROGRAMMING GENERAL OPTIONS

ORGANIZATIONAL DATA
MCM68A30A/68B30A MOS READ ONLY MEMORY

Customer:

Company ______________________________

Part No. ______________________________

Originator ______________________________

Phone No. ______________________________

Motorola Use Only:

Quote: ______________________

Part No.: ______________________

Specif. No.: ______________________

Chip Select Options:

	Active High	Active Low	No Connect "Don't Care"
CS1	☐	☐	☐
CS2	☐	☐	☐
CS3	☐	☐	☐
CS4	☐	☐	☐

MOTOROLA

MCM68A308
MCM68B308

MOS

(N-CHANNEL, SILICON-GATE)

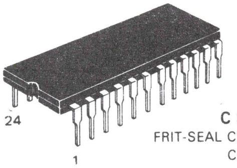
1024 X 8-BIT
READ ONLY MEMORY

1024 X 8-BIT READ ONLY MEMORY

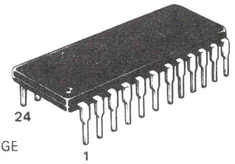
The MCM68A308/MCM68B308 is a mask-programmable byte-organized memory designed for use in bus-organized systems. It is fabricated with N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, has compatibility with TTL and DTL, and needs no clocks or refreshing because of static operation.

The memory is compatible with the M6800 Microcomputer Family, providing read only storage in byte increments. Memory expansion is provided through multiple Chip Select inputs. The active level of the Chip Select inputs and the memory content are defined by the customer.

- Organized as 1024 Bytes of 8 Bits
- Static Operation
- Three-State Data Output
- Mask-Programmable Chip Selects for Simplified Memory Expansion
- Single ±10% 5-Volt Power Supply
- TTL Compatible
- Maximum Access Time = 350 ns – MCM68A308
  250 ns – MCM68B308
- 350 mW Typical Power Dissipation

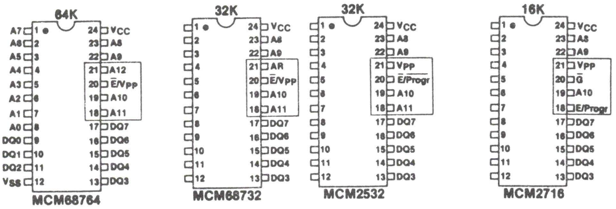


C SUFFIX
FRIT-SEAL CERAMIC PACKAGE
CASE 623

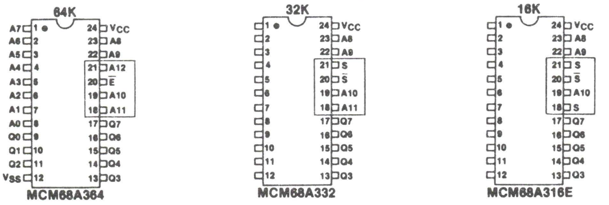


P SUFFIX
PLASTIC PACKAGE
CASE 709

MOTOROLA'S PIN-COMPATIBLE EPROM FAMILY

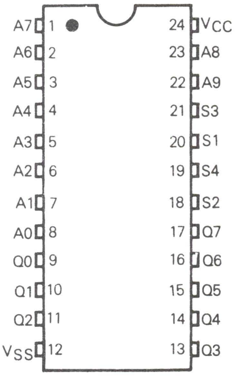

64K
A7 1 24 VCC
A6 2 23 A8
A5 3 22 A9
A4 4 21 A12
A3 5 20 E/Vpp
A2 6 19 A10
A1 7 18 A11
A0 8 17 DQ7
DQ0 9 16 DQ6
DQ1 10 15 DQ5
DQ2 11 14 DQ4
VSS 12 13 DQ3
MCM68764
32K
24 VCC
23 A8
22 A9
21 AR
20 E/Vpp
19 A10
18 A11
17 DQ7
16 DQ6
15 DQ5
14 DQ4
13 DQ3
MCM68732
32K
24 VCC
23 A8
22 A9
21 Vpp
20 E/Progr
19 A10
18 A11
17 DQ7
16 DQ6
15 DQ5
14 DQ4
13 DQ3
MCM2532
16K
24 VCC
23 A8
22 A9
21 Vpp
20 G
19 A10
18 E/Progr
17 DQ7
16 DQ6
15 DQ5
14 DQ4
13 DQ3
MCM2716

MOTOROLA'S PIN-COMPATIBLE ROM FAMILY


64K
A7 1 24 VCC
A6 2 23 A8
A5 3 22 A9
A4 4 21 A12
A3 5 20 E
A2 6 19 A10
A1 7 18 A11
A0 8 17 Q7
Q0 9 16 Q6
Q1 10 15 Q5
Q2 11 14 Q4
VSS 12 13 Q3
MCM68A364
32K
24 VCC
23 A8
22 A9
21 S
20 S
19 A10
18 A11
17 Q7
16 Q6
15 Q5
14 Q4
13 Q3
MCM68A332
16K
24 VCC
23 A8
22 A9
21 S
20 S
19 A10
18 S
17 Q7
16 Q6
15 Q5
14 Q4
13 Q3
MCM68A316E

INDUSTRY STANDARD PINOUTS

PIN ASSIGNMENT


A7 1 24 VCC
A6 2 23 A8
A5 3 22 A9
A4 4 21 S3
A3 5 20 S1
A2 6 19 S4
A1 7 18 S2
A0 8 17 Q7
Q0 9 16 Q6
Q1 10 15 Q5
Q2 11 14 Q4
VSS 12 13 Q3

PIN NAMES	
A0–A9	Address Inputs
S1–S4	Chip Selects
Q0–Q7	Data Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	Vdc
Input High Voltage	V_{IH}	2.0	–	5.5	Vdc
Input Low Voltage	V_{IL}	−0.3	–	0.8	Vdc

DC CHARACTERISTICS

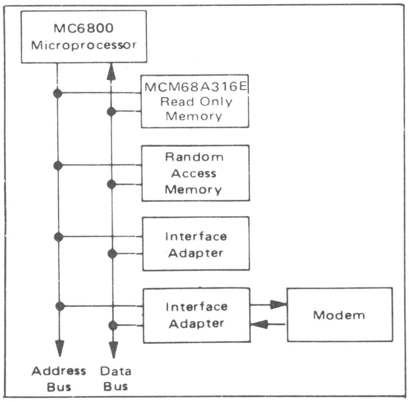
Characteristic	Symbol	Min	Max	Unit
Input Current (V_{in} = 0 to 5.5 V)	I_{in}	–	2.5	μAdc
Output High Voltage (I_{OH} = −205 μA)	V_{OH}	2.4	–	Vdc
Output Low Voltage (I_{OL} = 1.6 mA)	V_{OL}	–	0.4	Vdc
Output Leakage Current (Three-State) (S = 0.8 V or $\overline{S}$ = 2.0 V, V_{out} = 0.4 V to 2.4 V)	I_{LO}	–	10	μAdc
Supply Current (V_{CC} = 5.5 V, T_A = 0°C)	I_{CC}	–	130	mAdc

ABSOLUTE MAXIMUM RATINGS (See Note 1)

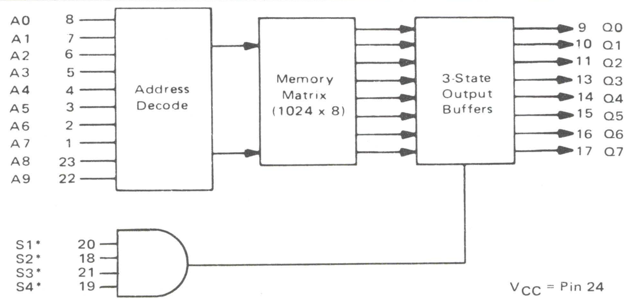
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{in}	−0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

M6800 MICROCOMPUTER FAMILY BLOCK DIAGRAM


MC6800 Microprocessor
MCM68A316E Read Only Memory
Random Access Memory
Interface Adapter
Interface Adapter
Modem
Address Bus
Data Bus

BLOCK DIAGRAM


A0 8
A1 7
A2 6
A3 5
A4 4
A5 3
A6 2
A7 1
A8 23
A9 22
Address Decode
Memory Matrix (1024 x 8)
3-State Output Buffers
9 Q0
10 Q1
11 Q2
13 Q3
14 Q4
15 Q5
16 Q6
17 Q7
S1* 20
S2* 18
S3* 21
S4* 19
V_{CC} = Pin 24
V_{SS} = Pin 12

* Active level defined by the user.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted.
All timing with $t_r = t_f = 20$ ns, Load of Figure 1)

Characteristic	Symbol	MCM68A308		MCM68B308		Unit
		Min	Max	Min	Max	
Cycle Time	t_{cyc}	350	–	250	–	ns
Access Time	t_{acc}	–	350	–	250	ns
Chip Select to Output Delay	t_{SO}	–	150	–	150	ns
Data Hold from Address	t_{DHA}	10	–	10	–	ns
Data Hold from Deselection	t_{DHD}	10	150	10	150	ns

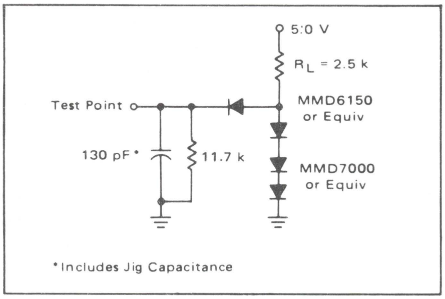
CAPACITANCE

(f = 2.0 MHz, $T_A = 25^{\circ}$C, periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Input Capacitance	C_{in}	7.5	pF
Output Capacitance	C_{out}	12.5	pF

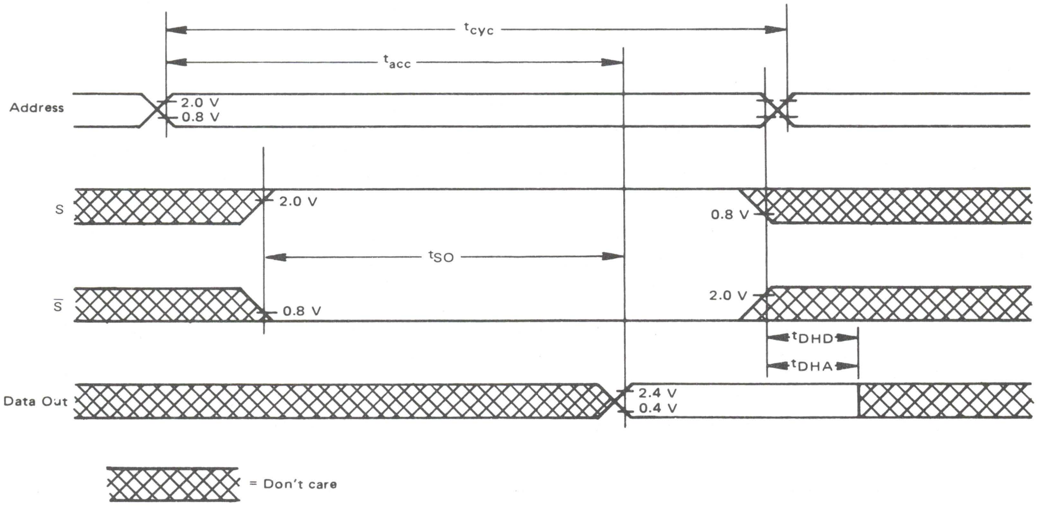
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

FIGURE 1 – AC TEST LOAD


5.0 V
R_L = 2.5 k
Test Point
MMD6150
or Equiv
130 pF*
11.7 k
MMD7000
or Equiv

*Includes Jig Capacitance

TIMING DIAGRAM


t_{cyc}
t_{acc}
Address
2.0 V
0.8 V
S
2.0 V
0.8 V
t_{SO}
$\overline{S}$
0.8 V
2.0 V
t_{DHD}
t_{DHA}
Data Out
2.4 V
0.4 V
= Don't care

CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM68A308/MCM68B308, the customer may specify the content of the memory and the method of enabling the outputs. (A "no-connect" must always be the highest order chip-select(s).)

Information on the general options of the MCM68A308/MCM68B308 should be submitted on an Organizational Data form such as that shown in Figure 4.

Information for customer memory content may be sent to Motorola in one of four forms (shown in order of preference):

1. Paper tape output of the Motorola M6800 Software.
2. Hexadecimal coding using IBM Punch Cards.
3. EPROM one MCM68A708 or equivalent.
4. Hand punched paper tape (Figure 3).

PAPER TAPE

Included in the software packages developed for the M6800 Microcomputer Family is the ability to produce a paper tape output for computerized mask generation. The assembler directives are used to control allocation of memory, to assign values for stored data, and for controlling the assembly process. The paper tape must specify the full 1024 bytes.

FIGURE 2 – BINARY TO HEXADECIMAL CONVERSION

Binary Data				Hexadecimal Character
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	A
1	0	1	1	B
1	1	0	0	C
1	1	0	1	D
1	1	1	0	E
1	1	1	1	F

IBM PUNCH CARDS

The hexadecimal equivalent (from Figure 2) may be placed on 80 column IBM punch cards as follows:

Step	Column	
1	12	Byte "0" Hexadecimal equivalent for outputs Q7 thru Q4 (Q7 = M.S.B.)
2	13	Byte "0" Hexadecimal equivalent for outputs Q3 thru Q0 (Q3 = M.S.B.)
3	14–75	Alternate steps 1 and 2 for consecutive bytes.
4	77–80	Card number (starting 0001)

FIGURE 3 – HAND-PUNCHED PAPER TAPE FORMAT

Frames	
Leader	Blank Tape
1 to M	Allowed for customer use (M ⩽ 64)
M + 1, M + 2	CR; LF (Carriage Return; Line Feed)
M + 3 to M + 66	First line of pattern information (64 hex figures per line)
M + 67, M + 68	CR; LF
M + 69 to M + 2112	Remaining 31 lines of hex figures, each line followed by a Carriage Return and Line Feed
Blank Tape	

Frames 1 to M are left to the customer for internal identification, where M ⩽ 64. Any combination of alphanumerics may be used. This information is terminated with a Carriage Return and Line Feed, delineating the start of data entry. (Note that the tape cannot begin with a CR and/or LF, or the customer identification will be assumed to be programming data.)

Frame M + 3 contains the hexadecimal equivalent of bits Q7 thru Q4 of byte 0. Frame M + 4 contains bits Q3 thru Q0. These two hex figures together program byte 0. Likewise, frames M + 5 and M + 6 program byte 1, while M + 7 and M + 8 program byte 2. Frames M + 3 to M + 66 comprise the first line of the printout and program, in sequence, the first 32 bytes of storage. The line is terminated with a CR and LF.

The remaining 31 lines of data are punched in sequence using the same format, each line terminated with a CR and LF. The total 32 lines of data contain 32 x 64 or 2048 characters. Since each character programs 4 bits of information, a full 8192 bits are programmed.

FIGURE 4 — FORMAT FOR PROGRAMMING GENERAL OPTIONS

ORGANIZATIONAL DATA
MCM68308 MOS READ ONLY MEMORY

Customer:

Company ____________________

Part No. ____________________

Originator ____________________

Phone No. ____________________

Motorola Use Only:

Quote: ____________________

Part No.: ____________________

Specif. No.: ____________________

Chip Select:

	Active High	Active Low	No Connect
S1	☐	☐	☐
S2	☐	☐	☐
S3	☐	☐	☐
S4	☐	☐	☐

MOTOROLA

MCM68A316E

MOS

(N-CHANNEL, SILICON-GATE)

2048 × 8 BIT
READ ONLY MEMORY

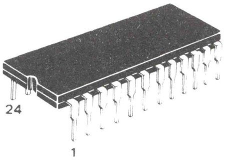
2048 × 8 BIT READ ONLY MEMORY

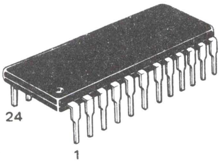
The MCM68A316E is a mask-programmable byte-organized memory designed for use in bus-organized systems. It is fabricated with N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, has compatibility with TTL and DTL, and needs no clocks or refeshing because of static operation.

The memory is compatible with the M6800 Microcomputer Family, providing read only storage in byte increments. Memory expansion is provided through multiple Chip Select inputs. The active level of the Chip Select inputs and the memory content are defined by the user.

- Fully Static Operation
- Three-State Data Output
- Mask-Programmable Chip Selects for Simplified Memory Expansion
- Single ±10% 5-Volt Power Supply
- TTL Compatible
- Maximum Access Time = 350 ns
- Plug-in Compatible with 2316E
- Pin Compatible with 2708 and TMS2716 EPROMs

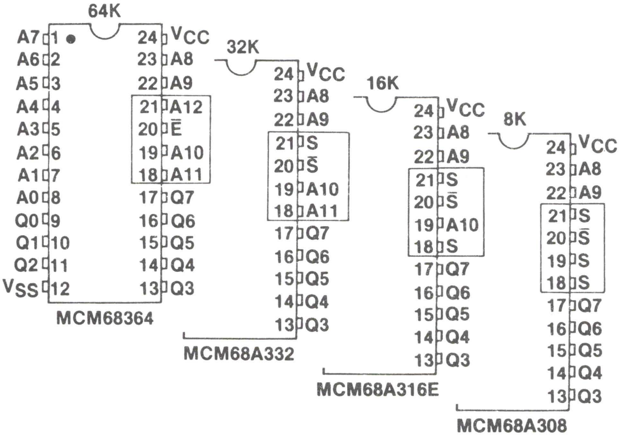
C SUFFIX
FRIT-SEAL CERAMIC PACKAGE
CASE 623





P SUFFIX
PLASTIC PACKAGE
CASE 709

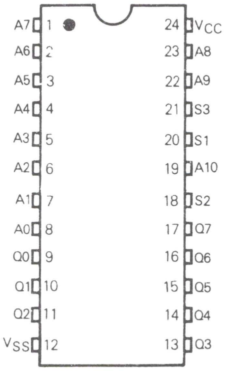
MOTOROLA'S PIN-COMPATIBLE ROM FAMILY



64K
A7 1 24 VCC
A6 2 23 A8
A5 3 22 A9
A4 4 21 A12
A3 5 20 Ē
A2 6 19 A10
A1 7 18 A11
A0 8 17 Q7
Q0 9 16 Q6
Q1 10 15 Q5
Q2 11 14 Q4
VSS 12 13 Q3
MCM68364
32K
24 VCC
23 A8
22 A9
21 S
20 S̄
19 A10
18 A11
17 Q7
16 Q6
15 Q5
14 Q4
13 Q3
MCM68A332
16K
24 VCC
23 A8
22 A9
21 S
20 S̄
19 A10
18 S
17 Q7
16 Q6
15 Q5
14 Q4
13 Q3
MCM68A316E
8K
24 VCC
23 A8
22 A9
21 S
20 S̄
19 S
18 S
17 Q7
16 Q6
15 Q5
14 Q4
13 Q3
MCM68A308
AA89-1

INDUSTRY STANDARD PINOUTS

PIN ASSIGNMENT



A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
Q0 9
Q1 10
Q2 11
VSS 12
24 VCC
23 A8
22 A9
21 S3
20 S1
19 A10
18 S2
17 Q7
16 Q6
15 Q5
14 Q4
13 Q3

PIN NAMES	
A0–A10	Address Inputs
S1–S3	Chip Selects
Q0–Q7	Data Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	Vdc
Input High Voltage	V_{IH}	2.0	–	5.5	Vdc
Input Low Voltage	V_{IL}	-0.3	–	0.8	Vdc

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Input Current (V_{in} = 0 to 5.5 V)	I_{in}	–	2.5	μAdc
Output High Voltage (I_{OH} = -205 μA)	V_{OH}	2.4	–	Vdc
Output Low Voltage (I_{OL} = 1.6 mA)	V_{OL}	–	0.4	Vdc
Output Leakage Current (Three-State) (S = 0.8 V or $\overline{S}$ = 2.0 V, V_{out} = 0.4 V to 2.4 V)	I_{LO}	–	10	μAdc
Supply Current (V_{CC} = 5.5 V, T_A = 0°C)	I_{CC}	–	130	mAdc

ABSOLUTE MAXIMUM RATINGS (See Note 1)

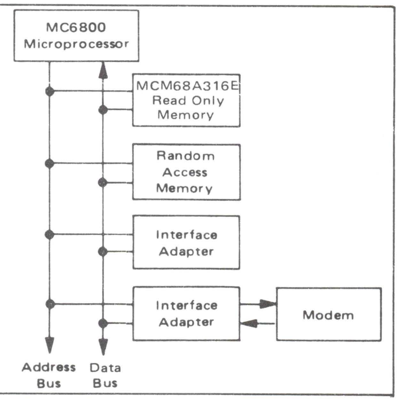
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

CAPACITANCE

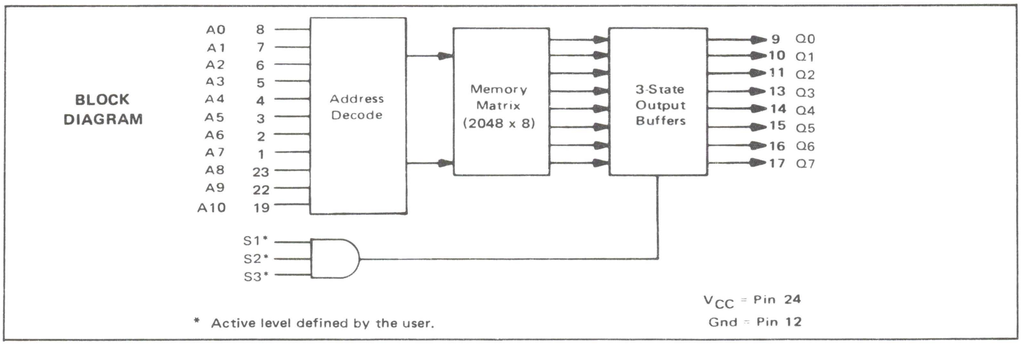
(f = 2.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Input Capacitance	C_{in}	7.5	pF
Output Capacitance	C_{out}	12.5	pF


MC6800
Microprocessor
MCM68A316E
Read Only
Memory
Random
Access
Memory
Interface
Adapter
Interface
Adapter
Modem
Address
Bus
Data
Bus

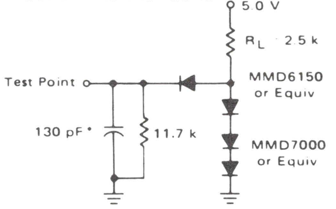
M6800 MICROCOMPUTER FAMILY BLOCK DIAGRAM

BLOCK DIAGRAM


A0 8
A1 7
A2 6
A3 5
A4 4
A5 3
A6 2
A7 1
A8 23
A9 22
A10 19
Address
Decode
Memory
Matrix
(2048 x 8)
3-State
Output
Buffers
9 Q0
10 Q1
11 Q2
13 Q3
14 Q4
15 Q5
16 Q6
17 Q7
S1*
S2*
S3*
VCC = Pin 24
Gnd = Pin 12

* Active level defined by the user.

FIGURE 1—AC TEST LOAD


5.0 V
R_L 2.5 k
Test Point
MMD6150
or Equiv
130 pF*
11.7 k
MMD7000
or Equiv

*Includes Jig Capacitance

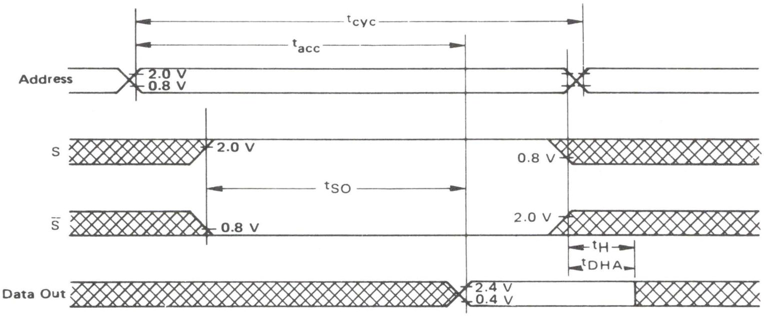
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted.
All timing with $t_r = t_f = 20$ ns, Load of Figure 1)

Characteristic	Symbol	Min	Max	Unit
Cycle Time	t_{cyc}	350	–	ns
Access Time	t_{acc}	–	350	ns
Chip Select to Output Delay	t_{SO}	–	150	ns
Data Hold from Address	t_{DHA}	10	–	ns
Data Hold from Deselection	t_H	10	150	ns

TIMING DIAGRAM


t_{cyc}
t_{acc}
Address
2.0 V
0.8 V
S
2.0 V
0.8 V
t_{SO}
$\bar{S}$
0.8 V
2.0 V
t_H
t_{DHA}
Data Out
2.4 V
0.4 V

CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM68A316E, the customer may specify the content of the memory and the method of enabling the outputs.

Information on the general options of the MCM68A316E should be submitted on an Organizational Data form such as that shown in Figure 3. ("No-Connect" must always be the highest order Chip Select(s).)

Information for custom memory content may be sent to Motorola in one of three forms (shown in order of preference):

1. Paper tape output of the Motorola M6800 Software.
2. Hexadecimal coding using IBM Punch Cards.
3. EPROM (TMS2716 or MCM2716).

PAPER TAPE

Included in the software packages developed for the M6800 Microcomputer Family is the ability to produce a paper tape output for computerized mask generation. The assembler directives are used to control allocation of memory, to assign values for stored data, and for controlling the assembly process. The paper tape must specify the full 2048 bytes.

FIGURE 2 – BINARY TO HEXADECIMAL CONVERSION

Binary Data				Hexadecimal Character
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	A
1	0	1	1	B
1	1	0	0	C
1	1	0	1	D
1	1	1	0	E
1	1	1	1	F

IBM PUNCH CARDS

The hexadecimal equivalent (from Figure 2) may be placed on 80 column IBM punch cards as follows:

Step	Column	
1	12	Byte "0" Hexadecimal equivalent for outputs Q7 thru Q4 (Q7 = M.S.B.)
2	13	Byte "0" Hexadecimal equivalent for outputs Q3 thru Q0 (Q3 = M.S.B.)
3	14–75	Alternate steps 1 and 2 for consecutive bytes.
4	77–80	Card number (starting 0001) Total number of cards (64)

FIGURE 3 – FORMAT FOR PROGRAMMING GENERAL OPTIONS

ORGANIZATIONAL DATA
MCM68A316E MOS READ ONLY MEMORY

Customer:

Company ________________________

Part No. ________________________

Originator ________________________

Phone No. ________________________

Motorola Use Only:

Quote: ____________________

Part No.: ____________________

Specif. No.: ____________________

Chip Select:

	Active High	Active Low	No Connect
S1	☐	☐	☐
S2	☐	☐	☐
S3	☐	☐	☐

MOTOROLA

MCM65516

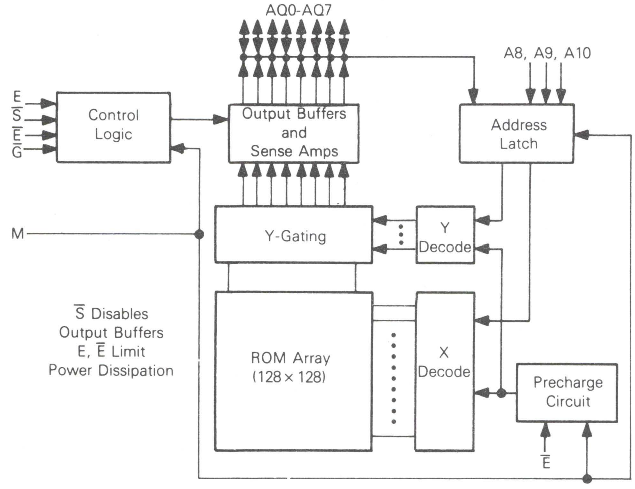
2048 × 8 BIT READ ONLY MEMORY

The MCM65516 is a complementary MOS mask programmable byte organized read only memory (ROM). The MCM65516 is organized as 2048 bytes of 8 bits, designed for use in multiplex bus systems. It is fabricated using Motorola's high performance silicon gate CMOS technology, which offers low-power operation from a single 5.0 volt supply.

The memory is compatible with CMOS microprocessors that share address and data lines. Compatibility is enhanced by pins 13, 14, 16, and 17 which give the user the versatility of selecting the active levels of each. Pin 17 allows the user to choose active high, active low, or a third option of programming which is termed the "MOTEL" mode. If this mode is selected by the user, it provides direct compatibility with either the Motorola MC146805E2 or Intel 8085 type microprocessor series. In the MOTEL operation the ROM can accept either polarity signal on the data strobe input as long as the signal toggles during the cycle. This unique operational feature makes the ROM an extremely versatile device.

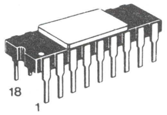
- 2K × 8 CMOS ROM
- 3 to 6 Volt Supply
- Access Time
  - 430 ns (5 V) MCM65516-43
  - 550 ns (5 V) MCM65516-55
- Low Power Dissipation
  - 15 mA Maximum (Active)
  - 30 µA Maximum (Standby)
- Multiplex Bus Directly Compatible With CMOS Microprocessors (MC146805E2, NSC800)
- Pins 13, 14, 16, and 17 are Mask Programmable
- MOTEL Mask Option Also Insures Direct Compatibility with NMOS Microprocessors Like MC6803, MC6801, 8085, and 8086
- Standard 18 Pin Package

BLOCK DIAGRAM

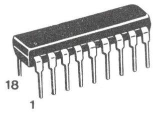

AQ0-AQ7
A8, A9, A10
E
S̄
Ē
G
Control Logic
Output Buffers and Sense Amps
Address Latch
M
Y-Gating
Y Decode
ROM Array (128 × 128)
X Decode
Precharge Circuit
Ē
S̄ Disables Output Buffers
E, Ē Limit Power Dissipation

CMOS
(COMPLEMENTARY MOS)

2048 × 8 BIT MULTIPLEXED BUS READ ONLY MEMORY

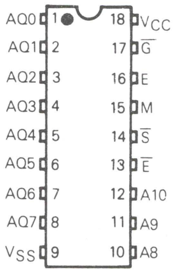


L SUFFIX
CERAMIC PACKAGE
CASE 680



P SUFFIX
PLASTIC PACKAGE
CASE 707

PIN ASSIGNMENTS


AQ0 1
AQ1 2
AQ2 3
AQ3 4
AQ4 5
AQ5 6
AQ6 7
AQ7 8
VSS 9
18 VCC
17 Ḡ
16 E
15 M
14 S̄
13 Ē
12 A10
11 A9
10 A8

PIN NAMES	
AQ0-AQ7	Address/Data Output
A8-A10	Address
M	Multiplex Address Strobe
E	Chip Enable
S	Chip Select
G	Data Strobe (Output Enable)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage (V_{CC} must be applied at least 100 μs before proper device operation is achieved)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	$V_{CC}-2.0$	–	V_{CC}	V
Input Low Voltage	V_{IL}	−0.3	–	0.8	V

RECOMMENDED OPERATING CHARACTERISTICS

Characteristic	Symbol	MCM65516-43		MCM65516-55		Unit	Test Condition
		Min	Max	Min	Max		
Output High Voltage Source Current −1.6 mA	V_{OH}	$V_{CC}-0.4$ V	–	$V_{CC}-0.4$ V	–	V	
Output Low Voltage Sink Current +1.6 mA	V_{OL}	–	0.4	–	0.4	V	
Supply Current (Operating)	I_{CC1}	–	15	–	15	mA	$C_L = 130$ pF, $V_{in} = V_{IH}$ to V_{IL} $t_{cyc} = 1.0$ μs
Supply Current (DC Active)	I_{CC2}	–	100	–	100	μA	$V_{in} = V_{CC}$ to GND
Standby Current	I_{SB}	–	30	–	50	μA	$V_{in} = V_{CC}$ to GND
Input Leakage	I_{in}	−10	+10	−10	+10	μA	
Output Leakage	I_{OL}	−10	+10	−10	+10	μA	

CAPACITANCE (f = 1.0 MHz, $T_A = 25°C$, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Max	Unit
Input Capacitance	C_{in}	5	pF
Output Capacitance	C_{out}	12.5	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

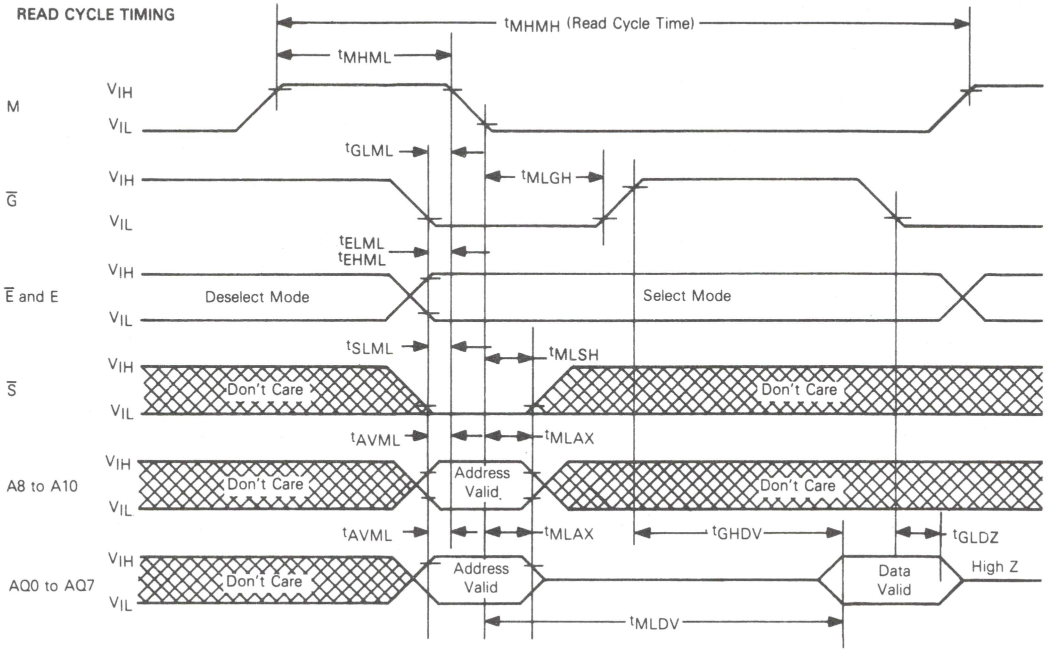
READ CYCLE

$C_L = 130$ pF

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MCM65516-43		MCM65516-55		Unit
		Min	Max	Min	Max	
Address Strobe Access Time	t_{MLDV}	–	430	–	550	ns
Read Cycle Time	t_{MHMH}	–	750	–	1000	ns
Multiplex Address Strobe High to Multiplex Address Strobe Low (Pulse Width)	t_{MHML}	150	–	175	–	ns
Data Strobe Low to Multiplex Address Strobe Low	t_{GLML}	50	–	50	–	ns
Multiplex Address Strobe Low to Data Strobe High	t_{MLGH}	100	–	160	–	ns
Address Valid to Multiplex Address Strobe Low	t_{AVML}	50	–	50	–	ns
Chip Select Low to Multiplex Address Strobe Low	t_{SLML}	50	–	50	–	ns
Multiplex Address Strobe Low to Chip Select High	t_{MLSH}	50	–	80	–	ns
Chip Enable Low/High to Multiplex Address Strobe Low	t_{ELML} t_{EHMH}	50 50	– –	50 50	– –	ns
Multiplex Address Strobe Low to Address Don't Care	t_{MLAX}	50	–	80	–	ns
Data Strobe High to Data Valid	t_{GHDV}	175	–	200	–	ns
Data Strobe Low to High Z	t_{GLDZ}	–	160	–	160	ns

READ CYCLE TIMING



FUNCTIONAL DESCRIPTION

The 2K × 8 bit CMOS ROM (MCM65516) shares address and data lines and, therefore, is compatible with the majority of CMOS microprocessors in the industry. The package size is reduced from 24 pins for standard NMOS ROMs to 18 pins due to the multiplexed bus approach. The savings in package size and external bus lines adds up to tighter board packing density which is handy for battery powered hand carried CMOS systems. This ROM is designed with the intention of having very low active as well as standby currents. The active power dissipation of 150 mW (at $V_{CC}=5$ V freq = 1 MHz) and standby power of 250 µW (at $V_{CC}=5$ V) add up to low power for battery operation. The typical access time of the ROM is 280 ns making it acceptable for operation with today's existing CMOS microprocessors.

An example of this operation is shown in Figure 1. Shown is a typical connection with either the Motorola MC146805E2 CMOS microprocessor (M6800 series) or the National NSC800 which is an 8085 or Z80 based system. The main difference between the systems is that the data strobe (DS) on the MC146805E2 and the read bar ($\overline{RD}$) on the 8085 both control the output of data from the ROM but are of opposite polarity. The Motorola 2K × 8 ROM can accept either polarity signal on the data strobe input as long as the signal toggles during the cycle. This is termed the MOTEL mode of operation. This unique operational feature makes the ROM an extremely versatile part. Further operational features are explained in the following section.

Operational Features

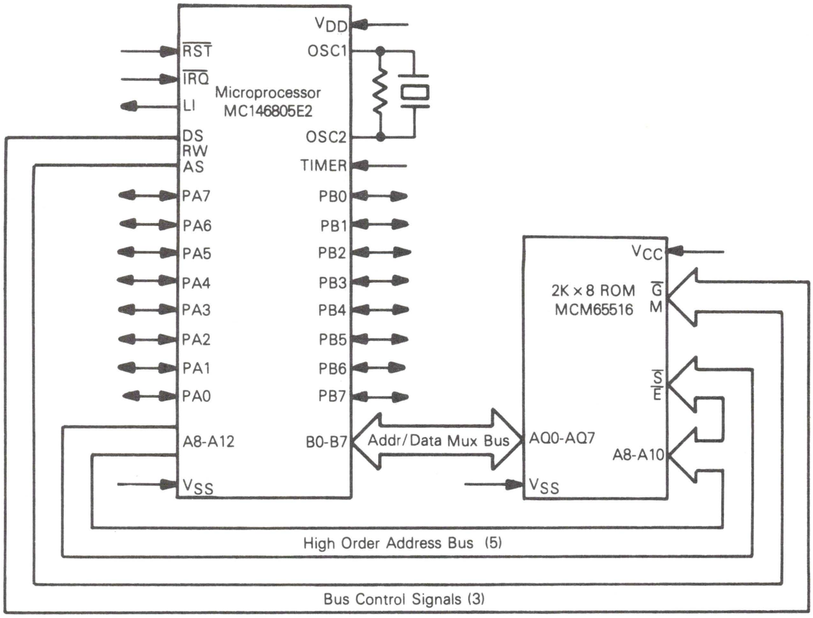
In order to operate in a multiplexed bus sytem the ROM latches, for one cycle, the address and chip select input information on the trailing edge of address strobe (M) so the address signals can be taken off the bus.

Since they are latched, the address and chip select signals have a setup and hold time referenced to the negative edge of address strobe. Address strobe has a minimum pulse width requirement since the circuit is internally precharged during this time and is setup for the next cycle on the trailing edge of address strobe. Access time is measured from the negative edge of address strobe.

The part is equipped with a data strobe input (G) which controls the output of data onto the bus lines after the addresses are off the bus. The data strobe has three potential modes of operation which are programmable with the ROM array. The first mode is termed the MOTEL mode of operation. In this mode, the circuit can work with either the Motorola or Intel type microprocessor series. The difference between the two series for a ROM peripheral is only the polarity of the data strobe signal. Therefore, in the MOTEL mode the ROM recognizes the state of the data strobe signal at the trailing edge of address strobe (requires a setup and hold time), latches the state into the circuit after address strobe, and turns on the data outputs when an opposite polarity signal appears on the data strobe input. In this manner the data strobe input can work with either polarity signal but that signal must toggle during a cycle to output data on the bus lines. If the data strobe remains at a d.c. level the outputs will remain off. The data strobe input has two other programmable modes of operation and those are the standard static select modes (high or low) where a d.c. input not synchronous with the address strobe will turn the outputs on or off.

The chip enable and chip select inputs are all programmable with the ROM array to either a high or low select. The chip select acts as an additional address and is latched on the address strobe trailing edge. On deselect the chip select merely turns off the output drivers acting as an output disable. It does not power down the chip. The chip enable inputs, however, do put the chip in a power down standby mode but they are not latched with address strobe and must be maintained in a d.c. state for a full cycle.

FIGURE 1
TYPICAL MINIMUM SYSTEM — MOTOROLA


V_{DD}
RST
IRQ
LI
DS
RW
AS
OSC1
OSC2
TIMER
Microprocessor
MC146805E2
PA7
PA6
PA5
PA4
PA3
PA2
PA1
PA0
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
A8-A12
B0-B7
V_{SS}
Addr/Data Mux Bus
V_{CC}
2K × 8 ROM
MCM65516
G
M
S
E
AQ0-AQ7
A8-A10
V_{SS}
High Order Address Bus (5)
Bus Control Signals (3)

INTRODUCTION

CBUG05 is a debug monitor program written for the MC146805E2 Microprocessor Unit and contained in the MCM65516 2K × 8 CMOS ROM. CBUG05 allows for rapid development and evaluation of hardware and M6805 Family type software, using memory and register examine/change commands as well as breakpoint and single instruction trace commands. CBUG05 also includes software to set and display time, using an optional MC146818 Real-Time Clock (RTC), and routines to punch and load an optional cassette interface. Figure 2 shows a minimum system which only requires the MPU, ROM, keypad inputs and display output interfaces. Port A of the MC146805E2 MPU is required for the I/O; however, Port B and all other MC146805E2 MPU features remain available to the user. A possible expanded system is shown in Figure 3. If additional information is required, please refer to Application Note AN-823 — "CBUG05 Debug Monitor Program for MC146805E2 Microprocessor Unit."

FIGURE 2 — MINIMUM CBUG05 SYSTEM

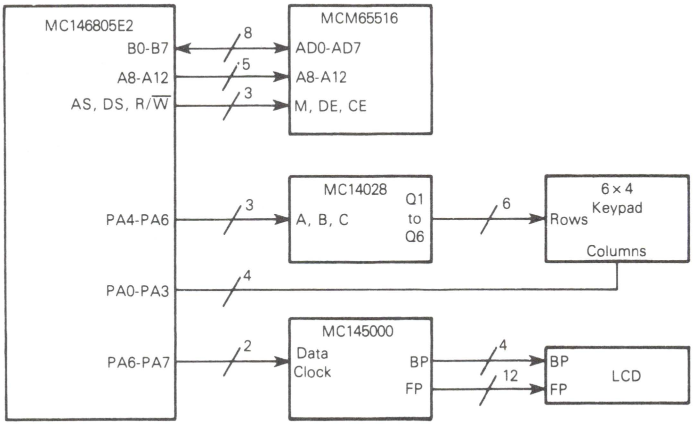
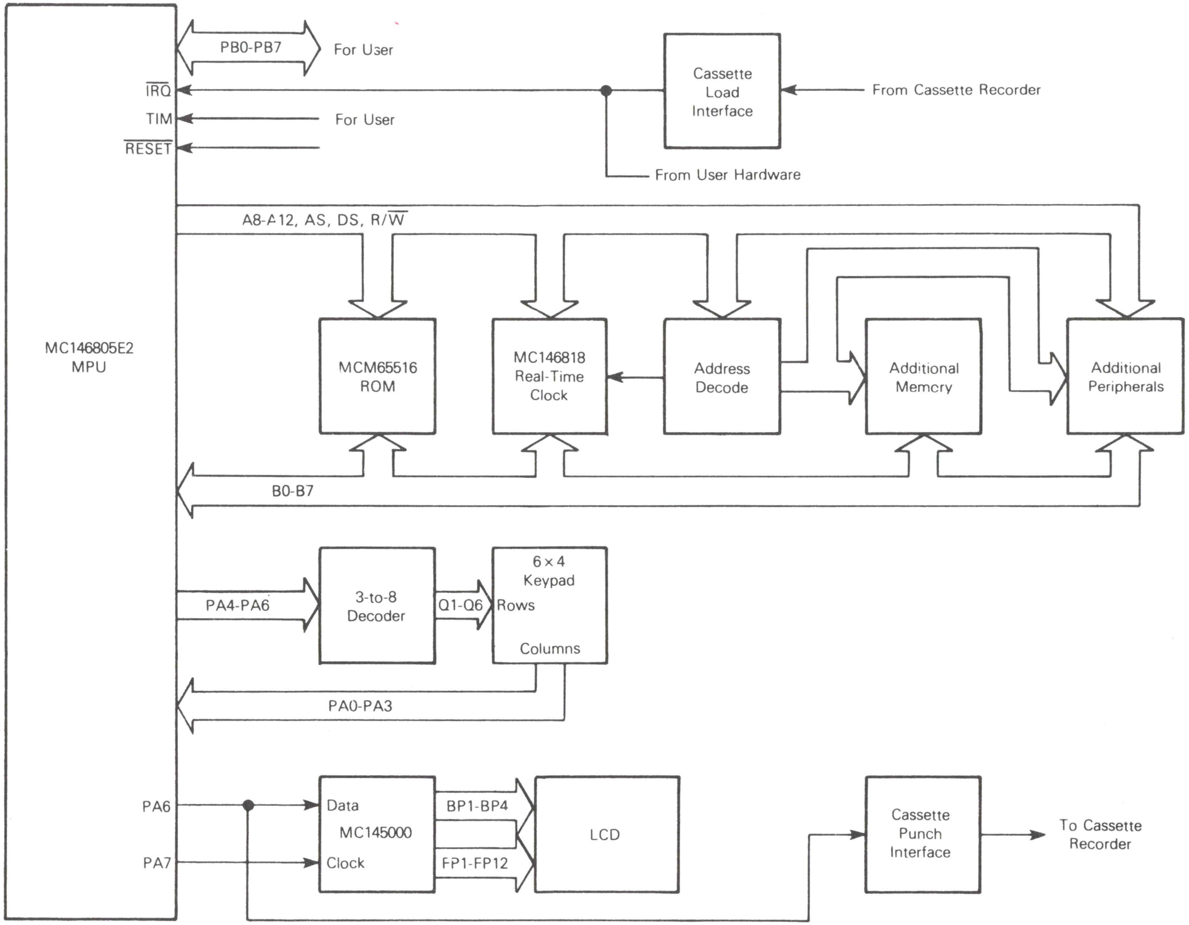

MC146805E2
B0-B7
A8-A12
AS, DS, R/W
PA4-PA6
PA0-PA3
PA6-PA7
8
5
3
3
4
2
MCM65516
AD0-AD7
A8-A12
M, DE, CE
MC14028
A, B, C
Q1
to
Q6
6
6 × 4
Keypad
Rows
Columns
MC145000
Data
Clock
BP
FP
4
12
BP
FP
LCD

FIGURE 3 — EXPANDED CBUG05 SYSTEM


PB0-PB7
For User
IRQ
TIM
For User
RESET
Cassette Load Interface
From Cassette Recorder
From User Hardware
A8-A12, AS, DS, R/W
MC146805E2 MPU
MCM65516 ROM
MC146818 Real-Time Clock
Address Decode
Additional Memory
Additional Peripherals
B0-B7
PA4-PA6
3-to-8 Decoder
Q1-Q6
6×4 Keypad
Rows
Columns
PA0-PA3
PA6
PA7
Data
MC145000
Clock
BP1-BP4
FP1-FP12
LCD
Cassette Punch Interface
To Cassette Recorder

CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM65516 the customer may specify the content of the memory and the method of enabling the outputs, or selection of the "MOTEL" option (Pin 17).

Information on the general options of the MCM65516 should be submitted on an Organizational Data form such as that shown in the below figure.

Information for custom memory content may be sent to Motorola in one of two forms (shown in order of preference):

1. Magnetic Tape
   9 track, 800 bpi, odd parity written in EBCDIC character code. Motorola's R.O.M.S. format.
2. EPROMs
   One 16K (MCM2716, or TMS2716).

FORMAT FOR PROGRAMMING GENERAL OPTIONS

ORGANIZATIONAL DATA MOS READ ONLY MEMORY

Customer:

Company ____________________

Part No. ____________________

Originator ____________________

Phone No. ____________________

Motorola Use Only

Quote: ____________________

Part No.: ____________________

Specif. No.: ____________________

Programmable Pin Options:

	13	14	16	17
Active High	☐	☐	☐	☐
Active Low	☐	☐	☐	☐
			MOTEL	☐

MOTOROLA

MCM68A332

4096 X 8-BIT READ ONLY MEMORY

The MCM68A332 is a mask-programmable byte-organized memory designed for use in bus-organized systems. It is fabricated with N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, has compatibility with TTL and DTL, and needs no clocks or refreshing because of static operation.

The memory is compatible with the M6800 Microcomputer Family, providing read only storage in byte increments. Memory expansion is provided through multiple Chip Select inputs. The active level of the Chip Select inputs and the memory content are defined by the user.

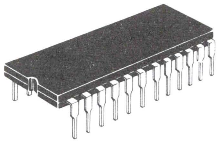
- Fully Static Operation
- Three-State Data Output for OR-Ties
- Mask-Programmable Chip Selects for Simplified Memory Expansion
- Single ±10% 5-Volt Power Supply
- Fully TTL Compatible
- Maximum Access Time = 350 ns
- Directly Compatible with 4732
- Pin Compatible with 2708 and 2716 EPROMs
- Preprogrammed MCM68A332-2 Available

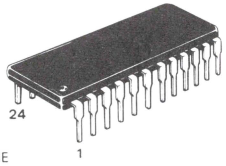
MOS

(N-CHANNEL, SILICON-GATE)

4096 X 8-BIT
READ ONLY MEMORY

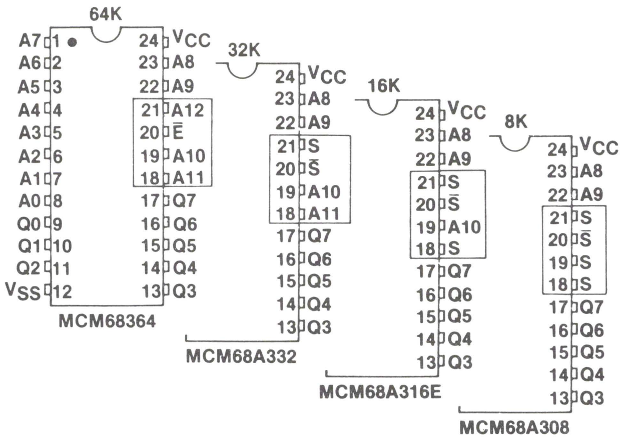
C SUFFIX
FRIT-SEAL CERAMIC PACKAGE
CASE 623





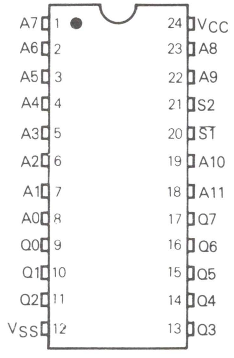
P SUFFIX
PLASTIC PACKAGE
CASE 709

MOTOROLA'S PIN-COMPATIBLE ROM FAMILY


64K
32K
16K
8K
A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
Q0 9
Q1 10
Q2 11
VSS 12
24 VCC
23 A8
22 A9
21 A12
20 Ē
19 A10
18 A11
17 Q7
16 Q6
15 Q5
14 Q4
13 Q3
21 S
20 S̄
19 A10
18 A11
21 S
20 S̄
19 A10
18 S
21 S
20 S̄
19 S
18 S
MCM68364
MCM68A332
MCM68A316E
MCM68A308
AA89-1

INDUSTRY STANDARD PINOUTS

PIN ASSIGNMENT


A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
Q0 9
Q1 10
Q2 11
VSS 12
24 VCC
23 A8
22 A9
21 S2
20 S̄1
19 A10
18 A11
17 Q7
16 Q6
15 Q5
14 Q4
13 Q3

PIN NAMES	
A0–A11	. . . . Address Inputs
S	. . . . Programmable Chip Selects
Q0–Q7	. . . . Data Output
V_{CC}	. . . . +5 V Power Supply
V_{SS}	. . . . Ground

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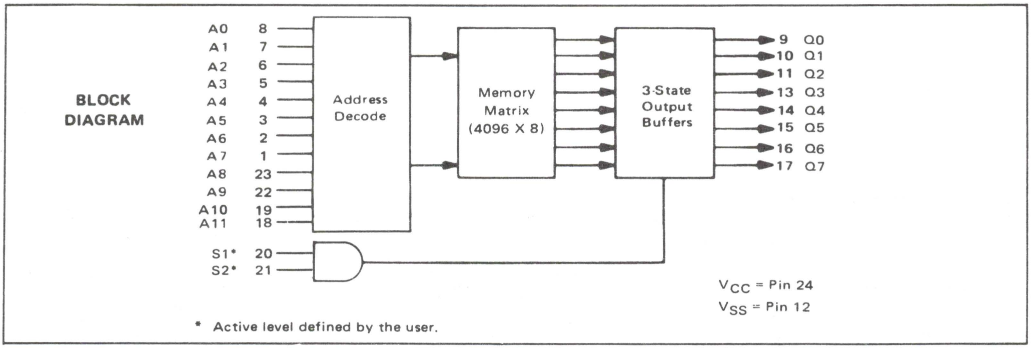
DS 9519
(Replaces ADI-469)

DS9519/7-78



BLOCK DIAGRAM

A0 8
A1 7
A2 6
A3 5
A4 4
A5 3
A6 2
A7 1
A8 23
A9 22
A10 19
A11 18
Address Decode
Memory Matrix (4096 X 8)
3-State Output Buffers
9 Q0
10 Q1
11 Q2
13 Q3
14 Q4
15 Q5
16 Q6
17 Q7
S1* 20
S2* 21
V_{CC} = Pin 24
V_{SS} = Pin 12

* Active level defined by the user.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (V_{CC} must be applied at least 100 μs before proper device operation is achieved.)	V_{CC}	4.5	5.0	5.5	Vdc
Input High Voltage	V_{IH}	2.0	–	5.5	Vdc
Input Low Voltage	V_{IL}	-0.3	–	0.8	Vdc

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Input Current (V_{in} = 0 to 5.5 V)	I_{in}	–	2.5	μAdc
Output High Voltage (I_{OH} = -205 μA)	V_{OH}	2.4	–	Vdc
Output Low Voltage (I_{OL} = 1.6 mA)	V_{OL}	–	0.4	Vdc
Output Leakage Current (Three-State) (S = 0.8 V or $\bar{S}$ = 2.0 V, V_{out} = 0.4 V to 2.4 V)	I_{LO}	–	10	μAdc
Supply Current (V_{CC} = 5.5 V, T_A = 0°C)	I_{CC}	–	80	mAdc

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

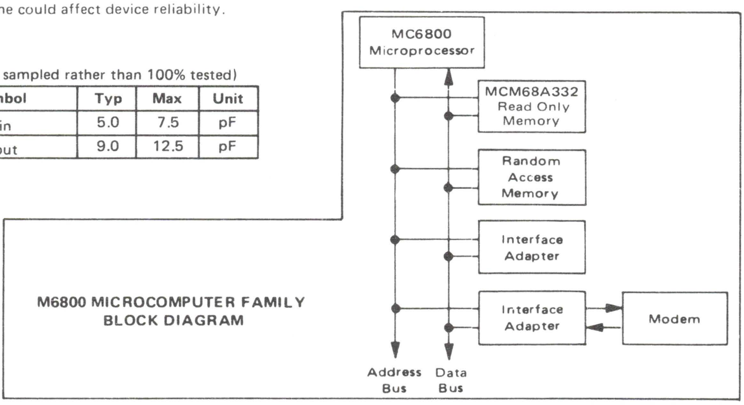
NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

CAPACITANCE

(f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested)

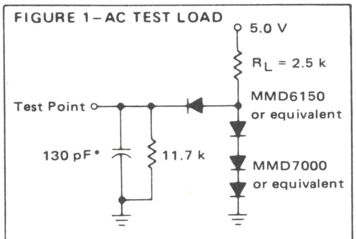
Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	5.0	7.5	pF
Output Capacitance	C_{out}	9.0	12.5	pF



M6800 MICROCOMPUTER FAMILY BLOCK DIAGRAM

MC6800 Microprocessor
MCM68A332 Read Only Memory
Random Access Memory
Interface Adapter
Interface Adapter
Modem
Address Bus
Data Bus

FIGURE 1—AC TEST LOAD


5.0 V
R_L = 2.5 k
MMD6150
or equivalent
Test Point
130 pF*
11.7 k
MMD7000
or equivalent

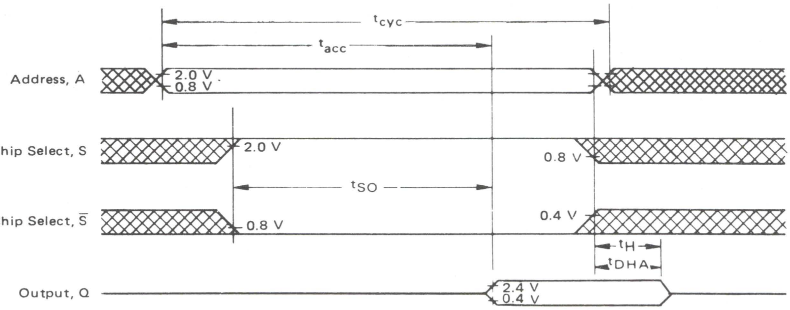
*Includes jig capacitance

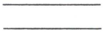
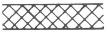
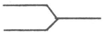
AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted.
All timing with $t_r = t_f = 20$ ns, Load of Figure 1)

Characteristic	Symbol	Min	Max	Unit
Cycle Time	t_{cyc}	350	–	ns
Access Time	t_{acc}	–	350	ns
Chip Select to Output Delay	t_{SO}	–	150	ns
Data Hold from Address	t_{DHA}	10	–	ns
Data Hold from Deselection	t_H	10	150	ns

TIMING DIAGRAM


t_{cyc}
t_{acc}
Address, A
2.0 V
0.8 V
Chip Select, S
2.0 V
0.8 V
t_{SO}
Chip Select, $\overline{S}$
0.8 V
0.4 V
t_H
t_{DHA}
Output, Q
2.4 V
0.4 V

Waveform Symbol	Input	Output	Waveform Symbol	Input	Output	Waveform Symbol	Input	Output
	MUST BE VALID	WILL BE VALID		DON'T CARE ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN		–	HIGH IMPEDANCE

MCM68A332 CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM68A332, the customer may specify the content of the memory and the method of enabling the outputs.

Information on the general options of the MCM68A332 should be submitted on an Organizational Data form such as that shown in Figure 3. (A "No-Connect" or "Don't Care" must always be the highest order Chip Select(s).)

Information for custom memory content may be sent to Motorola in one of four forms (shown in order of preference):

1. IBM Punch Cards:
   - A. Hexadecimal Format
   - B. Intel Format
   - C. Binary Negative-Postive Format
2. EPROMs—two 16K (MCM2716 or TMS2716) or four 8K (MCM2708)
3. Paper tape output of the Motorola M6800 software
4. Hand punched paper tape

PAPER TAPE

Included in the software packages developed for the M6800 Microcomputer Family is the ability to produce a paper tape output for computerized mask generation. The assembler directives are used to control allocation of memory, to assign values for stored data, and for controlling the assembly process. The paper tape must specify the full 4096 bytes.

IBM PUNCH CARDS, HEXADECIMAL FORMAT

The hexadecimal equivalent (from Figure 2) may be placed on 80 column IBM punch cards as follows:

Step	Column	
1	12	Byte "0" Hexadecimal equivalent for outputs Q7 through Q4 (Q7 = M.S.B.)
2	13	Byte "0" Hexadecimal equivalent for outputs Q3 through Q0 (Q3 = M.S.B.)
3	14–75	Alternate steps 1 and 2 for consecutive bytes.
4	77–79	Card number (starting 001).
5		Total number of cards must equal 128.

FIGURE 2 — BINARY TO HEXADECIMAL CONVERSION

Binary Data				Hexadecimal Character
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	A
1	0	1	1	B
1	1	0	0	C
1	1	0	1	D
1	1	1	0	E
1	1	1	1	F

PRE-PROGRAMMED MCM68A332P2, MCM68A332C2

The −2 standard ROM pattern contains sine-lookup and arctan-lookup tables.

Locations 0000 through 2001 contain the sine values. The sine's first quadrant is divided into 1000 parts with sine values corresponding to these angles stored in the ROM. Sin $\pi/2$ is included and is rounded to 0.9999.

The arctan values contain angles in radians corresponding to the arc tangents of 0 through 1 in steps of 0.001 and are contained in locations 2048 through 4049.

Locations 2002 through 2047 and 4050 through 4095 are zero filled.

All values are represented in absolute decimal format with four digit precision. They are stored in BCD format with the two most significant digits in the lower byte and the two least significant digits in the upper byte. The decimal point is assumed to be to the left of the most significant digit.

Example: $\sin\left(\frac{1}{1000}\,\frac{\pi}{2}\right) = 0.0016$ decimal

Address	Contents	
0002	0000	0000
0003	0001	0110

FIGURE 3 — FORMAT FOR PROGRAMMING GENERAL OPTIONS

ORGANIZATIONAL DATA
MCM68A332 MOS READ ONLY MEMORY

Customer:

Company ______________________

Part No. ______________________

Originator ______________________

Phone No. ______________________

Motorola Use Only

Quote ______________________

Part No. ______________________

Specif. No. ______________________

Chip Select Options:

	Active High	Active Low	No-Connect
S1	☐	☐	☐
S2	☐	☐	☐

MOTOROLA

MCM68364

64K-BIT READ ONLY MEMORY

The MCM68364 is a mask-programmable byte-organized memory designed for use in bus-organized systems. It is fabricated with N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, and is TTL compatible. The addresses are latched with the Chip Enable input — no external latches required.

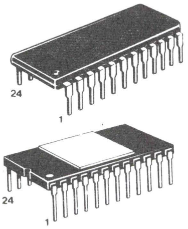
The memory is compatible with the M6800 Microcomputer Family, providing read only storage in byte increments. The Chip Enable input deselects the output and puts the chip in a power-down mode.

- Single ±10% 5-Volt Power Supply
- Automatic Power Down
- Low Power Dissipation
  - 150 mW active (typical)
  - 35 mW standby (typical)
- High Output Drive Capability (2 TTL Loads)
- Three-State Data Output for OR-Ties
- TTL Compatible
- Maximum Access Time
  - 200 ns — MCM68364-20
  - 250 ns — MCM68364-25
  - 300 ns — MCM68364-30
- Pin Compatible with 8K — MCM68A308, 16K — MCM68A316E, and 32K — MCM68A332 Mask-Programmable ROMs
- Pin Compatible with 24-pin 64K EPROM MCM68764

MOS

(N-CHANNEL, SILICON-GATE)

8192 X 8-BIT READ ONLY MEMORY

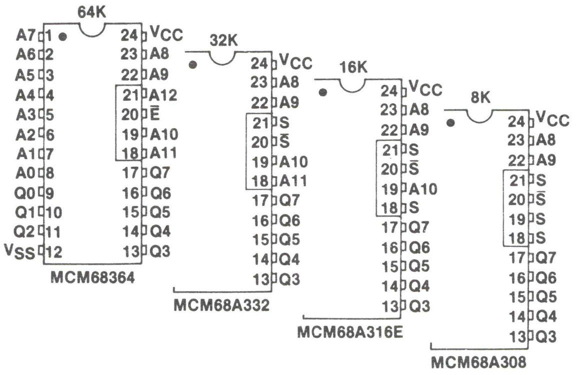


P SUFFIX
PLASTIC PACKAGE
CASE 709

L SUFFIX
CERAMIC PACKAGE
CASE 716

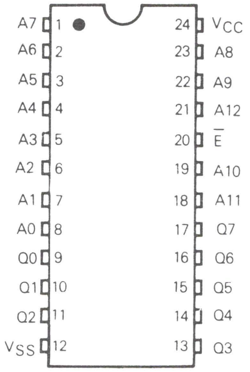
C SUFFIX FRIT-SEAL CERAMIC PACKAGE ALSO AVAILABLE — CASE 623

PIN COMPATIBLE ROM FAMILY
(INDUSTRY STANDARD PIN-OUTS)


64K
A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
Q0 9
Q1 10
Q2 11
VSS 12
24 VCC
23 A8
22 A9
21 A12
20 Ē
19 A10
18 A11
17 Q7
16 Q6
15 Q5
14 Q4
13 Q3
MCM68364
32K
24 VCC
23 A8
22 A9
21 S
20 S̄
19 A10
18 A11
17 Q7
16 Q6
15 Q5
14 Q4
13 Q3
MCM68A332
16K
24 VCC
23 A8
22 A9
21 S
20 S̄
19 A10
18 S
17 Q7
16 Q6
15 Q5
14 Q4
13 Q3
MCM68A316E
8K
24 VCC
23 A8
22 A9
21 S
20 S̄
19 S
18 S
17 Q7
16 Q6
15 Q5
14 Q4
13 Q3
MCM68A308

AA89-1

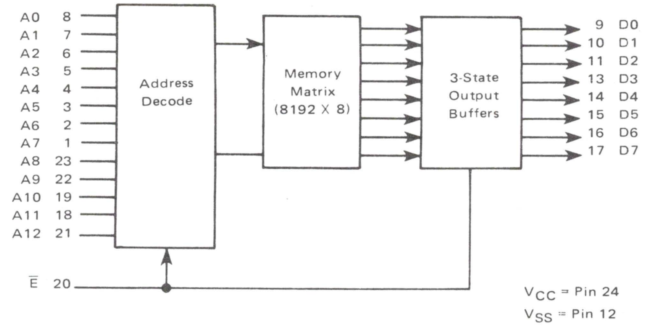
PIN ASSIGNMENT


A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
Q0 9
Q1 10
Q2 11
VSS 12
24 VCC
23 A8
22 A9
21 A12
20 Ē
19 A10
18 A11
17 Q7
16 Q6
15 Q5
14 Q4
13 Q3

PIN NAMES	
A0-A12	Address
Ē	Chip Enable
Q0-Q7	Data Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

BLOCK DIAGRAM


A0 8
A1 7
A2 6
A3 5
A4 4
A5 3
A6 2
A7 1
A8 23
A9 22
A10 19
A11 18
A12 21
Ē 20
Address Decode
Memory Matrix (8192 X 8)
3-State Output Buffers
9 D0
10 D1
11 D2
13 D3
14 D4
15 D5
16 D6
17 D7
V_{CC} = Pin 24
V_{SS} = Pin 12

ABSOLUTE MAXIMUM RATINGS (See note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	Vdc
Input Voltage	V_{in}	−0.5 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage (V_{CC} must be applied at least 100 μs before proper device operation is achieved, $\overline{E} = V_{IH}$)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0	—	V_{CC}	V
Input Low Voltage	V_{IL}	−0.3	—	0.8	V

RECOMMENDED OPERATING CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current (V_{in} = 0 to 5.5 V)	I_{in}	-10	—	10	μA
Output High Voltage (I_{OH} = -220 μA)	V_{OH}	2.4	—	—	V
Output Low Voltage (I_{OL} = 3.2 mA)	V_{OL}	—	—	0.4	V
Output Leakage Current (Three-State) ($\overline{E}$ = 2.0 V, V_{out} = 0 V to 5.5 V)	I_{LO}	-10	—	10	μA
Supply Current — Active* (Minimum Cycle Rate)	I_{CC}	—	25	40	mA
Supply Current — Standby (E = V_{IH})	I_{SB}	—	7	10	mA

*Current is proportional to cycle rate.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Input Capacitance	C_{in}	8	pF
Output Capacitance	C_{out}	15	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

Read Cycle

RECOMMENDED AC OPERATING CONDITIONS

($T_A = 0$ to 70°C, $V_{CC} = 5.0$ V ± 10%. All timing with $t_r = t_f = 20$ ns, loads of Figure 1)

Parameter	Symbol	MCM68364-20		MCM68364-25		MCM68364-30		Unit
		Min	Max	Min	Max	Min	Max	
Chip Enable Low to Chip Enable Low of Next Cycle (Cycle Time)	t_{ELEL}	300	–	375	–	450	–	ns
Chip Enable Low to Chip Enable High	t_{ELEH}	200	–	250	–	300	–	ns
Chip Enable Low to Output Valid (Access)	t_{ELQV}	–	200	–	250	–	300	ns
Chip Enable High to Output High Z (Off Time)	t_{EHQZ}	10	60	–	60	–	75	ns
Chip Enable Low to Address Don't Care (Hoid)	t_{ELAX}	60	–	60	–	75	–	ns
Address Valid to Chip Enable Low (Address Setup)	t_{AVEL}	0	–	0	–	0	–	ns
Chip Enable Precharge Time	t_{EHEL}	100	–	125	–	150	–	ns

TIMING DIAGRAM

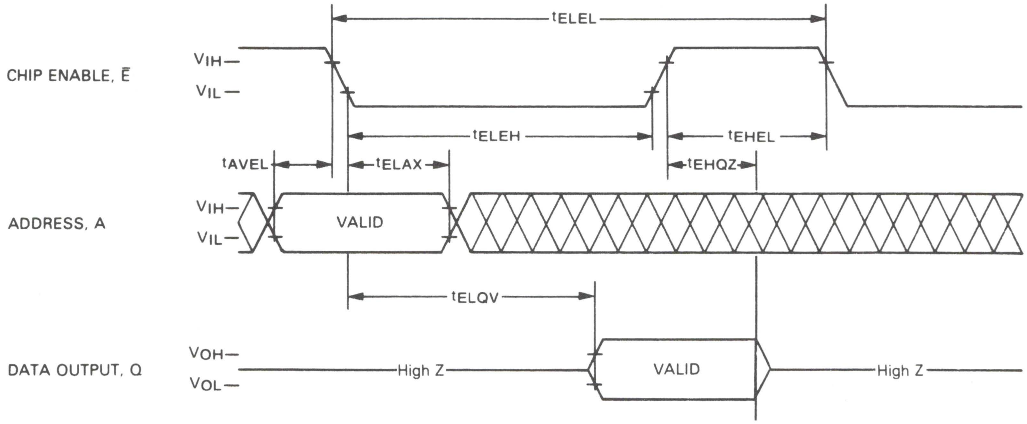
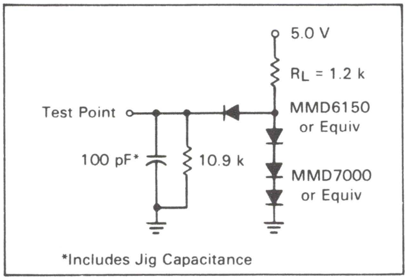

tELEL
CHIP ENABLE, Ē
VIH—
VIL—
tELEH
tEHEL
tAVEL
tELAX
tEHQZ
ADDRESS, A
VIH—
VIL—
VALID
tELQV
DATA OUTPUT, Q
VOH—
VOL—
High Z
VALID
High Z

FIGURE 1 — AC TEST LOAD


5.0 V
RL = 1.2 k
Test Point
MMD6150
or Equiv
100 pF*
10.9 k
MMD7000
or Equiv
*Includes Jig Capacitance

WAVEFORMS

Waveform Symbol	Input	Output
═	MUST BE VALID	WILL BE VALID
▧	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
▨	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
▩	DON'T CARE: ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
⟩		HIGH IMPEDANCE

PRODUCT DESCRIPTION

This Motorola MOS Read Only Memory (ROM), the MCM68364, is a clocked or edge enabled device. It makes use of virtual ground ROM cells and clocked peripheral circuitry, allowing a better speed-power product.

The MCM68364 has a period during which the non-static periphery must undergo a precharge. Therefore, the cycle time is slightly longer than the access time. It is essential that the precharge requirements are met to ensure proper address latching and avoid invalid output data. Once the address hold time has been met, new address information can be supplied in preparation for the next cycle.

CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM68364, the customer may specify the contents of the memory.

Information for custom memory content may be sent to Motorola in one of two forms (shown in order of preference):

1. EPROMs — one 64K (MCM68764), two 32K (MCM2532), four 16K (MCM2716 or TMS2716), or eight 8K (MCM2708).
2. Magnetic Tape — 9 Track, 800 bpi, odd parity written in EBCDIC character code. Motorola's R.O.M.S. format.

PRE-PROGRAMMED MCM68364P25-3

The −3 standard ROM pattern contains log (base 10) and antilog (base 10) lookup tables for the 64K ROM.

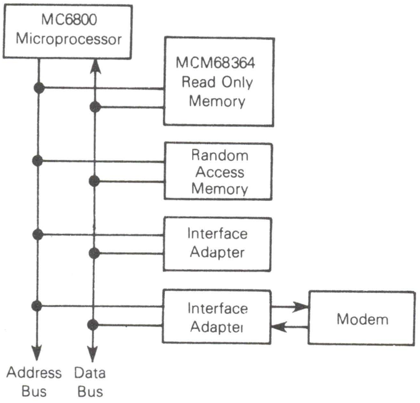
Locations 0000 through 3599 contain log base 10 values. The arguments for the log table range from 1.00 through 9.99 incrementing in steps of 1/100. Each log value is represented by an eight-digit decimal number with decimal point assumed to be to the left of the most significant digit.

Antilog (base 10) are stored in locations 4096 through 8095. The arguments range from .000 through .999 incrementing in steps of 1/1000. Each antilog value is represented by an eight-digit decimal number with decimal point assumed to be to the right of the most significant digit.

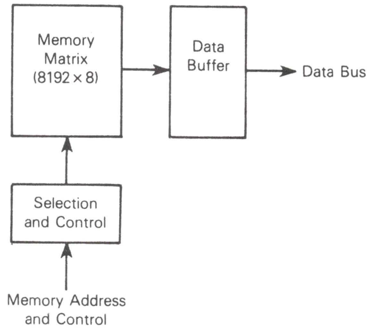
Locations 3600 through 4095 and 8096 through 8191 are zero filled.

All values are represented in absolute decimal format with eight digit precision. They are stored in BCD format with the two most significant digits in the lower byte and the remaining six digits in the three consecutive locations.

M6800 MICROCOMPUTER FAMILY
BLOCK DIAGRAM



READ ONLY MEMORY
BLOCK DIAGRAM



Example:
$\log_{10}(1.01) = .00432137$ decimal

Address	Contents	
4	0000	0000
5	0100	0011
6	0010	0001
7	0011	0111

MOTOROLA

MCM68365

64K BIT READ ONLY MEMORY

The MCM68365 is a mask-programmable byte-organized memory designed for use in bus-organized systems. It is fabricated with N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, has compatibility with TTL, and needs no clocks or refreshing due to its static operation.

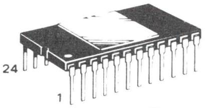
The memory is compatible with the M6800 Microcomputer Family, providing read only storage in byte increments. The active level of the Chip Enable input and the memory content are defined by the user. The Chip Enable input deselects the output and puts the chip in a power-down mode.

- Fully Static Operation
- Automatic Power Down
- Low Power Dissipation — 125 mW Active (Typical)
  25 mW Standby (Typical)
- Single ±10% 5-Volt Power Supply
- High Output Drive Capability (2 TTL Loads)
- Three-State Data Output for OR-Ties
- Mask Programmable Chip Enable
- TTL Compatible
- Maximum Access Time — 250 ns — MCM68365-25
  350 ns — MCM68365-35
- Pin Compatible with 8K — MCM68308, 16K — MCM68316E, and 32K — MCM68332, 64K — MCM68364, MCM68366 Mask-Programmable ROMs

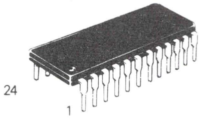
MOS

(N-CHANNEL, SILICON-GATE)

**8192 × 8-BIT
READ ONLY MEMORY**



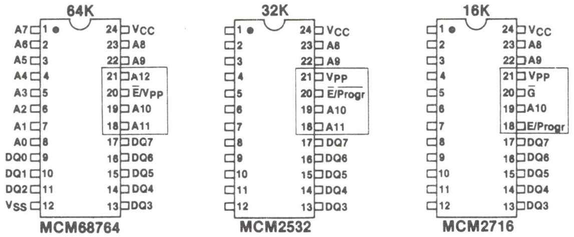
L SUFFIX
CERAMIC PACKAGE
CASE 716



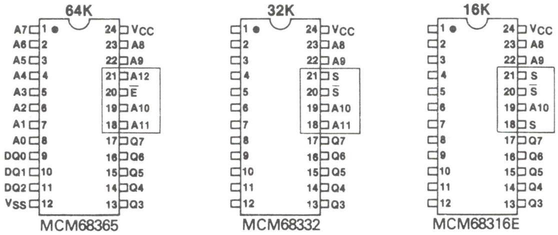
P SUFFIX
PLASTIC PACKAGE
CASE 709

C SUFFIX FRIT-SEAL CERAMIC PACKAGE
ALSO AVAILABLE — CASE 623

MOTOROLA'S PIN-COMPATIBLE EPROM FAMILY


64K
A7 1 24 VCC
A6 2 23 A8
A5 3 22 A9
A4 4 21 A12
A3 5 20 E/VPP
A2 6 19 A10
A1 7 18 A11
A0 8 17 DQ7
DQ0 9 16 DQ6
DQ1 10 15 DQ5
DQ2 11 14 DQ4
VSS 12 13 DQ3
MCM68764
32K
21 VPP
20 E/Progr
19 A10
18 A11
MCM2532
16K
21 VPP
20 G
19 A10
18 E/Progr
MCM2716

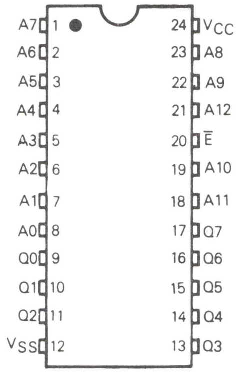
MOTOROLA'S PIN-COMPATIBLE ROM FAMILY


64K
A7 1 24 VCC
A6 2 23 A8
A5 3 22 A9
A4 4 21 A12
A3 5 20 E
A2 6 19 A10
A1 7 18 A11
A0 8 17 Q7
DQ0 9 16 Q6
DQ1 10 15 Q5
DQ2 11 14 Q4
VSS 12 13 Q3
MCM68365
32K
21 S
20 S
19 A10
18 A11
MCM68332
16K
21 S
20 S
19 A10
18 S
MCM68316E

INDUSTRY STANDARD PINOUTS

AA00090-1

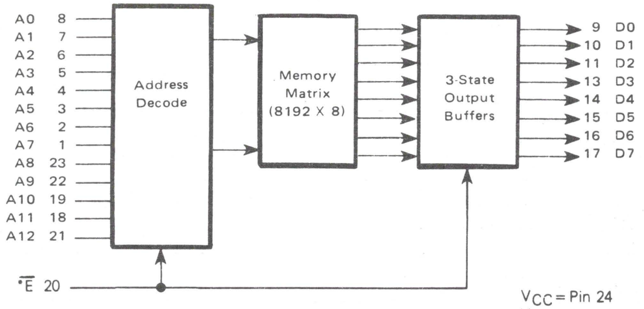
PIN ASSIGNMENT


A7 1 24 VCC
A6 2 23 A8
A5 3 22 A9
A4 4 21 A12
A3 5 20 Ē
A2 6 19 A10
A1 7 18 A11
A0 8 17 Q7
Q0 9 16 Q6
Q1 10 15 Q5
Q2 11 14 Q4
VSS 12 13 Q3

PIN NAMES	
A0-A12	Address
Ē	Chip Enable
Q0-Q7	Data Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

BLOCK DIAGRAM



V_{CC} = Pin 24
V_{SS} = Pin 12

*Active level defined by the user.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−1.0 to +7.0	V
Input Voltage	V_{in}	−1.0 to +7.0	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit	Notes
Supply Voltage (V_{CC} must be applied at least 100 μs before proper device operation is achieved)	V_{CC}	4.5	5.0	5.5	V	–
Input High Voltage	V_{IH}	2.0	–	5.5	V	–
Input Low Voltage	V_{IL}	−0.5	–	0.8		

RECOMMENDED OPERATING CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit	Notes
Input Current (V_{in} = 0 to 5.5 V)	I_{in}	−10	–	10	μA	1
Output High Voltage (I_{OH} = −205 μA)	V_{OH}	2.4	–	–	V	–
Output Low Voltage (I_{OL} = 3.2 mA)	V_{OL}	–	–	0.4	V	–
Output Leakage Current (Three-State) ($\overline{E}$ = 2.0 V, V_{out} = 0.4 V to 2.4 V)	I_{LO}	−10	–	10	μA	2
Supply Current — Active (V_{CC} = 5.5 V)	I_{CC}	–	20	60	mA	3
Supply Current — Standby (V_{CC} = 5.5 V)	I_{SB}	–	4	15	mA	4

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Input Capacitance	C_{in}	7.5	pF
Output Capacitance	C_{out}	12.5	pF

NOTES:
1. Measured a) forcing V_{CC} on one input pin at a time while all others are grounded, and
   b) maintaining 0.0 V on one pin at a time while all others are at V_{CC} = 4.5 V and 5.5 V.
2. Measured a) with A0-A12 = V_{SS} and forcing 0.4 V on one output at a time while all others are held at 2.4 V, and
   b) with A0-A12 = V_{SS} and force 2.4 on one output at a time while all others are held at 0.4 V (V_{CC} = 4.5 V and 5.5 V).
3. Measured with the Chip Enable ($\overline{E}$ = V_{IL}) addresses cycling, and the outputs unloaded.
4. Measured with the Chip Disabled ($\overline{E}$ = V_{IH}) and the outputs unloaded.

AC OPERATING CONDITIONS AND CHARACTERISTICS

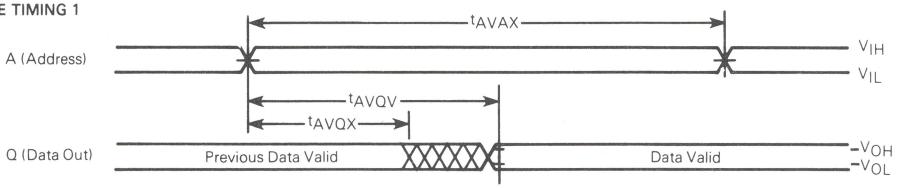
Read Cycle

RECOMMENDED OPERATING CONDITIONS (See Notes 5, 6)
($T_A = 0$ to 70°C, $V_{CC} = 5.0$ V ±10%. All timing with $t_r = t_f = 10$ ns, load of Figure 1)

Parameter	Symbol	MCM68365-25		MCM68365-35		Units
		Min	Max	Min	Max	
Address Valid to Address Don't Care (Cycle Time when Chip Enable is held Active)	t_{AVAX}	250	–	350	–	ns
Chip Enable Low to Chip Enable High	t_{ELEH}	250	–	350	–	ns
Address Valid to Output Valid (Access)	t_{AVQV}	–	250	–	350	ns
Chip Enable Low to Output Valid (Access)	t_{ELQV}	–	250	–	350	ns
Address Valid to Output Invalid	t_{AVQX}	20	–	20	–	ns
Chip Enable Low to Output Invalid	t_{ELQX}	10	–	10	–	ns
Chip Enable High to Output High-Z	t_{EHQZ}	10	80	10	80	ns
Chip Selection to Power Up Time	t_{PU}	0	–	0	–	ns
Chip Deselection to Power Down Time	t_{PD}	–	100	–	120	ns

5. $\overline{E}$ is represented by active low for illustrative purposes.
6. AC Test Conditions
   All times are guaranteed with worst case dc levels.
   Inputs: $V_{IH} = 2.0$ V or 5.5 V
   $V_{IL} = 0.8$ V or -0.5 V
   Measurement Levels: Input 1.5 V
   Output Low = 0.4 V
   High = 2.4 V

READ CYCLE TIMING 1
($\overline{E}$ Held Low)


tAVAX
A (Address)
VIH
VIL
tAVQV
tAVQX
Q (Data Out)
Previous Data Valid
Data Valid
VOH
VOL

READ CYCLE TIMING 2

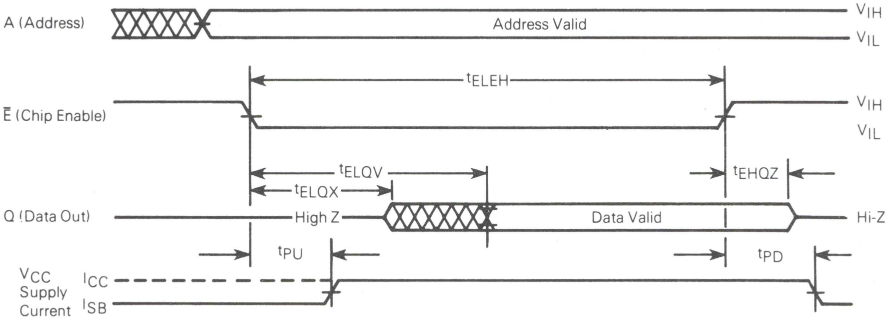
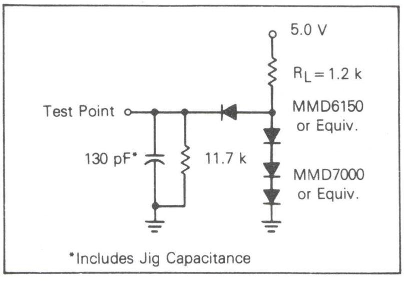

A (Address)
Address Valid
VIH
VIL
tELEH
Ē (Chip Enable)
VIH
VIL
tELQV
tELQX
tEHQZ
Q (Data Out)
High Z
Data Valid
Hi-Z
tPU
tPD
VCC Supply Current
ICC
ISB

FIGURE 1 — AC TEST LOAD


5.0 V
RL = 1.2 k
MMD6150 or Equiv.
Test Point
130 pF*
11.7 k
MMD7000 or Equiv.

*Includes Jig Capacitance

FIGURE 2 — ADDRESS ACCESS TIME VERSUS TEMPERATURE

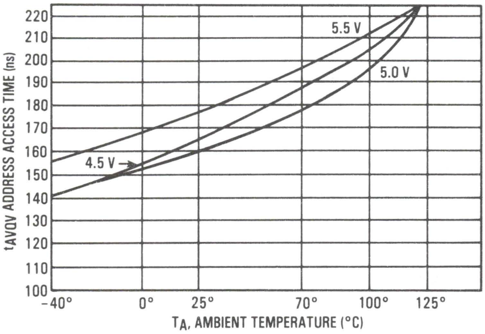


FIGURE 3 — I_{CC} SUPPLY CURRENT VERSUS TEMPERATURE

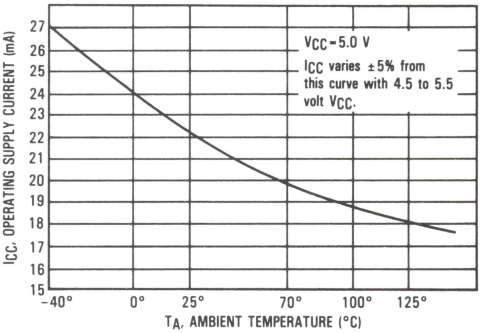
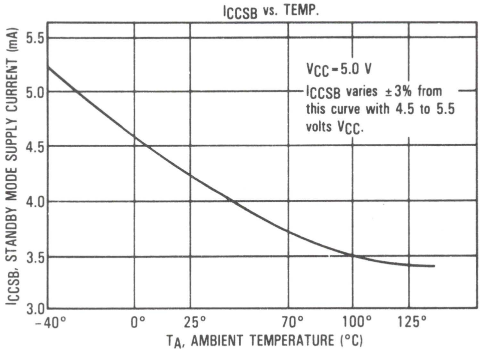


FIGURE 4 — I_{CCSB} STANDBY CURRENT VERSUS TEMPERATURE



PRE-PROGRAMMED MCM68365P35-3/C35-3, MCM68365P25-3/C25-3

The −3 standard ROM pattern contains log (base 10) and antilog (base 10) lookup tables for the 64K ROM.

Locations 0000 through 3599 contain log base 10 values. The arguments for the log table range from 1.00 through 9.99 incrementing in steps of 1/100. Each log value is represented by an eight-digit decimal number with decimal point assumed to be to the left of the most-significant digit.

Antilog (base 10) are stored in locations 4096 through 8095. The arguments range from .000 through .999 incrementing in steps of 1/1000. Each antilog value is represented by an eight-digit decimal number with decimal point assumed to be to the right of the most-significant digit.

Locations 3600 through 4095 and 8096 through 8191 are zero filled.

All values are represented in absolute decimal format with eight digit precision. They are stored in BCD format with the two most significant digits in the lower byte and the remaining six digits in the three consecutive locations.

Example: $\log_{10}(1.01) = 0.00432137$ decimal

Address	Contents	
4	0000	0000
5	0100	0011
6	0010	0001
7	0011	0111

CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM68365, the customer may specify the content of the memory and the method of enabling the outputs.

Information on the general options of the MCM68365 should be submitted on an Organizational Data form such as that shown in Figure 2.

Information for custom memory content may be sent to Motorola in one of two forms (shown in order of preference):

1. EPROMs — One 64K (MCM68764, MCM68766), two 32K (MCM2532), four 16K (MCM2716 or TMS2716), or eight 8K (MCM2708).
2. Magnetic Tape
   9 track, 800 bpi, odd parity written in EBCDIC character code. Motorola R.O.M.S. format.

FIGURE 2 — FORMAT FOR PROGRAMMING GENERAL OPTIONS

ORGANIZATIONAL DATA
MCM68365 MOS READ ONLY MEMORY

Customer:

Company ______________________________

Part No. ______________________________

Originator ______________________________

Phone No. ______________________________

Motorola Use Only:

Quote: ______________________

Part No: ______________________

Specif. No: ______________________

Enable Options:

	Active High	Active Low
Chip Enable	☐	☐

MCM68366

MOS

(N-CHANNEL, SILICON-GATE)

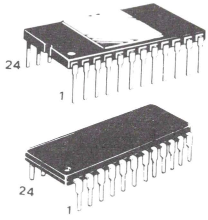
8192 × 8-BIT
READ ONLY MEMORY

64K BIT READ ONLY MEMORY

The MCM68366 is a mask-programmable byte-organized memory designed for use in bus-organized systems. It is fabricated with N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, has compatibility with TTL and needs no clocks or refreshing due to its static operation.

The memory is compatible with the M6800 Microcomputer Family, providing read only storage in byte increments. The active level of the Output Enable input and the memory content is defined by the user. The Output Enable input deselects the output.

- Fully Static Operation
- Fast Data Valid Time for High Speed Microprocessors
- Low Power Dissipation — 125 mW Active (Typical)
- Single ±10% 5-Volt Power Supply
- High Output Drive Capability (2 TTL Loads)
- Three-State Data Output for OR-Ties
- Mask Programmable Output Enable
- TTL Compatible
- Maximum Access Time — 120 ns from Output Enable
  250 ns from Address — MCM68366-25
  350 ns from Address — MCM68366-35
- Pin Compatible with 8K, 16K, and 32K — Mask-Programmable ROMs
- Pin Compatible with MCM68766 64K EPROM

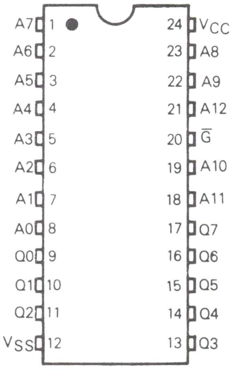


L SUFFIX
CERAMIC PACKAGE
CASE 716

P SUFFIX
PLASTIC PACKAGE
CASE 709

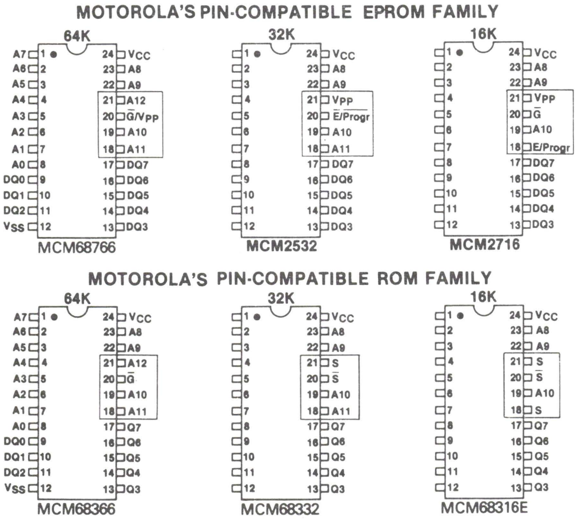
C SUFFIX FRIT-SEAL CERAMIC PACKAGE
ALSO AVAILABLE — CASE 623

PIN ASSIGNMENT


A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
Q0 9
Q1 10
Q2 11
V_{SS} 12
24 V_{CC}
23 A8
22 A9
21 A12
20 $\overline{G}$
19 A10
18 A11
17 Q7
16 Q6
15 Q5
14 Q4
13 Q3

PIN NAMES	
A0-A12	Address
$\overline{G}$	Output Enable
Q0-Q7	Data Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

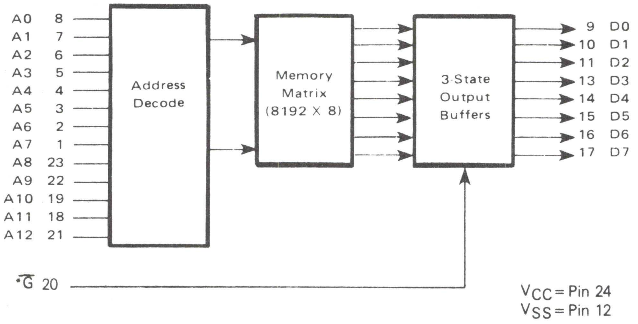
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.


MOTOROLA'S PIN-COMPATIBLE EPROM FAMILY
64K
A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
DQ0 9
DQ1 10
DQ2 11
V_{SS} 12
24 V_{CC}
23 A8
22 A9
21 A12
20 $\overline{G}$/V_{PP}
19 A10
18 A11
17 DQ7
16 DQ6
15 DQ5
14 DQ4
13 DQ3
MCM68766
32K
24 V_{CC}
23 A8
22 A9
21 V_{PP}
20 $\overline{E}$/Progr
19 A10
18 A11
17 DQ7
16 DQ6
15 DQ5
14 DQ4
13 DQ3
MCM2532
16K
24 V_{CC}
23 A8
22 A9
21 V_{PP}
20 $\overline{G}$
19 A10
18 E/Progr
17 DQ7
16 DQ6
15 DQ5
14 DQ4
13 DQ3
MCM2716
MOTOROLA'S PIN-COMPATIBLE ROM FAMILY
64K
A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
DQ0 9
DQ1 10
DQ2 11
V_{SS} 12
24 V_{CC}
23 A8
22 A9
21 A12
20 $\overline{G}$
19 A10
18 A11
17 Q7
16 Q6
15 Q5
14 Q4
13 Q3
MCM68366
32K
24 V_{CC}
23 A8
22 A9
21 S
20 $\overline{S}$
19 A10
18 A11
17 Q7
16 Q6
15 Q5
14 Q4
13 Q3
MCM68332
16K
24 V_{CC}
23 A8
22 A9
21 S
20 $\overline{S}$
19 A10
18 S
17 Q7
16 Q6
15 Q5
14 Q4
13 Q3
MCM68316E

INDUSTRY STANDARD PINOUTS

AA00090-1

BLOCK DIAGRAM



*Active Level Defined by the User

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−1.0 to +7.0	V
Input Voltage	V_{in}	−1.0 to +7.0	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit	Notes
Supply Voltage (V_{CC} must be applied at least 100 μs before proper device operation is achieved)	V_{CC}	4.5	5.0	5.5	V	–
Input High Voltage	V_{IH}	2.0	–	5.5	V	–
Input Low Voltage	V_{IL}	−0.5	–	0.8		

RECOMMENDED OPERATING CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit	Notes
Input Current (V_{in} = 0 to 5.5 V)	I_{in}	−10	–	10	μA	1
Output High Voltage (I_{OH} = −205 μA)	V_{OH}	2.4	–	–	V	–
Output Low Voltage (I_{OL} = 3.2 mA)	V_{OL}	–	–	0.4	V	–
Output Leakage Current (Three-State) (G = 2.0 V, V_{out} = 0.4 V to 2.4 V)	I_{LO}	−10	–	10	μA	2
Supply Current (V_{CC} = 5.5 V)	I_{CC}	–	20	60	mA	3

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Input Capacitance	C_{in}	7.5	pF
Output Capacitance	C_{out}	12.5	pF

NOTES: 1. Measured a) forcing V_{CC} on one input pin at a time, while all others are grounded (V_{SS}), and
b) maintaining 0.0 V (V_{SS}) on one pin at a time, while all others are at V_{CC} = 4.5 V and 5.5 V.
2. Measured a) with A0-A12 = V_{SS} and forcing 0.4 V on one output at a time while all others are held at 2.4 V, and
b) with A0-A12 = V_{SS} and forcing 2.4 V on one output at a time while all others are held at 0.4 V (V_{CC} = 4.5 V and 5.5 V).
3. Measured with the Output Enabled ($\overline{G} = V_{IL}$), addresses cycling and the outputs unloaded.

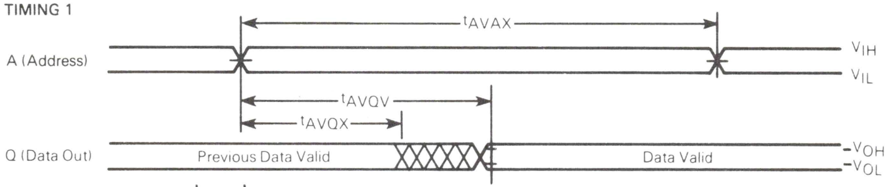
AC OPERATING CONDITIONS AND CHARACTERISTICS
Read Cycle

RECOMMENDED OPERATING CONDITIONS (See Notes 4, 5)
($T_A = 0$ to 70°C, $V_{CC} = 5.0$ V ± 10%. All timing with $t_r = t_f = 10$ ns, load of Figure 1)

Parameter	Symbol	MCM68366-25		MCM68366-35		Unit
		Min	Max	Min	Max	
Address Valid to Address Don't Care (Cycle Time when Output Enable is Held Active)	t_{AVAX}	250	–	350	–	ns
Address Valid to Output Valid (Access)	t_{AVQV}	–	250	–	350	ns
Output Enable Low to Output Valid (Access)	t_{GLQV}	–	120	–	120	ns
Address Valid to Output Invalid	t_{AVQX}	10	–	10	–	ns
Output Enable Low to Output Invalid	t_{GLQX}	10	–	10		ns
Output Enable High to Output High Z	t_{GHQZ}	0	80	0	80	ns
Address Valid to Output Enable Low (Note 6)	t_{AVGL}	130	–	230	–	ns

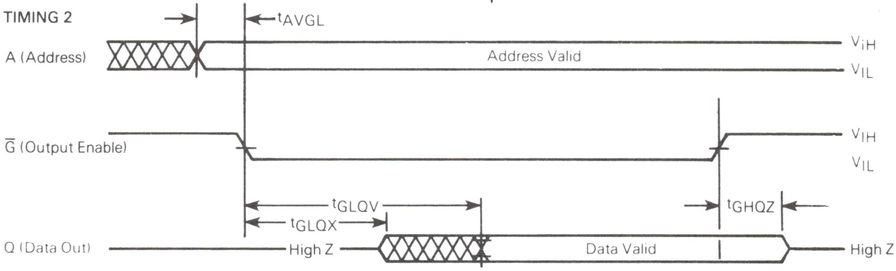
4. $\overline{G}$ represented as active low for illustrative purposes.
5. AC Test Conditions
   All times are guaranteed with worst case dc levels.
   Inputs: $V_{IH} = 2.0$ V or 5.5 V
   $V_{IL} = 0.8$ V or −0.5 V
   Measurement Levels: Input 1.5 V
   Output Low = 0.4 V
   High = 2.4 V
6. A faster minimum time is allowed, but the timing must then be referenced to t_{AVQV} and t_{AVQX}.

READ CYCLE TIMING 1
($\overline{G}$ Held Low)



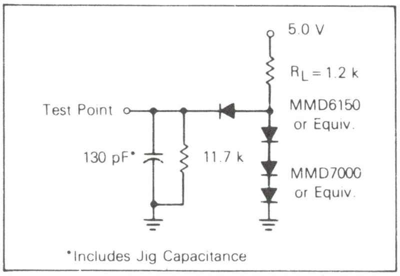
tAVAX
A (Address)
VIH
VIL
tAVQV
tAVQX
Q (Data Out)
Previous Data Valid
Data Valid
VOH
VOL

READ CYCLE TIMING 2



tAVGL
A (Address)
Address Valid
VIH
VIL
G̅ (Output Enable)
VIH
VIL
tGLQV
tGLQX
tGHQZ
Q (Data Out)
High Z
Data Valid
High Z

FIGURE 1 — AC TEST LOAD



5.0 V
RL = 1.2 k
MMD6150 or Equiv.
Test Point
130 pF*
11.7 k
MMD7000 or Equiv.

*Includes Jig Capacitance

FIGURE 2 — ADDRESS ACCESS TIME
VERSUS TEMPERATURE

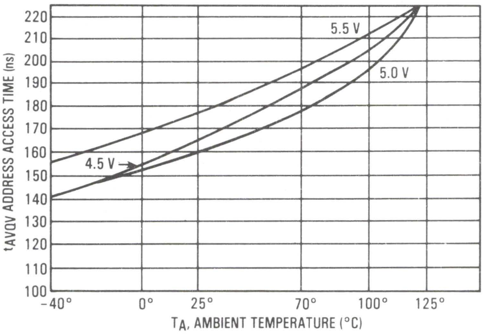


FIGURE 3 — I_{CC} SUPPLY CURRENT
VERSUS TEMPERATURE

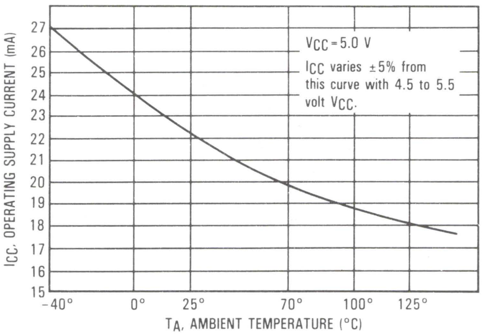
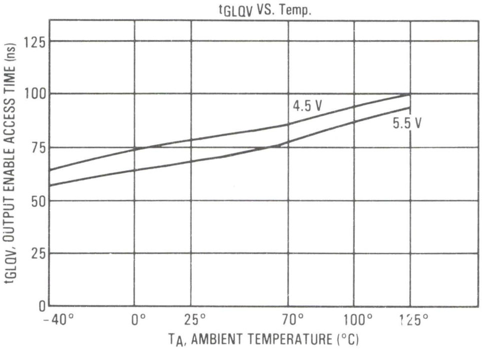


FIGURE 4 — OUTPUT ENABLE ACCESS
VERSUS TEMPERATURE



PRE-PROGRAMMED MCM68366P35-3/C35-3, MCM68366P25-3/C25-3

The −3 standard ROM pattern contains log (base 10) and antilog (base 10) lookup tables for the 64K ROM.

Locations 0000 through 3599 contain log base 10 values. The arguments for the log table range from 1.00 through 9.99 incrementing in steps of 1/100. Each log value is represented by an eight-digit decimal number with decimal point assumed to be to the left of the most-significant digit.

Antilog (base 10) are stored in locations 4096 through 8095. The arguments range from 0.000 through 0.999 incrementing in steps of 1/1000. Each antilog value is represented by an eight-digit decimal number with decimal point assumed to be to the right of the most-significant digit.

Locations 3600 through 4095 and 8096 through 8191 are zero filled.

All values are represented in absolute decimal format with eight digit precision. They are stored in BCD format with the two most significant digits in the lower byte and the remaining six digits in the three consecutive locations.

Example: $\log_{10}$ (1.01) = .00432137 decimal

Address	Contents	
4	0000	0000
5	0100	0011
6	0010	0001
7	0011	0111

CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM68366, the customer may specify the content of the memory and the method of enabling the outputs.

Information on the general options of the MCM68366 should be submitted on an Organizational Data form such as that shown in Figure 3.

Information for custom memory content may be sent to Motorola in one of two forms (shown in order of preference):

1. EPROMs — one 64K (MCM68764, MCM68766), two 32K (MCM2532), four 16K (MCM2716, or TMS2716), or eight 8K (MCM2708).
2. Magnetic Tape
   9 track, 800 bpi, odd parity written in EBCDIC character Code. Motorola's R.O.M.S. format.

FIGURE 3 — FORMAT FOR PROGRAMMING GENERAL OPTIONS

ORGANIZATIONAL DATA
MCM68366 MOS READ ONLY MEMORY

Customer:

Company ______________________

Part No. ______________________

Originator ______________________

Phone No. ______________________

Motorola Use Only:

Quote: ______________________

Part No: ______________________

Specif. No: ______________________

Enable Options:

	Active High	Active Low
Output Enable	☐	☐

MOTOROLA

MCM63256

Product Preview

256K BIT READ ONLY MEMORY

The MCM63256 is a MOS mask programmable byte-organized Read Only Memory (ROM). The MCM63256 is organized as 32,768 bytes of 8 bits and is fabricated using Motorola's high performance N-channel silicon gate technology (HMOS). This device is designed to provide maximum circuit density and reliability with highest possible performance while maintaining low power dissipation and wide operating margins and remaining fully compatible with TTL inputs and outputs.

The active level of the Chip Enable and the Output Enable, along with the memory contents, are defined by the user. The Chip Enable input deselects the output and puts the chip in a power-down mode.

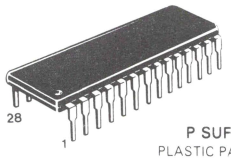
- Single ± 10% +5 Volt Power Supply
- Fully Static Periphery — No Clocking Required on Chip Enable
- Automatic Power Down
- Power Dissipation
    - 100 mA Active (Maximum) (Unloaded)
    - 15 mA Standby (Maximum)
- Current Surge Suppression When Powering Up Device
- Program Layer Late in Process for Quick Turnaround Time
- 150 ns Maximum Access from Address and Chip Enable
- 28-Pin JEDEC Standard Package and Pinout

ADDITIONAL FEATURE

- Address (A14) is User Selectable for Either Pin 27 or Pin 1

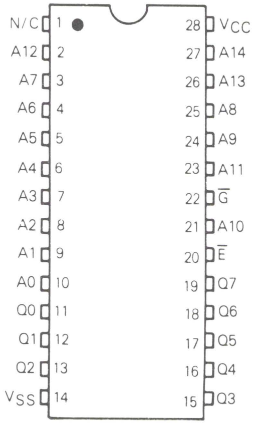
HMOS
(N-CHANNEL, SILICON GATE)

32,768 × 8 BIT
READ ONLY MEMORY



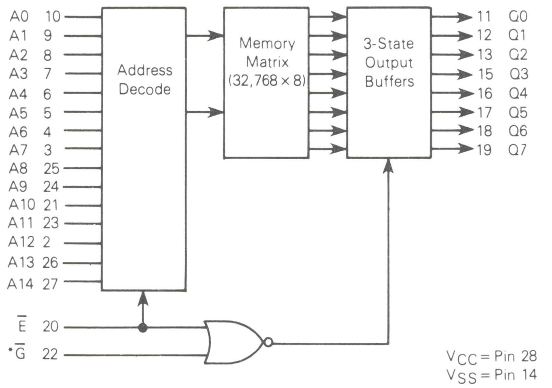
P SUFFIX
PLASTIC PACKAGE
CASE 710

PIN ASSIGNMENT


N/C 1
A12 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
Q0 11
Q1 12
Q2 13
VSS 14
28 VCC
27 A14
26 A13
25 A8
24 A9
23 A11
22 G̅
21 A10
20 E̅
19 Q7
18 Q6
17 Q5
16 Q4
15 Q3

PIN NAMES	
A0-A14	Address
E̅	Chip Enable
G̅	Output Enable
Q0-Q7	Data Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

BLOCK DIAGRAM


A0 10
A1 9
A2 8
A3 7
A4 6
A5 5
A6 4
A7 3
A8 25
A9 24
A10 21
A11 23
A12 2
A13 26
A14 27
Address Decode
Memory Matrix (32,768 × 8)
3-State Output Buffers
11 Q0
12 Q1
13 Q2
15 Q3
16 Q4
17 Q5
18 Q6
19 Q7
E̅ 20
•G̅ 22
VCC = Pin 28
VSS = Pin 14

*Active level defined by the user.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MOTOROLA

MCM65256

Product Preview

HCMOS
(COMPLEMENTARY MOS)

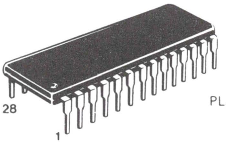
32,768 × 8 BIT
READ ONLY MEMORY

256K BIT READ ONLY MEMORY

The MCM65256 is a complementary MOS mask programmable byte-organized Read Only Memory (ROM). The MCM65256 is organized as 32,768 bytes of 8 bits and is fabricated using Motorola's high performance silicon gate CMOS technology (HCMOS). This device is designed to provide maximum circuit density and reliability with highest possible performance while maintaining low power dissipation and wide operating margins. The MCM65256 offers low-power operation from a single +5 Volt supply and is fully TTL compatible on all inputs and outputs.

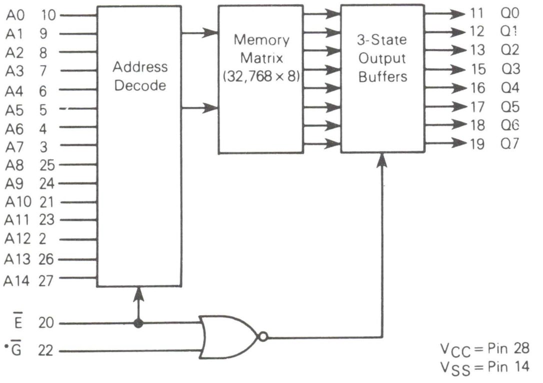
The active level of the Chip Enable and the Output Enable, along with the memory contents, are defined by the user. The Chip Enable input deselects the output and puts the chip in a power-down mode.

- Single ±10% +5 Volt Power Supply
- Fully Static Periphery — No Clocking Required on Chip Enable
- 250 ns Maximum Access from Address and Chip Enable
- Automatic Power Down
- Active Current 50 mA Maximum (Unloaded at a 250 ns Cycle Time) — Decreases with Increasing Cycle Time
- D.C. Active Current 10 mA Maximum
- Standby Current 50 μA Maximum (Full Rail Inputs)
- Standby Current 3.0 mA Maximum (TTL Inputs)
- Mask Programmable Chip Enable and Output Enable
- Program Layer Late in Process for Quick Turnaround Time
- 28-Pin JEDEC Standard Package and Pinout
- Address (A14) is User Selectable for Either Pin 27 or Pin 1



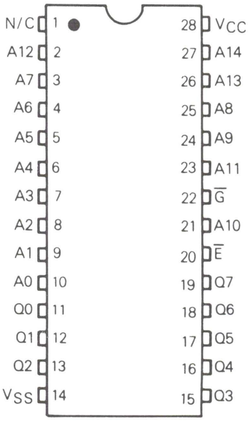
P SUFFIX
PLASTIC PACKAGE
CASE 710

BLOCK DIAGRAM


A0 10
A1 9
A2 8
A3 7
A4 6
A5 5
A6 4
A7 3
A8 25
A9 24
A10 21
A11 23
A12 2
A13 26
A14 27
Address Decode
Memory Matrix (32,768 × 8)
3-State Output Buffers
11 Q0
12 Q1
13 Q2
15 Q3
16 Q4
17 Q5
18 Q6
19 Q7
$\overline{E}$ 20
*$\overline{G}$ 22
V_{CC} = Pin 28
V_{SS} = Pin 14

*Active level defined by the user.

PIN ASSIGNMENT

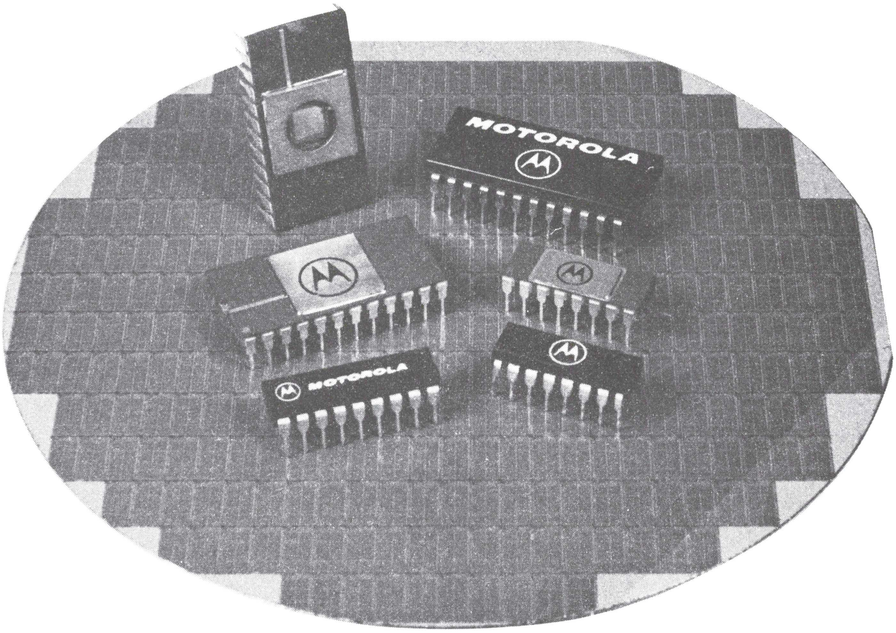

N/C 1
A12 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
Q0 11
Q1 12
Q2 13
V_{SS} 14
28 V_{CC}
27 A14
26 A13
25 A8
24 A9
23 A11
22 $\overline{G}$
21 A10
20 $\overline{E}$
19 Q7
18 Q6
17 Q5
16 Q4
15 Q3

PIN NAMES

A0-A14	Address
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
Q0-Q7	Data Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

TTL RAM


MOTOROLA
MOTOROLA

MOTOROLA

MCM93412
MCM93422

Advance Information

1024-BIT RANDOM ACCESS MEMORY

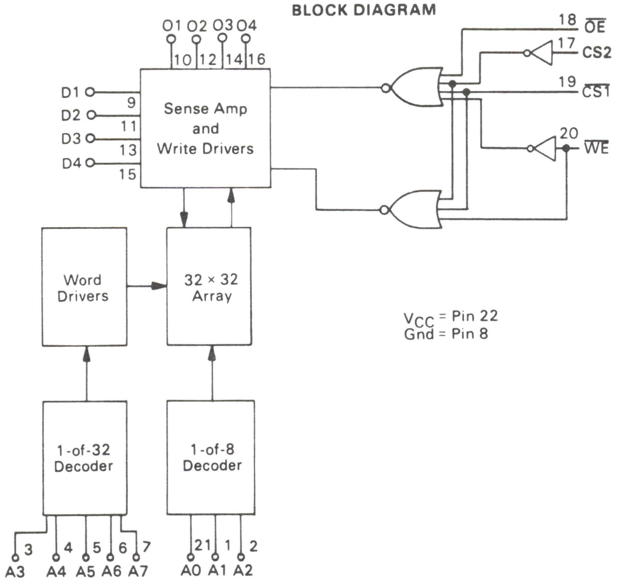
The MCM93412/422 is a 1024-bit Read/Write RAM, organized 256 words by 4 bits.

The MCM93412/422 is designed for high performance main memory and control storage applications and has a typical address time of 30 ns.

The MCM93412/422 has full decoding on-chip, separate data input and data output lines, an active low-output enable, write enable, and two chip selects, one active high, one active low. The device is fully compatible with standard DTL and TTL logic families. A three-state output is provided on the MCM93422 to drive bus-organized systems and/or highly capacitive loads. An uncommitted collector output is provided on the MCM93412 for ease of memory expansion.

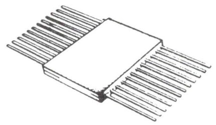
- Three-State Output or Uncommitted Collector Output
- TTL Inputs and Output
- Non-Inverting Data Output
- Full 16 mA Outputs Drive 30 pF Loads
- High Speed —
  Access Time — 30 ns Typical
  Chip Select — 15 ns Typical
- Power Dissipation — 0.5 mW/Bit Typical
- Standard 22-Pin Package
- Power Dissipation Decreases with Increasing Temperature
- Organized 256 Words × 4 Bits
- Two Chip Select Lines for Memory Expansion

BLOCK DIAGRAM

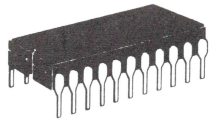

O1 O2 O3 O4
10 12 14 16
D1 9
D2 11
D3 13
D4 15
Sense Amp and Write Drivers
18 $\overline{OE}$
17 CS2
19 $\overline{CS1}$
20 $\overline{WE}$
Word Drivers
32 × 32 Array
V_{CC} = Pin 22
Gnd = Pin 8
1-of-32 Decoder
1-of-8 Decoder
3 4 5 6 7
A3 A4 A5 A6 A7
21 1 2
A0 A1 A2

TTL
256 × 4-BIT
RANDOM ACCESS MEMORY

MCM93412 — OPEN COLLECTOR
MCM93422 — THREE-STATE



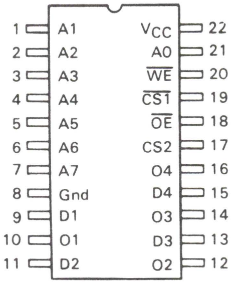
F SUFFIX
CERAMIC PACKAGE
CASE 652



D SUFFIX
CERAMIC PACKAGE
CASE 736

Plastic package to be announced.

PIN ASSIGNMENT


1 A1
2 A2
3 A3
4 A4
5 A5
6 A6
7 A7
8 Gnd
9 D1
10 O1
11 D2
22 V_{CC}
21 A0
20 $\overline{WE}$
19 $\overline{CS1}$
18 $\overline{OE}$
17 CS2
16 O4
15 D4
14 O3
13 D3
12 O2

Pin Description

$\overline{CS}$	Chip Select
A0–A7	Address Inputs
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
D_n	Data Input
O_n	Data Output

FUNCTIONAL DESCRIPTION

The MCM93412 and the MCM93422 are fully decoded 1024-bit Random Access Memories organized 256 words by 4 bits. Word selection is achieved by means of an 8-bit address, A0–A7.

The Chip Select ($\overline{CS1}$ and CS2) inputs provide for memory array expansion. For large memories, the fast chip select time permits the decoding of chip select from the address without increasing address access time.

The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$, Pin 20). With $\overline{WE}$ and $\overline{CS1}$ held low and the CS2 held high, the data at D_n is written into the addressed location. To read, $\overline{WE}$ and CS2 are held in high and $\overline{CS1}$ is held low. Data in the specified location is presented at O_n and is non-inverted.

The three-state output of the MCM93422 provides drive capability for higher speeds with capacitive load systems. The third state (high impedance) allows bus-organized systems where multiple outputs are connected to a common bus.

During writing, the output is held in the high-impedance state.

Uncommitted collector outputs of the MCM93412 are provided to allow wired-OR applications. In any application an external pull-up resistor of R_L value must be used to provide a high at the output when it is off. Any R_L value within the range specified below may be used.

$$\frac{V_{CC}(Min)}{I_{OL} - FO(1.6)} \leqslant R_L \leqslant \frac{V_{CC}(Min) - V_{OH}}{n(I_{CEX}) + FO(0.04)}$$

R_L is in kΩ
n = number of wired-OR outputs tied together
FO = number of TTL Unit Loads (UL) driven
I_{CEX} = Memory Output Leakage Current
V_{OH} = Required Output High Level at Output Node
I_{OL} = Output Low Current.

The minimum R_L value is limited by output current sinking ability. The minimum R_L value is determined by the output and input leakage current which must be supplied to hold the output at V_{OH}. One Unit Load = 40 μA High/1.6 mA Low.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature	
Ceramic Package (D and F Suffix)	−55°C to +165°C
Plastic Package (P Suffix)	−55°C to +125°C
Operating Junction Temperature, T_J	
Ceramic Package (D and F Suffix)	<165°C
Plastic Package (P Suffix)	<125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
Input Voltage (dc)	−0.5 V to +5.5 V
Voltage Applied to Outputs (Output High)	−0.5 V to +5.5 V
Output Current (dc) (Output Low)	+20 mA
Input Current (dc)	−12 mA to +5.0 mA

NOTE 1: Device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

GUARANTEED OPERATING RANGES (Note 2)

Part Number	Supply Voltage (V_{CC})			Ambient Temperature (T_A)
	Min	Nom	Max	
MCM934XXDC, PC	4.75 V	5.0 V	5.25 V	0°C to +75°C
MCM934XXFM, DM	4.50 V	5.0 V	5.50 V	−55°C to +125°C

DC OPERATING CONDITONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

Symbol	Characteristic	Limits		Units	Conditions
		Min	Max		
V_{OL}	Output Low Voltage		0.45	Vdc	V_{CC} = Min, I_{OL} = 16 mA
V_{IH}	Input High Voltage	2.1		Vdc	Guaranteed Input High Voltage for all Inputs
V_{IL}	Input Low Voltage		0.8	Vdc	Guaranteed Input Low Voltage for all Inputs
I_{IL}	Input Low Current		−400	μAdc	V_{CC} = Max, V_{in} = 0.4 V
I_{IH}	Input High Current		40	μAdc	V_{CC} = Max, V_{in} = 4.5 V
			1.0	mAdc	V_{CC} = Max, V_{in} = 5.25 V
I_{off}	Output Current (High Z) (MCM93422 only)		50	μAdc	V_{CC} = Max, V_{out} = 2.4 V
			−50		V_{CC} = Max, V_{out} = 0.5 V
I_{OS}	Output Current Short Circuit to Ground (MCM93422 only)		−100	mAdc	V_{CC} = Max
V_{OH}	Output High Voltage MCM93422DC, PC	2.4		Vdc	I_{OH} = −10.3 mA, V_{CC} = 5.0 V ±5%
	MCM93422FM, DM	2.4		Vdc	I_{OH} = −5.2 mA, V_{CC} = 5.0 V ±10%
V_{CD}	Input Diode Clamp Voltage		−1.5	Vdc	V_{CC} = Max, I_{in} = −10 mA
I_{CC}	Power Supply Current		130	mAdc	T_A = Max V_{CC} = Max, All Inputs Grounded
			155	mAdc	T_A = 0°C
			170	mAdc	T_A = Min
I_{CEX}	Output Leakage Current (MCM93412 only)		100	μAdc	V_{CC} = Max, V_{out} = 4.5 V

TRUTH TABLE

Inputs					Output	Mode
$\overline{OE}$	$\overline{CS1}$	CS2	$\overline{WE}$	D_n	O_n	
X	H	X	X	X	High Z (H)	Not Selected
X	X	L	X	X	High Z (H)	Not Selected
X	L	H	L	L	High Z (H)	Write "0"
X	L	H	L	H	High Z (H)	Write "1"
H	X	X	X	X	High Z (H)	Output Disabled
L	L	H	H	X	O_n	Read

H = High Voltage Level
L = Low Voltage Level
X = Don't Care (High or Low)

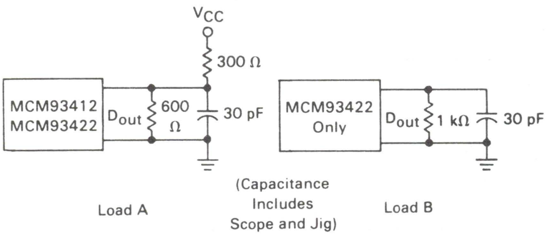
(H) Output of Open Collector Device is High.

AC OPERATING CONDITIONS AND CHARACTERISTICS

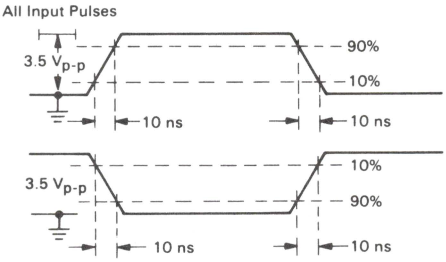
(Full operating voltage and temperature unless otherwise noted)

AC TEST LOAD AND WAVEFORMS

Loading Conditions


VCC
300 Ω
MCM93412
MCM93422
Dout
600 Ω
30 pF
MCM93422 Only
Dout
1 kΩ
30 pF
Load A
(Capacitance Includes Scope and Jig)
Load B

Input Pulses

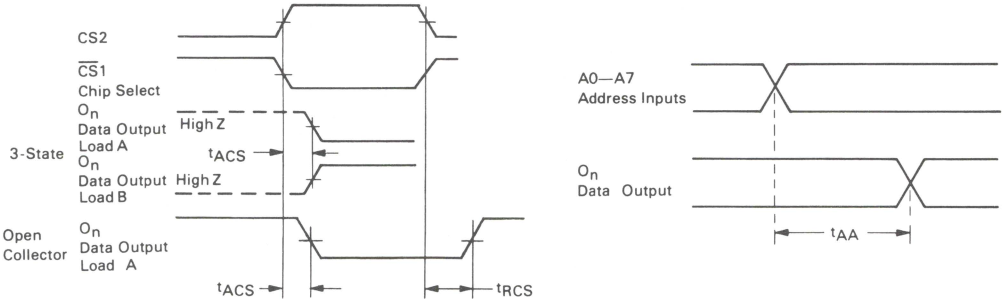

All Input Pulses
3.5 Vp-p
90%
10%
10 ns
10 ns
3.5 Vp-p
10%
90%
10 ns
10 ns

Symbol	Characteristic (Notes 2, 4)	MCM93412DC, PC MCM93422DC, PC Min	MCM93412DC, PC MCM93422DC, PC Max	MCM93412DM MCM93422DM, FM Min	MCM93412DM MCM93422DM, FM Max	Units	Conditions
READ MODE	DELAY TIMES					ns	
t_{ACS}	Chip Select Time		30		45		See Test Circuit and Waveforms
t_{ZRCS}, [t_{RCS}]	Chip Select to High Z [Chip Select Disable Time]		30		45		
t_{AOS}	Output Enable Time		30		45		
t_{ZROS}, [t_{ROS}]	Output Enable to High Z [Output Disable Time]		30		45		
t_{AA}	Address Access Time		45		60		
WRITE MODE	DELAY TIMES					ns	
t_{ZWS}, [t_{WS}]	Write Disable to High Z [Write Disable Time]		35		45		See Test Circuit and Waveforms
t_{WR}	Write Recovery Time		40		50		
	INPUT TIMING REQUIREMENTS					ns	
t_W	Write Pulse Width (to guarantee write)	30		40			See Test Circuit and Waveforms
t_{WSD}	Date Setup Time Prior to Write	5		5			
t_{WHD}	Data Hold Time After Write	5		5			
t_{WSA}	Address Setup Time (at t_W = Min)	10		10			
t_{WHA}	Address Hold Time	5		10			
t_{WSCS}	Chip Select Setup Time	5		5			
t_{WHCS}	Chip Select Hold Time	5		5			

[ ] Open Collector parameters for MCM93412 only.

READ OPERATION TIMING DIAGRAM

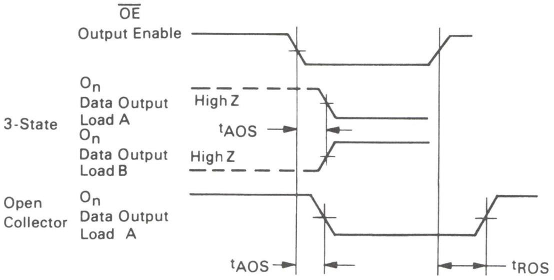
(All Time Measurements Referenced to 1.5 V)


CS2
$\overline{\text{CS}}$1
Chip Select
O_n
Data Output
Load A
3-State
O_n
Data Output
Load B
High Z
High Z
t_{ACS}
Open
Collector
O_n
Data Output
Load A
t_{ACS}
t_{RCS}
A0—A7
Address Inputs
O_n
Data Output
t_{AA}

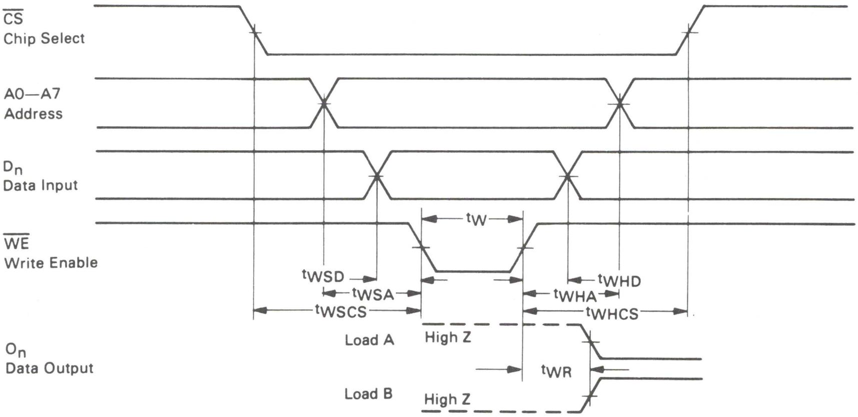
Propagation Delay from Chip Select

Propagation Delay from Address Inputs

Propagation Delay from Output Enable

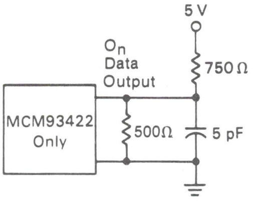

$\overline{\text{OE}}$
Output Enable
3-State
O_n
Data Output
Load A
O_n
Data Output
Load B
High Z
High Z
t_{AOS}
Open
Collector
O_n
Data Output
Load A
t_{AOS}
t_{ROS}

WRITE CYCLE TIMING

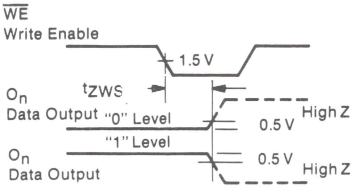

$\overline{\text{CS}}$
Chip Select
A0—A7
Address
D_n
Data Input
$\overline{\text{WE}}$
Write Enable
t_W
t_{WSD}
t_{WSA}
t_{WSCS}
t_{WHD}
t_{WHA}
t_{WHCS}
O_n
Data Output
Load A
High Z
t_{WR}
Load B
High Z

(All above measurements reference to 1.5 V.)

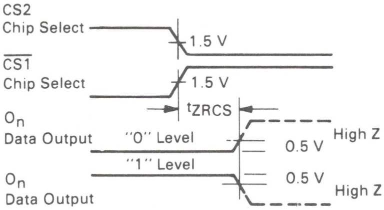
WRITE ENABLE TO HIGH Z DELAY (MCM93422 only)


5 V
On
Data
Output
750 Ω
MCM93422
Only
500Ω
5 pF

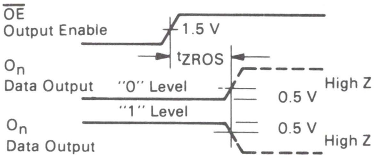
Load C


WE
Write Enable
1.5 V
tZWS
On
Data Output "0" Level
"1" Level
On
Data Output
0.5 V
0.5 V
High Z
High Z

Propagation Delay from Chip Select to High Z


CS2
Chip Select
1.5 V
CS1
Chip Select
1.5 V
tZRCS
On
Data Output
"0" Level
"1" Level
On
Data Output
0.5 V
0.5 V
High Z
High Z

Propagation Delay from Output Enable to High Z


OE
Output Enable
1.5 V
tZROS
On
Data Output
"0" Level
"1" Level
On
Data Output
0.5 V
0.5 V
High Z
High Z

(All t_{ZXXX} parameters are measured at a delta of 0.5 V from the logic level and using Load C.)

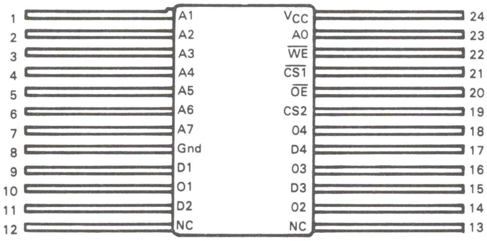
NOTE 2: DC and AC specifications limits guaranteed with 500 linear feet per minute blown air. Contact your Motorola sales representative if extended temperature or modified operating conditions are desired.

NOTE 3: Output short circuit conditions must not exceed 1 second duration.

NOTE 4: The maximum address access time is guaranteed to be the worst-case bit in the memory.

Package	θ_{JA} **(Junction to Ambient)**		θ_{JA} **(Junction to Case)**
	Blown	**Still**	
D Suffix	50°C/W	85°C/W	15°C/W
F Suffix	55°C/W	90°C/W	15°C/W
P Suffix	50°C/W	85°C/W	15°C/W

PIN ASSIGNMENT


1 A1
2 A2
3 A3
4 A4
5 A5
6 A6
7 A7
8 Gnd
9 D1
10 O1
11 D2
12 NC
24 VCC
23 A0
22 WE
21 CS1
20 OE
19 CS2
18 O4
17 D4
16 O3
15 D3
14 O2
13 NC

MOTOROLA

MCM93415

1024-BIT RANDOM ACCESS MEMORY

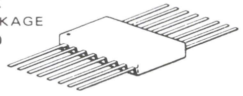
The MCM93415 is a 1024-bit Read/Write RAM organized 1024 words by 1 bit.

The MCM93415 is designed for buffer control storage and high performance main memory applications, and has a typical access time of 35 ns.

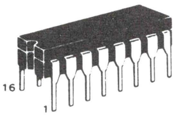
The MCM93415 has full decoding on-chip, separate data input and data output lines, and an active low chip select. The device is fully compatible with standard DTL and TTL logic families and features an uncommitted collector output for ease of memory expansion.

- Uncommitted Collector Output
- TTL Inputs and Output
- Non-Inverting Data Output
- High Speed –
  - Access Time – 35 ns Typical
  - Chip Select – 15 ns Typical
- Power Dissipation Decreases with Increasing Temperature
- Power Dissipation 0.5 mW/Bit Typical
- Organized 1024 Words X 1 Bit

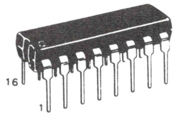
TTL
1024 X 1 BIT
RANDOM ACCESS MEMORY



F SUFFIX
CERAMIC PACKAGE
CASE 650

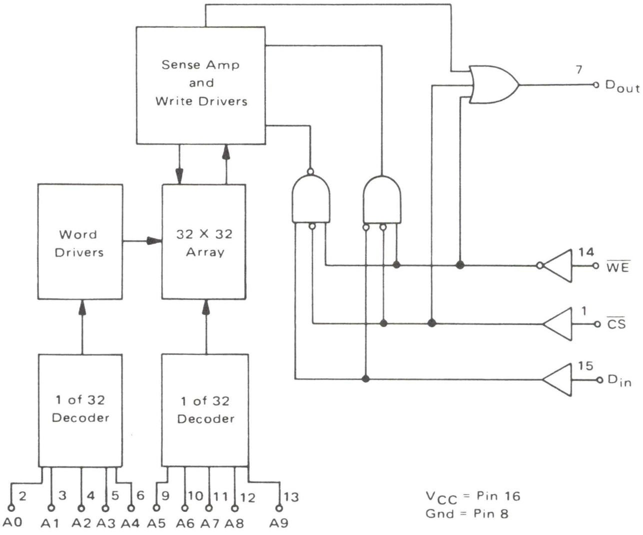


D SUFFIX
CERAMIC PACKAGE
CASE 620



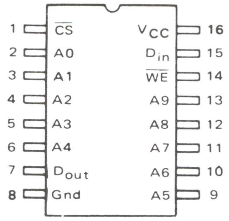
P SUFFIX
PLASTIC PACKAGE
CASE 648

BLOCK DIAGRAM


Sense Amp
and
Write Drivers
Word
Drivers
32 X 32
Array
1 of 32
Decoder
1 of 32
Decoder
7
D_{out}
14
$\overline{WE}$
1
$\overline{CS}$
15
D_{in}
2
3
4
5
6
9
10
11
12
13
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9

V_{CC} = Pin 16
Gnd = Pin 8

PIN ASSIGNMENT


1 $\overline{CS}$
2 A0
3 A1
4 A2
5 A3
6 A4
7 D_{out}
8 Gnd
16 V_{CC}
15 D_{in}
14 $\overline{WE}$
13 A9
12 A8
11 A7
10 A6
9 A5

Pin Designation

$\overline{CS}$	Chip Select
A0 – A9	Address Inputs
$\overline{WE}$	Write Enable
D_{in}	Data Input
D_{out}	Data Output

FUNCTIONAL DESCRIPTION

The MCM93415 is a fully decoded 1024-bit Random Access Memory organized 1024 words by one bit. Bit selection is achieved by means of a 10-bit address, A0 to A9.

The Chip Select input provides for memory array expansion. For large memories, the fast chip select access time permits the decoding of Chip Select ($\overline{CS}$) from the address without affecting system performance.

The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$, Pin 14). With $\overline{WE}$ held low and the chip selected, the data at D_{in} is written into the addressed location. To read, $\overline{WE}$ is held high and the chip selected. Data in the specified location is presented at D_{out} and is non-inverted.

Uncommitted collector outputs are provided to allow wired-OR applications. In any application an external pull-up resistor of R_L value must be used to provide a high at the output when it is off. Any R_L value within the range specified below may be used.

$$\frac{V_{CC}(\text{Min})}{I_{OL} - FO(1.6)} \leq R_L \leq \frac{V_{CC}(\text{Min}) - V_{OH}}{n(I_{CEX}) + FO(0.04)}$$

R_L is in kΩ

n = number of wired-OR outputs tied together

FO = number of TTL Unit Loads (UL) driven

I_{CEX} = Memory Output Leakage Current

V_{OH} = Required Output High Level at Output Node

I_{OL} = Output Low Current

The minimum R_L value is limited by output current sinking ability. The maximum R_L value is determined by the output and input leakage current which must be supplied to hold the output at V_{OH}. One Unit Load = 40 µA High/1.6 mA Low.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature	
Ceramic Package (D and F Suffix)	-55°C to +165°C
Plastic Package (P Suffix)	-55°C to +125°C
Operating Junction Temperature, T_J	
Ceramic Package (D and F Suffix)	< 165°C
Plastic Package (P Suffix)	< 125°C
V_{CC} Pin Potential to Ground Pin	-0.5 V to +7.0 V
Input Voltage (dc)	-0.5 V to +5.5 V
Voltage Applied to Outputs (Output High)	-0.5 V to +5.5 V
Output Current (dc) (Output Low)	+20 mA
Input Current (dc)	-12 mA to +5.0 mA

TRUTH TABLE

Inputs			Output	
$\overline{CS}$	$\overline{WE}$	D_{in}	Open Collector	Mode
H	X	X	H	Not Selected
L	L	L	H	Write "0"
L	L	H	H	Write "1"
L	H	X	D_{out}	Read

H = High Voltage Level
L = Low Voltage Level
X = Don't Care (High or Low)

NOTE 1: Device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

GUARANTEED OPERATING RANGES (Note 2)

	Supply Voltage (V_{CC})			
Part Number	Min	Nom	Max	Ambient Temperature (T_A)
MCM93415DC, PC	4.75 V	5.0 V	5.25 V	0°C to +75°C
MCM93415FM, DM	4.50 V	5.0 V	5.50 V	-55°C to +125°C

DC OPERATING CONDITIONS AND CHARACTERISTICS

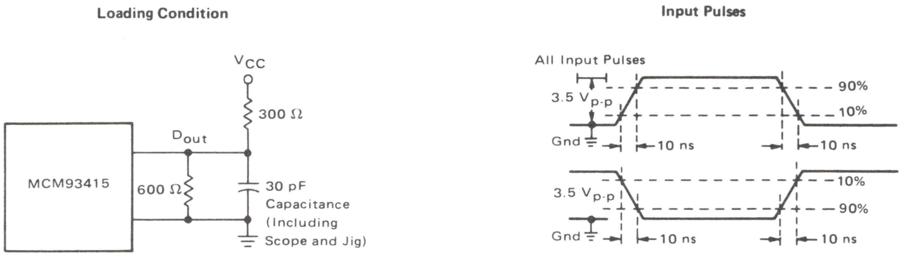
(Full operating voltage and temperature range unless otherwise noted)

		Limits				
Symbol	Characteristic	Min	Max	Unit	Conditions	
V_{OL}	Output Low Voltage		0.45	Vdc	V_{CC} = Min, I_{OL} = 16 mA	
V_{IH}	Input High Voltage	2.1		Vdc	Guaranteed Input High Voltage for All Inputs	
V_{IL}	Input Low Voltage		0.8	Vdc	Guaranteed Input Low Voltage for All Inputs	
I_{IL}	Input Low Current		-400	µAdc	V_{CC} = Max, V_{in} = 0.4 V	
I_{IH}	Input High Current		40	µAdc	V_{CC} = Max, V_{in} = 4.5 V	
			1.0	mAdc	V_{CC} = Max, V_{in} = 5.25 V	
I_{CEX}	Output Leakage Current		100	µAdc	V_{CC} = Max, V_{out} = 4.5 V	
V_{CD}	Input Diode Clamp Voltage		-1.5	Vdc	V_{CC} = Max, I_{in} = -10 mA	
I_{CC}	Power Supply Current		130	mAdc	T_A = Max	V_{CC} = Max, All Inputs Grounded
			155	mAdc	T_A = 0°C	
			170	mAdc	T_A = Min	

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted)

AC TEST LOAD AND WAVEFORM



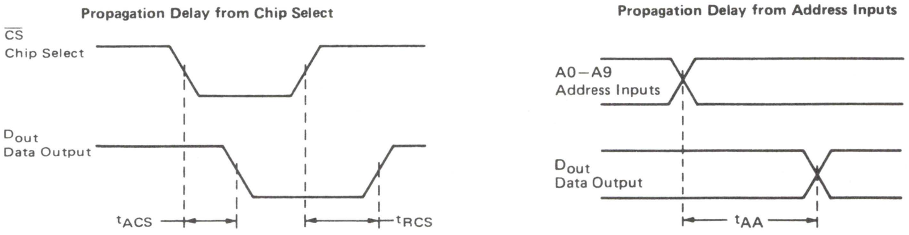
Loading Condition

Input Pulses

VCC
300 Ω
Dout
MCM93415
600 Ω
30 pF
Capacitance
(Including
Scope and Jig)
All Input Pulses
3.5 Vp-p
Gnd
90%
10%
10 ns
10 ns
3.5 Vp-p
Gnd
10%
90%
10 ns
10 ns

Symbol	Characteristic (Notes 2, 3)	MCM93415DC, PC		MCM93415DM, FM		Unit	Conditions
		Min	Max	Min	Max		
READ MODE	DELAY TIMES					ns	
t_{ACS}	Chip Select Time		35		45		See Test Circuit and Waveforms
t_{RCS}	Chip Select Recovery Time		35		50		
t_{AA}	Address Access Time		45		60		
WRITE MODE	DELAY TIMES					ns	
t_{WS}	Write Disable Time		35		45		See Test Circuit and Waveforms
t_{WR}	Write Recovery Time		40		50		
	INPUT TIMING REQUIREMENTS					ns	
t_W	Write Pulse Width (to guarantee write)	30		40			See Test Circuit and Waveforms
t_{WSD}	Data Setup Time Prior to Write	5		5			
t_{WHD}	Data Hold Time After Write	5		5			
t_{WSA}	Address Setup Time (at t_W = Min)	10		15			
t_{WHA}	Address Hold Time	10		10			
t_{WSCS}	Chip Select Setup Time	5		5			
t_{WHCS}	Chip Select Hold Time	5		5			

READ OPERATION TIMING DIAGRAM



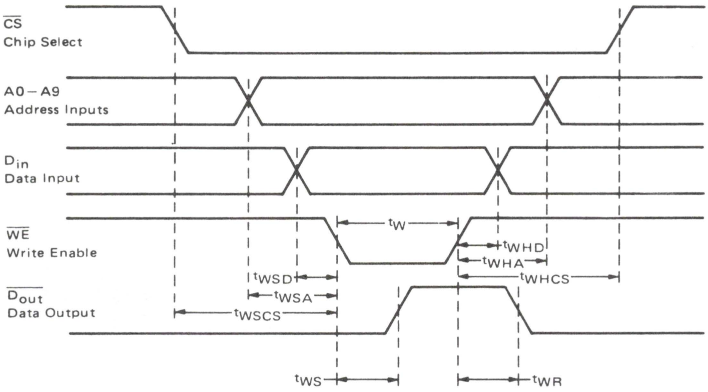
Propagation Delay from Chip Select

Propagation Delay from Address Inputs

$\overline{CS}$
Chip Select
Dout
Data Output
tACS
tRCS
A0–A9
Address Inputs
Dout
Data Output
tAA

(All Time Measurements Referenced to 1.5 V)

WRITE CYCLE TIMING


CS
Chip Select
A0 – A9
Address Inputs
D_{in}
Data Input
WE
Write Enable
D_{out}
Data Output
t_W
t_{WHD}
t_{WHA}
t_{WHCS}
t_{WSD}
t_{WSA}
t_{WSCS}
t_{WS}
t_{WR}

(All Time Measurements Referenced to 1.5 V)

NOTE 2: DC and AC specifications limits guaranteed with 500 linear feet per minute blown air. Contact your Motorola Sales Representative if extended temperature or modified operating conditions are desired.

Package	θ_{JA} (Junction to Ambient)		θ_{JC} (Junction to Case)
	Blown	Still	
D Suffix	50°C/W	85°C/W	15°C/W
F Suffix	55°C/W	90°C/W	15°C/W
P Suffix	65°C/W	100°C/W	25°C/W

NOTE 3: The AC limits are guaranteed to be the worst case bit in the memory.

MOTOROLA

MCM93425

1024-BIT RANDOM ACCESS MEMORY

The MCM93425 is a 1024-bit Read/Write RAM, organized 1024 words by 1 bit.

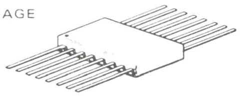
The MCM93425 is designed for high performance main memory and control storage applications and has a typical address time of 35 ns.

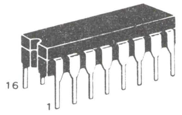
The MCM93425 has full decoding on-chip, separate data input and data output lines, and an active low-chip select and write enable. The device is fully compatible with standard DTL and TTL logic families. A three-state output is provided to drive bus-organized systems and/or highly capacitive loads.

- Three-State Output
- TTL Inputs and Output
- Non-Inverting Data Output
- High Speed —
  - Access Time — 35 ns Typical
  - Chip Select — 15 ns Typical
- Power Dissipation — 0.5 mW/Bit Typical
- Power Dissipation Decreases With Increasing Temperature

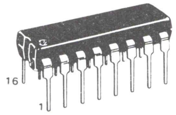
TTL
1024 X 1 BIT
RANDOM ACCESS MEMORY

F SUFFIX
CERAMIC PACKAGE
CASE 650



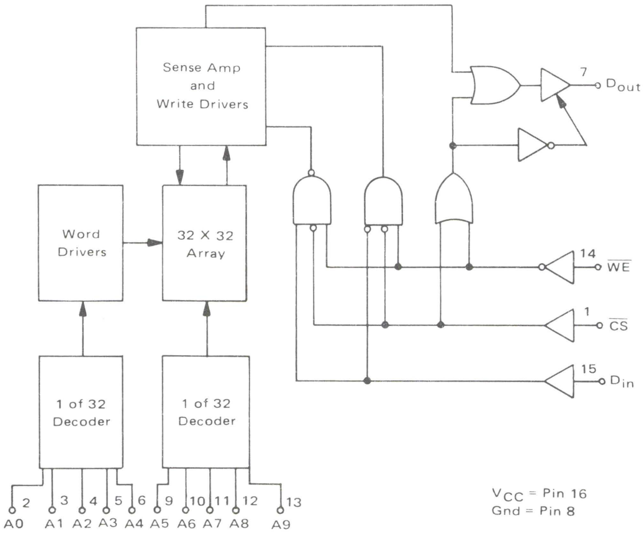


D SUFFIX
CERAMIC PACKAGE
CASE 620



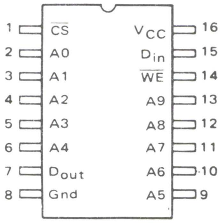
P SUFFIX
PLASTIC PACKAGE
CASE 648

BLOCK DIAGRAM


Sense Amp and Write Drivers
Word Drivers
32 X 32 Array
1 of 32 Decoder
1 of 32 Decoder
7
D_{out}
14
$\overline{WE}$
1
$\overline{CS}$
15
D_{in}
2
3
4
5
6
9
10
11
12
13
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
V_{CC} = Pin 16
Gnd = Pin 8

NOTE: Logic driving sense amp/write drivers depicts negative-only write used on C4m.

PIN ASSIGNMENT


1 $\overline{CS}$
2 A0
3 A1
4 A2
5 A3
6 A4
7 D_{out}
8 Gnd
16 V_{CC}
15 D_{in}
14 $\overline{WE}$
13 A9
12 A8
11 A7
10 A6
9 A5

Pin Description

$\overline{CS}$	Chip Select
A0 - A9	Address Inputs
$\overline{WE}$	Write Enable
D_{in}	Data Input
D_{out}	Data Output

FUNCTIONAL DESCRIPTION

The MCM93425 is a fully decoded 1024-bit Random Access Memory organized 1024 words by one bit. Word selection is achieved by means of a 10-bit address, A0–A9.

The Chip Select ($\overline{\text{CS}}$) input provides for memory array expansion. For large memories, the fast chip select time permits the decoding of chip select from the address without increasing address access time.

The read and write operations are controlled by the state of the active low Write Enable ($\overline{\text{WE}}$, Pin 14). With $\overline{\text{WE}}$ and $\overline{\text{CS}}$ held low, the data at D_{in} is written into the addressed location. To read, $\overline{\text{WE}}$ is held high and $\overline{\text{CS}}$ held low. Data in the specified location is presented at D_{out} and is non-inverted.

The three-state output provides drive capability for higher speeds with capacitive load systems. The third state (high impedance) allows bus organized systems where multiple outputs are connected to a common bus.

During writing, the output is held in the high-impedance state.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature Ceramic Package (D and F Suffix) Plastic Package (P Suffix)	 -55°C to +165°C -55°C to +125°C
Operating Junction Temperature, T_J Ceramic Package (D and F Suffix) Plastic Package (P Suffix)	 < 165°C < 125°C
V_{CC} Pin Potential to Ground Pin	-0.5 V to +7.0 V
Input Voltage (dc)	-0.5 V to +5.5 V
Voltage Applied to Outputs (Output High)	-0.5 V to +5.5 V
Output Current (dc) (Output Low)	+20 mA
Input Current (dc)	-12 mA to +5.0 mA

NOTE 1: Device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

TRUTH TABLE

Inputs			Output	
$\overline{\text{CS}}$	$\overline{\text{WE}}$	D_{in}	D_{out}	Mode
H	X	X	High Z	Not Selected
L	L	L	High Z	Write "0"
L	L	H	High Z	Write "1"
L	H	X	D_{out}	Read

H = High Voltage Level
L = Low Voltage Level
X = Don't Care (High or Low)

GUARANTEED OPERATING RANGES (Notes 2 and 3)

Part Number	Supply Voltage (V_{CC}) Min	Nom	Max	Ambient Temperature (T_A)
MCM93425DC, PC	4.75 V	5.0 V	5.25 V	0°C to +75°C
MCM93425FM, DM	4.50 V	5.0 V	5.50 V	-55°C to +125°C

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

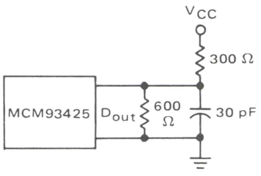
Symbol	Characteristic		Limits Min	Max	Units	Conditions	
V_{OL}	Output Low Voltage			0.45	Vdc	V_{CC} = Min, I_{OL} = 16 mA	
V_{IH}	Input High Voltage		2.1		Vdc	Guaranteed Input High Voltage for all Inputs	
V_{IL}	Input Low Voltage			0.8	Vdc	Guaranteed Input Low Voltage for all Inputs	
I_{IL}	Input Low Current			-400	µAdc	V_{CC} = Max, V_{in} = 0.4 V	
I_{IH}	Input High Current			40	µAdc	V_{CC} = Max, V_{in} = 4.5 V	
				1.0	mAdc	V_{CC} = Max, V_{in} = 5.25 V	
I_{off}	Output Current (High Z)			50	µAdc	V_{CC} = Max, V_{out} = 2.4 V	
				-50		V_{CC} = Max, V_{out} = 0.5 V	
I_{OS}	Output Current Short Circuit to Ground			-100	mAdc	V_{CC} = Max	
V_{OH}	Output High Voltage	MCM93425DC, PC	2.4		Vdc	I_{OH} = -10.3 mA, V_{CC} = 5.0 V ± 5%	
		MCM93425FM, DM	2.4		Vdc	I_{OH} = -5.2 mA	
V_{CD}	Input Diode Clamp Voltage			-1.5	Vdc	V_{CC} = Max, I_{in} = -10 mA	
I_{CC}	Power Supply Current			130	mAdc	T_A = Max	V_{CC} = Max, All Inputs Grounded
				155	mAdc	T_A = 0°C	
				170	mAdc	T_A = Min	

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted)

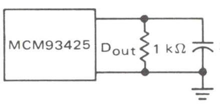
AC TEST LOAD AND WAVEFORMS

Loading Conditions



V_{CC}
300 Ω
MCM93425
D_{out}
600 Ω
30 pF

Load A

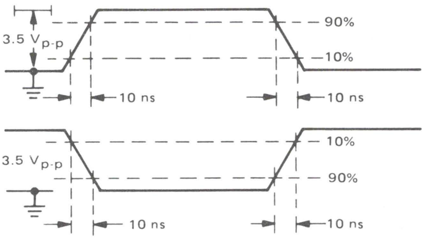


MCM93425
D_{out}
1 kΩ
30 pF

Load B

Input Pulses

All Input Pulses

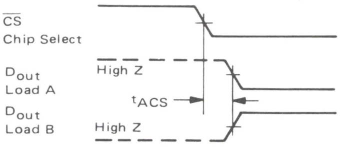


3.5 $V_{p\text{-}p}$
90%
10%
10 ns
10 ns
3.5 $V_{p\text{-}p}$
10%
90%
10 ns
10 ns

Symbol	Characteristic (Notes 2, 4)	MCM93425DC, PC		MCM93425DM, FM		Units	Conditions
		Min	Max	Min	Max		
READ MODE	DELAY TIMES					ns	
t_{ACS}	Chip Select Time		35		45		See Test Circuit and Waveforms
t_{ZRCS}	Chip Select to High Z		35		50		
t_{AA}	Address Access Time		45		60		
WRITE MODE	DELAY TIMES					ns	
t_{ZWS}	Write Disable to High Z		35		45		See Test Circuit and Waveforms
t_{WR}	Write Recovery Time		40		50		
	INPUT TIMING REQUIREMENTS					ns	
t_W	Write Pulse Width (to guarantee write)	30		40			See Test Circuit and Waveforms
t_{WSD}	Data Setup Time Prior to Write	5		5			
t_{WHD}	Data Hold Time After Write	5		5			
t_{WSA}	Address Setup Time (at t_W = Min)	10		15			
t_{WHA}	Address Hold Time	10		10			
t_{WSCS}	Chip Select Setup Time	5		5			
t_{WHCS}	Chip Select Hold Time	5		5			

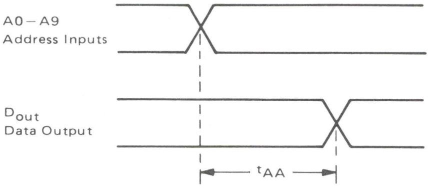
READ OPERATION TIMING DIAGRAM

Propagation Delay from Chip Select



$\overline{CS}$
Chip Select
D_{out}
Load A
D_{out}
Load B
High Z
t_{ACS}
High Z

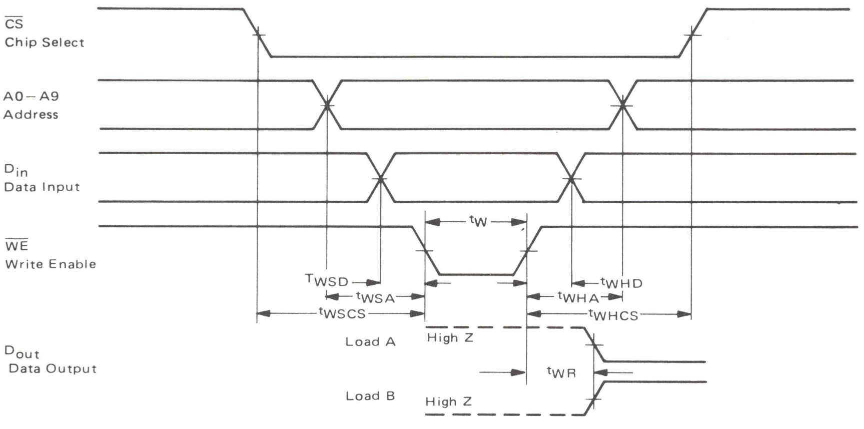
Propagation Delay from Address Inut



A0 – A9
Address Inputs
D_{out}
Data Output
t_{AA}

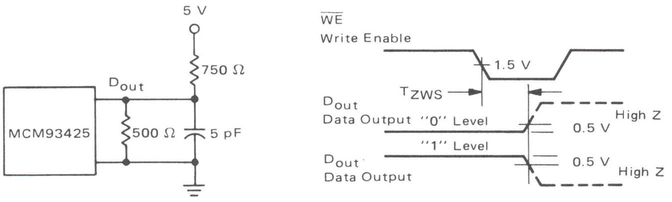
(All time measurements referenced to 1.5 V)

WRITE CYCLE TIMING


CS
Chip Select
A0 – A9
Address
Din
Data Input
WE
Write Enable
tW
TWSD
tWSA
tWSCS
tWHD
tWHA
tWHCS
Dout
Data Output
Load A
High Z
tWR
Load B
High Z

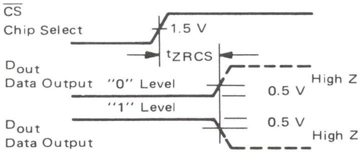
(All above measurements reference to 1.5 V)

WRITE ENABLE TO HIGH Z DELAY


5 V
750 Ω
Dout
MCM93425
500 Ω
5 pF
WE
Write Enable
1.5 V
TZWS
Dout
Data Output "0" Level
"1" Level
0.5 V
High Z
Dout
Data Output
0.5 V
High Z

Load C

Propagation Delay from Chip Select to High Z


CS
Chip Select
1.5 V
tZRCS
Dout
Data Output "0" Level
"1" Level
0.5 V
High Z
Dout
Data Output
0.5 V
High Z

(All t_{ZXXX} parameters are measured at a delta of 0.5 V from the logic level and using Load C)

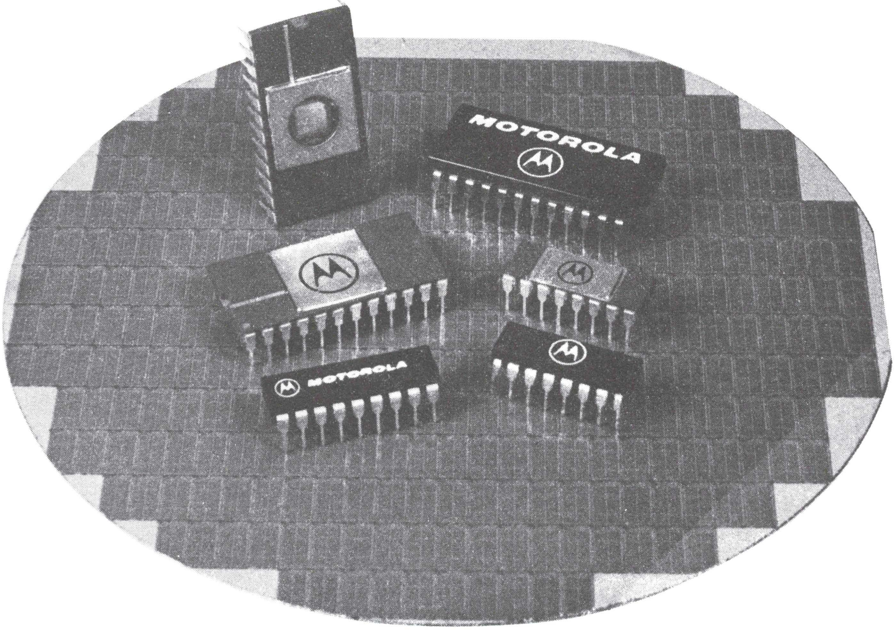
NOTE 2: DC and AC specifications limits guaranteed with 500 linear feet per minute blown air. Contact your Motorola Sales Representative if extended temperature or modified operating conditions are desired.

Package	θ_{JA} (Junction to Ambient)		θ_{JC} (Junction to Case)
	Blown	**Still**	
D Suffix	50°C/W	85°C/W	15°C/W
F Suffix	55°C/W	90°C/W	15°C/W
P Suffix	65°C/W	100°C/W	25°C/W

NOTE 3: Output short circuit conditions must not exceed 1 second duration.

NOTE 4: The maximum address access time is guaranteed to be the worst case bit in the memory.

TTL PROM


MOTOROLA
MOTOROLA

MOTOROLA

MCM7621
MCM7620

2048-BIT PROGRAMMABLE READ ONLY MEMORY

The MCM7620/MCM7621 have common dc electrical characteristics and identical programming requirements. They are fully decoded, high-speed, field-programmable ROMs and are available with open-collector or three-state outputs. All bits are manufactured storing a logical "1" (outputs high), and can be selectively programmed for logical "0" (outputs low).

The field-programmable PROM can be custom programmed to any pattern using a simple programming procedure. Schottky bipolar circuitry provides fast access time, and features temperature and voltage compensation to minimize access time variations.

All pinouts are compatible to industry-standard PROMs and ROMs.

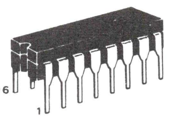
In addition to the conventional storage array, extra test rows and columns are included to assure high programmability, and guarantee parametric and ac performance. Fuses in these test rows and columns are blown prior to shipment.

- Common dc Electrical Characteristics and Programming Procedure
- Simple, High-Speed Programming Procedure (0.1 Second per 1024 Bits, Typical)
- Expandable – Open-Collector or Three-State Outputs and Chip Enable Inputs
- Inputs and Outputs TTL-Compatible
  Low Input Current – 250 μA Logic "0", 40 μA Logic "1"
  Full Output Drive – 16 mA Sink, 2.0 mA Source
- Fast Access Time – Guaranteed for Worst-Case N^2 Sequencing, Over Commercial and Military Temperature and Voltage Ranges
- Pin-Compatible with Industry-Standard PROMs and ROMs

MTTL

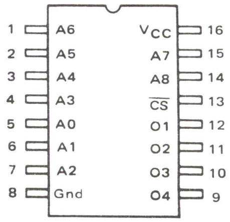
2048-BIT PROGRAMMABLE READ ONLY MEMORIES

MCM7620 – 512 × 4 – Open-Collector
MCM7621 – 512 × 4 – Three-State



L SUFFIX
CERAMIC PACKAGE
CASE 620

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Supply Voltage (operating)	V_{CC}	+7.0	Vdc
Input Voltage	V_{in}	+5.5	Vdc
Output Voltage (operating)	V_{OH}	+7.0	Vdc
Supply Current	I_{CC}	650	mAdc
Input Current	I_{in}	-20	mAdc
Output Sink Current	I_o	100	mAdc
Operating Temperature Range MCM76xxDM MCM76xxDC	T_A	 -55 to +125 0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C
Maximum Junction Temperature	T_J	+175	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability. (While programming, follow the programming specifications.)

DC OPERATING CONDITIONS AND CHARACTERISTICS

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}				Vdc
MCM76xxDM		4.50	5.0	5.50	
MCM76xxDC		4.75	5.0	5.25	
Input High Voltage	V_{IH}	2.0	–	–	Vdc
Input Low Voltage	V_{IL}	–	–	0.8	Vdc

DC CHARACTERISTICS

			Open-Collector Output			Three-State Output			
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{RA}, I_{RE}	Address/Enable "1"	$V_{IH} = V_{CC}$ Max	–	–	40	–	–	40	μAdc
I_{FA}, I_{FE}	Input Current "0"	$V_{IL} = 0.45$ V	–	-0.1	-0.25	–	-0.1	-0.25	mAdc
V_{OH}	Output Voltage "1"	$I_{OH} = -2.0$ mA, $V_{CC} = V_{CC}$ Min	N/A	–	–	2.4	3.4	–	Vdc
V_{OL}	"0"	$I_{OL} = +16$ mA, $V_{CC} = V_{CC}$ Min	–	0.35	0.45	–	0.35	0.45	Vdc
I_{OHE}	Output Disabled "1"	V_{OH}, $V_{CC} = V_{CC}$ Max	–	–	100	–	–	100	μAdc
I_{OLE}	Current "0"	$V_{OL} = +0.3$ V, $V_{CC} = V_{CC}$ Max	–	–	N/A	–	–	-100	μAdc
I_{OH}	Output Leakage "1"	V_{OH}, $V_{CC} = V_{CC}$ Max	–	–	100	–	–	N/A	μAdc
V_{CL}	Input Clamp Voltage	$I_{in} = -10$ mA	–	–	-1.5	–	–	-1.5	Vdc
I_{OS}	Output Short Circuit Current	$V_{CC} = V_{CC}$ Max, $V_{out} = 0.0$ V One Output Only for 1 s Max	N/A	–	N/A	15	–	70	mAdc
I_{CC}	Power Supply Current MCM7620/MCM7621	$V_{CC} = V_{CC}$ Max All Inputs Grounded	–	60	100	–	60	100	mAdc

CAPACITANCE (f = 1.0 MHz, $T_A = 25^{o}$C, periodically sampled rather than 100% tested.)

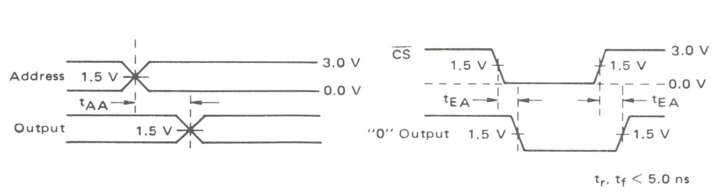
Characteristic	Symbol	Typ	Unit
Input Capacitance	C_{in}	8.0	pF
Output Capacitance	C_{out}	8.0	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

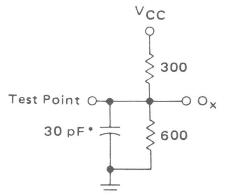
(Full operating voltage and temperature unless otherwise noted)

		0 to +70°C		-55 to +125°C		
Characteristic	**Symbol**	**Typ**	**Max**	**Typ**	**Max**	**Unit**
Address to Output Access Time	t_{AA}	45	70	45	85	ns
Chip Enable Access Time MCM7620/7621	t_{EA}	15	25	15	30	ns

TIMING DIAGRAM



AC TEST LOAD



*Includes Jig Capacitance

PROGRAMMING

The PROMs are manufactured with all bits/outputs Logical "1" (Output High). Any desired bit/output can be programmed to a Logical "0" (Output Low) by following the simple procedure shown below. One may build his own programmer to satisfy the sepcifications described in Table 1, or buy any of the commercially available programmers which meet these specifications. These PROMs can be programmed automatically or by the manual procedure shown below.

PROGRAMMING PROCEDURE

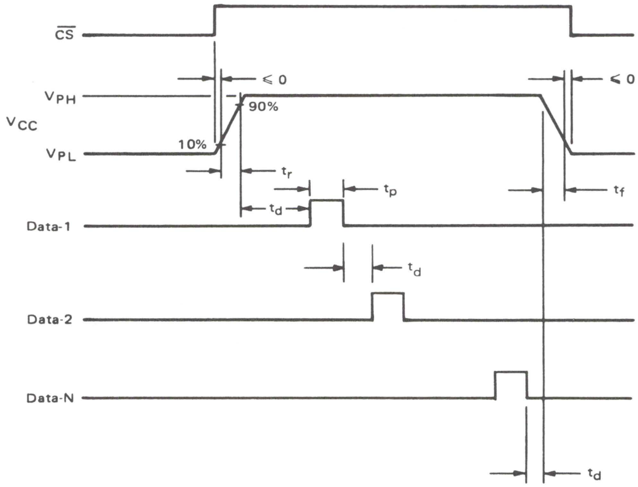
1. Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL-compatible. An open circuit should not be used to address the PROM.
2. Disable the chip by applying input highs (V_{IH}) to the $\overline{CS}$ input. The chip select is TTL-compatible. An open circuit should not be used to disable the chip.
3. Disable the programming circuitry by applying an Output Voltage Disable of less than V_{OPD} to the output of the PROM. The output may be left open to achieve the disable.
4. Raise V_{CC} to V_{PH} with rise time equal to t_r.
5. After a delay equal to or greater than t_d, apply a pulse with amplitude of V_{OPE} and duration of t_p to the output selected for programming. Note that the PROM is supplied with fuses intact generating an output high. Programming a fuse will cause the output to go low in the verify mode.
6. Other bits in the same word may be programmed while the V_{CC} input is raised to V_{PH} by applying output enable pulses to each output which is to be programmed. The output enable pulses must be separated by a minimum interval of t_d.
7. Lower V_{CC} to 4.5 Volts following a delay of t_d from the last programming enable pulse applied to an output.
8. Enable the PROM for verification by applying a logic "0" (V_{IL}) to the $\overline{CS}$ input.
9. If any bit does not verify as programmed, repeat Steps 2 through 8 until the bit has received a total of 1.0 ms of programming time. Bits which do not program within 1.0 ms may be considered programming rejects. Multiple pulses of durations shorter than 1.0 ms may be used to enhance programming speed.
10. Repeat Steps 1 through 9 for all other bits to be programmed in the PROM.
11. Programming rejects returned to the factory must be accompanied by data giving address with desired and actual output data of a location in which a programming failure has occurred.

TABLE 1
PROGRAMMING SPECIFICATIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{IH}	Address Input	2.4	5.0	5.0	V
V_{IL}	Voltage(1)	0.0	0.4	0.8	V
V_{PH}	Programming/Verify	11.75	12.0	12.25	V
V_{PL}	Voltage to V_{CC}	4.5	4.5	5.5	V
I_{CCP}	Programming Voltage Current Limit	600	600	650	mA
	Programming (V_{CC})				
t_r	Voltage Rise and	1	1	10	µs
t_f	Fall Time	1	1	10	µs
t_d	Programming Delay	10	10	100	µs
t_p	Programming Pulse Width	100	–	1000	µs
DC	Programming Duty Cycle	–	50	90	%
	Output Voltage				
V_{OPE}	Enable	10.0	10.5	11.0	V
V_{OPD}	Disable(2)	4.5	5.0	5.5	V
I_{OPE}	Output Voltage Enable Current	2	4	10	mA
T_C	Case Temperature	–	25	75	°C

(1) Address and chip select should not be left open for V_{IH}.
(2) Disable condition will be met with output open circuit.

FIGURE 1 – TYPICAL PROGRAMMING WAVEFORMS


$\overline{CS}$
≤ 0
≤ 0
V_{PH}
V_{CC}
V_{PL}
90%
10%
t_r
t_p
t_f
t_d
Data-1
t_d
Data-2
Data-N
t_d

MOTOROLA

MCM7640
thru
MCM7643

MTTL

4096-BIT PROGRAMMABLE READ ONLY MEMORIES

MCM7640 – 512 x 8 – Open-Collector
MCM7641 – 512 x 8 – Three-State
MCM7642 – 1024 x 4 – Open-Collector
MCM7643 – 1024 x 4 – Three-State

TTL PROM

4096-BIT PROGRAMMABLE READ ONLY MEMORY

The MCM7640 through 43 PROMs comprise a completely compatible family having common dc electrical characteristics and identical programming requirements. They are fully-decoded, high-speed, field-programmable ROMs and are available in commonly used organizations, with both open-collector and three-state outputs. All bits are manufactured storing a logical "1" (outputs high), and can be selectively programmed for logical "0" (outputs low).

The field-programmable PROM can be custom programmed to any pattern using a simple programming procedure. Schottky bipolar circuitry provides fast access time, and features temperature and voltage compensation to minimize access time variations.

All pinouts are compatible to industry-standard PROMs and ROMs.

In addition to the conventional storage array, extra test rows and columns are included to assure high programmability, and guarantee parametric and ac performance. Fuses in these test rows and columns are blown prior to shipment.

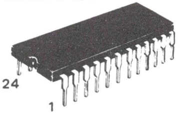
- Common dc Electrical Characteristics and Programming Procedure
- Simple, High-Speed Programming Procedure (1 Second per 1024 Bits, Typical)
- Expandable – Open-Collector or Three-State Outputs and Chip Enable Inputs
- Inputs and Outputs TTL-Compatible
  Low Input Current – 250 μA Logic "0", 40 μA Logic "1"
  Full Output Drive – 16 mA Sink, 2.0 mA Source
- Fast Access Time – Guaranteed for Worst-Case N^2 Sequencing, Over Commercial and Military Temperature and Voltage Ranges
- Pin-Compatible with Industry-Standard PROMs and ROMs

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Supply Voltage (operating)	V_{CC}	+7.0	Vdc
Input Voltage	V_{in}	+5.5	Vdc
Output Voltage (operating)	V_{OH}	+7.0	Vdc
Supply Current	I_{CC}	650	mAdc
Input Current	I_{in}	-20	mAdc
Output Sink Current	I_o	100	mAdc
Operating Temperature Range MCM76xxDM MCM76xxDC	T_A	 -55 to +125 0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C
Maximum Junction Temperature	T_J	+175	°C

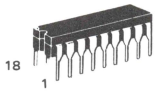
NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability. (While programming, follow the programming specifications.)

MCM7640/41



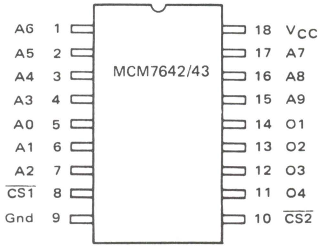
D SUFFIX
CERAMIC PACKAGE

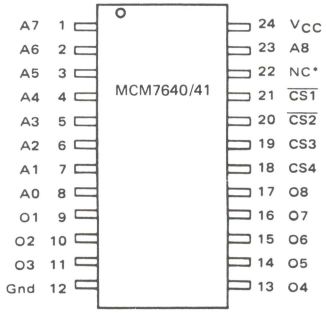
MCM7642/43



D SUFFIX
CERAMIC PACKAGE

PIN ASSIGNMENT





*No Connection

DC OPERATING CONDITIONS AND CHARACTERISTICS

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}				Vdc
MCM76xxDM		4.50	5.0	5.50	
MCM76xxDC		4.75	5.0	5.25	
Input High Voltage	V_{IH}	2.0	–	–	Vdc
Input Low Voltage	V_{IL}	–	–	0.8	Vdc

DC CHARACTERISTICS

			Open-Collector Output			Three-State Output			
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{RA}, I_{RE}	Address/Enable "1"	$V_{IH} = V_{CC}$ Max	–	–	40	–	–	40	μAdc
I_{FA}, I_{FE}	Input Current "0"	$V_{IL} = 0.45$ V	–	-0.1	-0.25	–	-0.1	-0.25	mAdc
V_{OH}	Output Voltage "1"	$I_{OH} = -2.0$ mA, $V_{CC} = V_{CC}$ Min	N/A	–	–	2.4	3.4	–	Vdc
V_{OL}	"0"	$I_{OL} = +16$ mA, $V_{CC} = V_{CC}$ Min	–	0.35	0.45	–	0.35	0.45	Vdc
I_{OHE}	Output Disabled "1"	V_{OH}, $V_{CC} = V_{CC}$ Max	–	–	100	–	–	100	μAdc
I_{OLE}	Current "0"	$V_{OL} = +0.3$ V, $V_{CC} = V_{CC}$ Max	–	–	N/A	–	–	-100	μAdc
I_{OH}	Output Leakage "1"	V_{OH}, $V_{CC} = V_{CC}$ Max	–	–	100	–	–	N/A	μAdc
V_{CL}	Input Clamp Voltage	$I_{in} = -10$ mA	–	–	-1.5	–	–	-1.5	Vdc
I_{OS}	Output Short Circuit Current	$V_{CC} = V_{CC}$ Max, $V_{out} = 0.0$ V One Output Only for 1 s Max	N/A	–	N/A	15	–	70	mAdc
I_{CC}	Power Supply Current	$V_{CC} = V_{CC}$ Max All Inputs Grounded							
	MCM7640/MCM7641		–	100	140	–	100	140	mAdc
	MCM1642/MCM7643		–	100	140	–	100	140	mAdc

CAPACITANCE (f = 1.0 MHz, $T_A = 25^{\circ}$C, periodically sampled rather than 100% tested.)

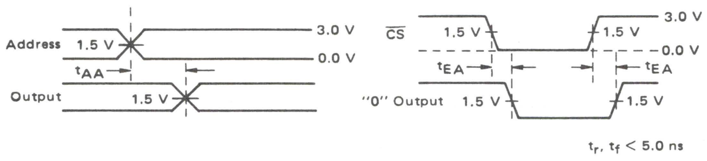
Characteristic	Symbol	Typ	Unit
Input Capacitance	C_{in}	8.0	pF
Output Capacitance	C_{out}	8.0	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

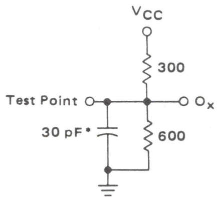
(Full operating voltage and temperature unless otherwise noted)

		0 to +70°C		-55 to +125°C		
Characteristic	**Symbol**	**Typ**	**Max**	**Typ**	**Max**	**Unit**
Address to Output Access Time	t_{AA}	45	70	45	85	ns
Chip Enable Access Time	t_{EA}					ns
MCM7640/7641		30	40	30	50	
MCM7642/7643		15	25	15	30	

TIMING DIAGRAM



AC TEST LOAD



*Includes Jig Capacitance

PROGRAMMING

The PROMs are manufactured with all bits/outputs Logical "1" (Output High). Any desired bit/output can be programmed to a Logical "0" (Output Low) by following the simple procedure shown below. One may build his own programmer to satisfy the sepcifications described in Table 1, or buy any of the commercially available programmers which meet these specifications. These PROMs can be programmed automatically or by the manual procedure shown below.

PROGRAMMING PROCEDURE

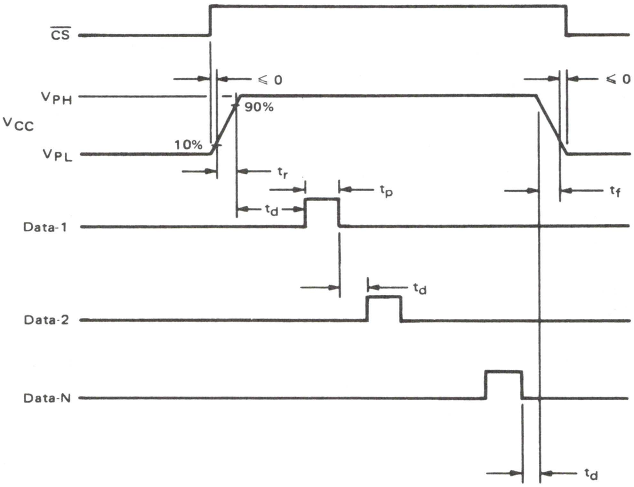
1. Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL-compatible. An open circuit should not be used to address the PROM.
2. Disable the chip by applying input highs (V_{IH}) to the $\overline{CS}$ input(s). CS inputs (MCM7640/41 only) must remain at V_{IH} for program and verify. The chip select is TTL-compatible. An open circuit should not be used to disable the chip.
3. Disable the programming circuitry by applying an Output Voltage Disable of less than V_{OPD} to the output of the PROM. The output may be left open to achieve the disable.
4. Raise V_{CC} to V_{PH} with rise time equal to t_r.
5. After a delay equal to or greater than t_d, apply a pulse with amplitude of V_{OPE} and duration of t_p to the output selected for programming. Note that the PROM is supplied with fuses intact generating an output high. Programming a fuse will cause the output to go low in the verify mode.
6. Other bits in the same word may be programmed while the V_{CC} input is raised to V_{PH} by applying output enable pulses to each output which is to be programmed. The output enable pulses must be separated by a minimum interval of t_d.
7. Lower V_{CC} to 4.5 Volts following a delay of t_d from the last programming enable pulse applied to an output.
8. Enable the PROM for verification by applying a logic "0" (V_{IL}) to the $\overline{CS}$ input(s).
9. If any bit does not verify as programmed, repeat Steps 2 through 8 until the bit has received a total of 1.0 ms of programming time. Bits which do not program within 1.0 ms may be considered programming rejects. Multiple pulses of durations shorter than 1.0 ms may be used to enhance programming speed.
10. Repeat Steps 1 through 9 for all other bits to be programmed in the PROM.
11. Programming rejects returned to the factory must be accompanied by data giving address with desired and actual output data of a location in which a programming failure has occurred.

TABLE 1
PROGRAMMING SPECIFICATIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{IH}	Address Input	2.4	5.0	5.0	V
V_{IL}	Voltage(1)	0.0	0.4	0.8	V
V_{PH}	Programming/Verify	11.75	12.0	12.25	V
V_{PL}	Voltage to V_{CC}	4.5	4.5	5.5	V
I_{CCP}	Programming Voltage Current Limit	600	600	650	mA
	Programming (V_{CC})				
t_r	Voltage Rise and	1	1	10	µs
t_f	Fall Time	1	1	10	µs
t_d	Programming Delay	10	10	100	µs
t_p	Programming Pulse Width	100	–	1000	µs
DC	Programming Duty Cycle	–	50	90	%
	Output Voltage				
V_{OPE}	Enable	10.0	10.5	11.0	V
V_{OPD}	Disable(2)	4.5	5.0	5.5	V
I_{OPE}	Output Voltage Enable Current	2	4	10	mA
T_C	Case Temperature	–	25	75	°C

(1) Address and chip select should not be left open for V_{IH}.
(2) Disable condition will be met with output open circuit.

FIGURE 1 – TYPICAL PROGRAMMING WAVEFORMS



$\overline{CS}$
≤ 0
≤ 0
V_{PH}
90%
V_{CC}
10%
V_{PL}
t_r
t_p
t_f
t_d
Data-1
t_d
Data-2
Data-N
t_d

MOTOROLA

MCM7680
MCM7681

MTTL

8192-BIT PROGRAMMABLE READ ONLY MEMORIES

MCM7680 – 1024 × 8 – Open-Collector
MCM7681 – 1024 × 8 – Three-State

8192-BIT PROGRAMMABLE READ ONLY MEMORY

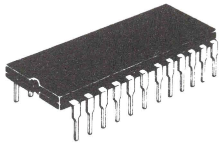
The MCM7680/81 together with the MCM7620/21, MCM7640/43 comprise a complete, compatible family having common dc electrical characteristics and identical programming requirements. They are fully decoded, high-speed, field-programmable ROMs and are available in commonly used organizations, with both open-collector and three-state outputs. All bits are manufactured storing a logical "1" (outputs high), and can be selectively programmed for logical "0" (outputs low).

The field-programmable PROM can be custom-programmed to any pattern using a simple programming procedure. Schottky bipolar circuitry provides fast access time, and features temperature and voltage compensation to minimize access time variations.

Pinouts are compatible to industry-standard PROMs and ROMs. In addition, the MCM7680 and 81 are pin compatible replacement for the 512 × 8 with pin 2 connected as A9 on the 1024 × 8.

In addition to the conventional storage array, extra test rows and columns are included to assure high programmability, and guarantee parametric and ac performance. Fuses in these test rows and columns are blown prior to shipment.

- Common dc Electrical Characteristics and Programming Procedure
- Simple, High-Speed Programming Procedure (0.1 second per 1024 Bits, Typical)
- Expandable – Open-Collector or Three-State Outputs and Chip Enable Inputs
- Inputs and Outputs TTL-Compatible
  Low Input Current – 250 μA Logic "0", 40 μA Logic "1"
  Full Output Drive – 16 mA Sink, 2.0 mA Source
- Fast Access Time – Guaranteed for Worst-Case N^2 Sequencing, Over Commercial and Military Temperature Ranges
- Pin-Compatible with Industry-Standard PROMs and ROMs



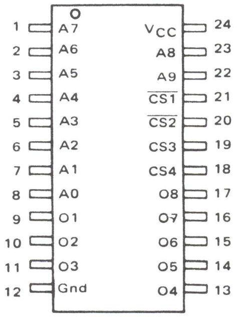
CERAMIC PACKAGE
CASE 623

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Supply Voltage (operating)	V_{CC}	+7.0	Vdc
Input Voltage	V_{in}	+5.5	Vdc
Output Voltage (operating)	V_{OH}	+7.0	Vdc
Supply Current	I_{CC}	650	mAdc
Input Current	I_{in}	-20	mAdc
Output Sink Current	I_O	100	mAdc
Operating Temperature Range	T_A		°C
MCM76xxDM		-55 to +125	
MCM76xxDC		0 to +70	
Storage Temperature Range	T_{stg}	-55 to +150	°C
Maximum Junction Temperature	T_J	+175	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability. (While programming, follow the programming specifications.)

PIN ASSIGNMENT



DC OPERATING CONDITIONS AND CHARACTERISTICS

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage MCM76xxDM MCM76xxDC	V_{CC}	 4.50 4.75	 5.0 5.0	 5.50 5.25	Vdc
Input High Voltage	V_{IH}	2.0	–	–	Vdc
Input Low Voltage	V_{IL}	–	–	0.8	Vdc

DC CHARACTERISTICS

			Open-Collector Output			Three-State Output			
Symbol	Parameter	Test Conditions	Min	Typ	Max	Min	Typ	Max	Unit
I_{RA}, I_{RE} I_{FA}, I_{FE}	Address/Enable "1" Input Current "0"	$V_{IH} = V_{CC}$ Max $V_{IL} = 0.45$ V	– –	– -0.1	40 -0.25	– –	– -0.1	40 -0.25	μAdc mAdc
V_{OH} V_{OL}	Output Voltage "1" "0"	$I_{OH} = -2.0$ mA, $V_{CC} = V_{CC}$ Min $I_{OL} = +16$ mA, $V_{CC} = V_{CC}$ Min	N/A –	– 0.35	– 0.45	2.4 –	3.4 0.35	– 0.45	Vdc Vdc
I_{OHE} I_{OLE}	Output Disabled "1" Current "0"	V_{OH}, $V_{CC} = V_{CC}$ Max $V_{OL} = +0.3$ V, $V_{CC} = V_{CC}$ Max	– –	– –	100 N/A	– –	– –	100 -100	μAdc μAdc
I_{OH}	Output Leakage "1"	V_{OH}, $V_{CC} = V_{CC}$ Max	–	–	100	–	–	N/A	μAdc
V_{CL}	Input Clamp Voltage	$I_{in} = -10$ mA	–	–	-1.5	–	–	-1.5	Vdc
I_{OS}	Output Short Circuit Current	$V_{CC} = V_{CC}$ Max, $V_{out} = 0.0$ V One Output Only for 1 s Max	N/A	–	N/A	15	–	70	mAdc
I_{CC}	Power Supply Current MCM7680/MCM7681DC MCM7680/MCM7681DM	$V_{CC} = V_{CC}$ Max All Inputs Grounded	 – –	 110 110	 150 170	 – –	 110 110	 150 170	 mAdc mAdc

CAPACITANCE (f = 1.0 MHz, $T_A = 25^{\circ}$C, periodically sampled rather than 100% tested.)

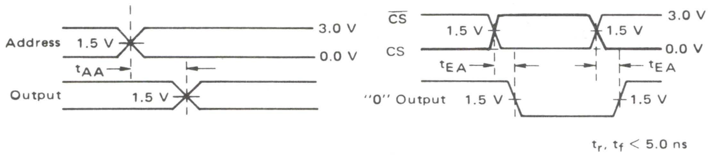
Characteristic	Symbol	Typ	Unit
Input Capacitance	C_{in}	8.0	pF
Output Capacitance	C_{out}	8.0	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

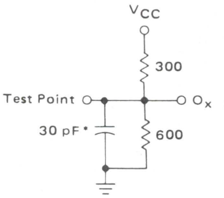
(Full operating voltage and temperature unless otherwise noted)

		0 to +70°C		-55 to +125°C		
Characteristic	Symbol	Typ	Max	Typ	Max	Unit
Address to Output Access Time	t_{AA}	45	70	45	85	ns
Chip Enable Access Time MCM7680/81	t_{EA}	30	40	30	50	ns

TIMING DIAGRAM



AC TEST LOAD



*Includes Jig Capacitance

PROGRAMMING

The PROMs are manufactured with all bits/outputs Logical "1" (Output High). Any desired bit/output can be programmed to a Logical "0" (Output Low) by following the simple procedure shown below. One may build his own programmer to satisfy the sepcifications described in Table 1, or buy any of the commercially available programmers which meet these specifications. These PROMs can be programmed automatically or by the manual procedure shown below.

PROGRAMMING PROCEDURE

1. Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL-compatible. An open circuit should not be used to address the PROM.
2. Disable the chip by applying inputs highs (V_{IH}) to the $\overline{CS}$ inputs. CS inputs must remain at V_{IH} for program and verify. The chip select is TTL-compatible. An open circuit should not be used to disable the chip.
3. Disable the programming circuitry by applying an Output Voltage Disable of less than V_{OPD} to the output of the PROM. The output may be left open to achieve the disable.
4. Raise V_{CC} to V_{PH} with rise time equal to t_r.
5. After a delay equal to or greater than t_d, apply a pulse with amplitude of V_{OPE} and duration of t_p to the output selected for programming. Note that the PROM is supplied with fuses intact generating an output high. Programming a fuse will cause the output to go low in the verify mode.
6. Other bits in the same word may be programmed while the V_{CC} input is raised to V_{PH} by applying output enable pulses to each output which is to be programmed. The output enable pulses must be separated by a minimum interval of t_d.
7. Lower V_{CC} to 4.5 Volts following a delay of t_d from the last programming enable pulse applied to an output.
8. Enable the PROM for verification by applying a logic "0" (V_{IL}) to the $\overline{CS}$ inputs.
9. If any bit does not verify as programmed, repeat Steps 2 through 8 until the bit has received a total of 1.0 ms of programming time. Bits which do not program within 1.0 ms may be considered programming rejects. Multiple pulses of durations shorter than 1.0 ms may be used to enhance programming speed.
10. Repeat Steps 1 through 9 for all other bits to be programmed in the PROM.
11. Programming rejects returned to the factory must be accompanied by data giving address with desired and actual output data of a location in which a programming failure has occurred.

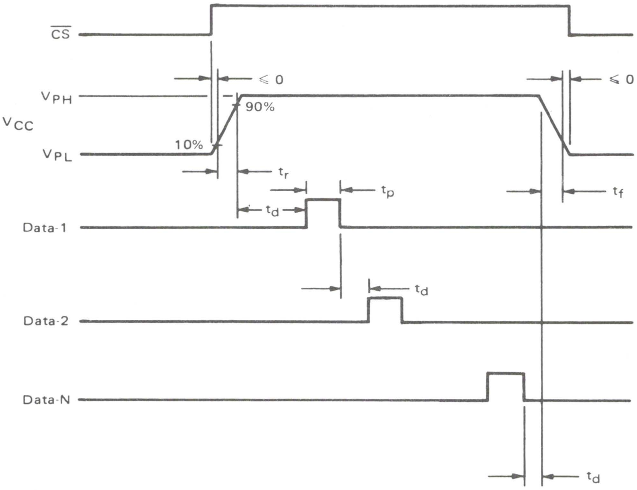
TABLE 1
PROGRAMMING SPECIFICATIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{IH}	Address Input	2.4	5.0	5.0	V
V_{IL}	Voltage(1)	0.0	0.4	0.8	V
V_{PH}	Programming/Verify	11.75	12.0	12.25	V
V_{PL}	Voltage to V_{CC}	4.5	4.5	5.5	V
I_{CCP}	Programming Voltage Current Limit Programming (V_{CC})	600	600	650	mA
t_r	Voltage Rise and	1	1	10	µs
t_f	Fall Time	1	1	10	µs
t_d	Programming Delay	10	10	100	µs
t_p	Programming Pulse Width	100	–	1000	µs
DC	Programming Duty Cycle	–	50	90	%
	Output Voltage				
V_{OPE}	Enable	10.0	10.5	11.0	V
V_{OPD}	Disable(2)	4.5	5.0	5.5	V
I_{OPE}	Output Voltage Enable Current	2	4	10	mA
T_C	Case Temperature	–	25	75	°C

(1) Address and chip select should not be left open for V_{IH}.

(2) Disable condition will be met with output open circuit.

FIGURE 1 — TYPICAL PROGRAMMING WAVEFORMS


$\overline{CS}$
≤ 0
≤ 0
V_{PH}
V_{CC}
90%
10%
V_{PL}
t_r
t_p
t_f
t_d
Data-1
t_d
Data-2
Data-N
t_d

MOTOROLA

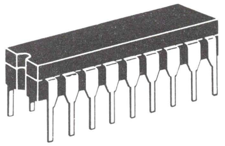
Advance Information

MCM7684
MCM7685

MTTL

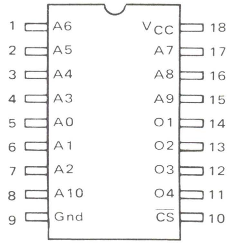
8192-BIT PROGRAMMABLE READ ONLY MEMORIES

MCM7684 – 2048 × 4 – Open-Collector
MCM7685 – 2048 × 4 – Three-State



D SUFFIX
CERAMIC PACKAGE
CASE 726

PIN ASSIGNMENT



8192-BIT PROGRAMMABLE READ ONLY MEMORY

The MCM7684/85 together with the MCM7620/21/40/41/42/43/80/81 comprise a complete, compatible family having common dc electrical characteristics and identical programming requirements. They are fully decoded, high-speed, field-programmable ROMs and are available in commonly used organizations, with both open-collector and three-state outputs. All bits are manufactured storing a logical "1" (outputs high), and can be selectively programmed for logical "0" (outputs low).

The field-programmable PROM can be custom-programmed to any pattern using a simple programming procedure. Schottky bipolar circuitry provides fast access time, and features temperature and voltage compensation to minimize access time variations.

Pinouts are compatible to industry-standard PROMs and ROMs. In addition, the MCM7684 and 85 are pin compatible replacement for the 1024 × 4 with pin 8 connected as A10 on the 2048 × 4.

In addition to the conventional storage array, extra test rows and columns are included to assure high programmability, and guarantee parametric and ac performance. Fuses in these test rows and columns are blown prior to shipment.

- Common dc Electrical Characteristics and Programming Procedure
- Simple, High-Speed Programming Procedure (0.1 second per 1024 Bits, Typical)
- Expandable – Open-Collector or Three-State Outputs and Chip Enable Input
- Inputs and Outputs TTL-Compatible
  - Low Input Current – 250 μA Logic "0", 40 μA Logic "1"
  - Full Output Drive – 16 mA Sink, 2.0 mA Source
- Fast Access Time – Guaranteed for Worst-Case N^2 Sequencing, Over Commercial and Military Temperature Ranges
- Pin-Compatible with Industry-Standard PROMs and ROMs

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Supply Voltage (operating)	V_{CC}	+7.0	Vdc
Input Voltage	V_{in}	+5.5	Vdc
Output Voltage (operating)	V_{OH}	+7.0	Vdc
Supply Current	I_{CC}	650	mAdc
Input Current	I_{in}	-20	mAdc
Output Sink Current	I_{O}	100	mAdc
Operating Temperature Range	T_A		°C
MCM76xxDM		-55 to +125	
MCM76xxDC		0 to +70	
Storage Temperature Range	T_{stg}	-55 to +150	°C
Maximum Junction Temperature	T_J	+175	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability. (While programming, follow the programming specifications.)

This is advance information and specifications are subject to change without notice.

DC OPERATING CONDITIONS AND CHARACTERISTICS

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}				Vdc
MCM76xxDM		4.50	5.0	5.50	
MCM76xxDC		4.75	5.0	5.25	
Input High Voltage	V_{IH}	2.0	–	–	Vdc
Input Low Voltage	V_{IL}	–	–	0.8	Vdc

DC CHARACTERISTICS

(Over Recommended Operating Temperature Range)

			Open-Collector Output			Three-State Output			
Symbol	Parameter	Test Conditions	Min	Typ	Max	Min	Typ	Max	Unit
I_{RA}, I_{RE}	Address/Enable "1"	$V_{IH} = V_{CC}$ Max	–	–	40	–	–	40	μAdc
I_{FA}, I_{FE}	Input Current "0"	$V_{IL} = 0.45$ V	–	-0.1	-0.25	–	-0.1	-0.25	mAdc
V_{OH}	Output Voltage "1"	$I_{OH} = -2.0$ mA, V_{CC} Min	N/A	–	–	2.4	3.4	–	Vdc
V_{OL}	"0"	$I_{OL} = +16$ mA, V_{CC} Min	–	0.35	0.45	–	0.35	0.45	Vdc
I_{OHZ}	Output Disabled "1"	V_{OH}, V_{CC} Max	–	–	100	–	–	100	μAdc
I_{OLZ}	Current "0"	$V_{OL} = +0.3$ V, V_{CC} Max	–	–	N/A	–	–	-100	μAdc
I_{OH}	Output Leakage "1"	V_{OH}, V_{CC} Max	–	–	100	–	–	N/A	μAdc
V_{IC}	Input Clamp Voltage	$I_{in} = -10$ mA	–	–	-1.5	–	–	-1.5	Vdc
I_{OS}	Output Short Circuit Current	V_{CC} Max, $V_{out} = 0.0$ V One Output Only for 1 s Max	N/A	–	N/A	15	–	70	mAdc
I_{CC}	Power Supply Current	V_{CC} Max All Inputs Grounded							
	MCM7684/MCM7685 DC		–	80	120	–	80	120	mAdc
	MCM7684/MCM7685 DM		–	80	140	–	80	140	mAdc

CAPACITANCE (f = 1.0 MHz, $T_A = 25^{\circ}$C, periodically sampled rather than 100% tested.)

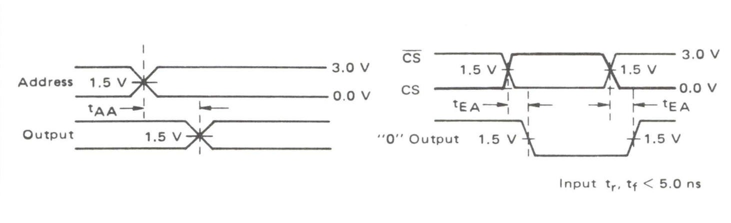
Characteristic	Symbol	Typ	Unit
Input Capacitance	C_{in}	8.0	pF
Output Capacitance	C_{out}	8.0	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted)

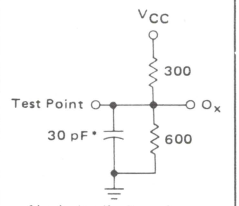
		0 to +70°C		-55 to +125°C		
Characteristic	Symbol	Typ	Max	Typ	Max	Unit
Address to Output Access Time	t_{AA}	45	70	45	85	ns
Chip Enable Access Time	t_{EA}	15	25	15	30	ns

TIMING DIAGRAM



Input t_r, t_f < 5.0 ns

AC TEST LOAD



*Includes Jig Capacitance

PROGRAMMING

The PROMs are manufactured with all bits/outputs Logical "1" (Output High). Any desired bit/output can be programmed to a Logical "0" (Output Low) by following the simple procedure shown below. One may build his own programmer to satisfy the sepcifications described in Table 1, or buy any of the commercially available programmers which meet these specifications. These PROMs can be programmed automatically or by the manual procedure shown below.

PROGRAMMING PROCEDURE

1. Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL-compatible. An open circuit should not be used to address the PROM.
2. Disable the chip by applying an input high (V_{IH}) to the $\overline{CS}$ input. The chip select is TTL-compatible. An open circuit should not be used to disable the chip.
3. Disable the programming circuitry by applying an Output Voltage Disable of less than V_{OPD} to the output of the PROM. The output may be left open to achieve the disable.
4. Raise V_{CC} to V_{PH} with rise time equal to t_r.
5. After a delay equal to or greater than t_d, apply a pulse with amplitude of V_{OPE} and duration of t_p to the output selected for programming. Note that the PROM is supplied with fuses intact generating an output high. Programming a fuse will cause the output to go low in the verify mode.
6. Other bits in the same word may be programmed while the V_{CC} input is raised to V_{PH} by applying output enable pulses to each output which is to be programmed. The output enable pulses must be separated by a minimum interval of t_d.
7. Lower V_{CC} to 4.5 Volts following a delay of t_d from the last programming enable pulse applied to an output.
8. Enable the PROM for verification by applying a logic "0" (V_{IL}) to the $\overline{CS}$ inputs.
9. If any bit does not verify as programmed, repeat Steps 2 through 8 until the bit has received a total of 1.0 ms of programming time. Bits which do not program within 1.0 ms may be considered programming rejects. Multiple pulses of durations shorter than 1.0 ms may be used to enhance programming speed.
10. Repeat Steps 1 through 9 for all other bits to be programmed in the PROM.
11. Programming rejects returned to the factory must be accompanied by data giving address with desired and actual output data of a location in which a programming failure has occurred.

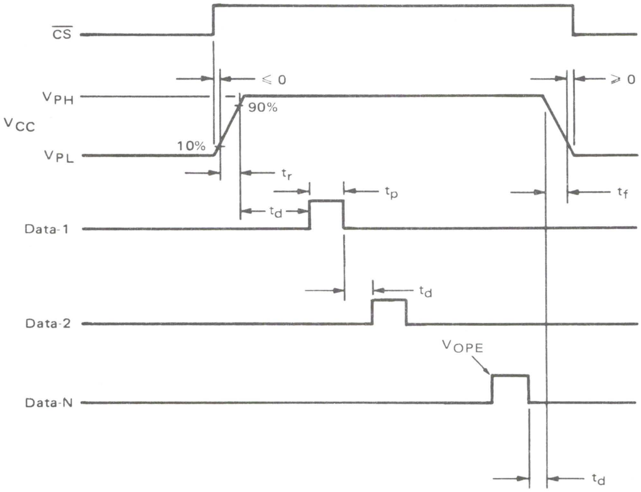
TABLE 1
PROGRAMMING SPECIFICATIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{IH}	Address Input	2.4	5.0	5.0	V
V_{IL}	Voltage(1)	0.0	0.4	0.8	V
V_{PH}	Programming/Verify	11.75	12.0	12.25	V
V_{PL}	Voltage to V_{CC}	4.5	4.5	5.5	V
I_{CCP}	Programming Voltage Current Limit	600	600	650	mA
t_r	Programming (V_{CC}) Voltage Rise and	1	1	10	µs
t_f	Fall Time	1	1	10	µs
t_d	Programming Delay	10	10	100	µs
t_p	Programming Pulse Width	100	–	1000	µs
DC	Programming Duty Cycle	–	50	90	%
	Output Voltage				
V_{OPE}	Enable	10.0	10.5	11.0	V
V_{OPD}	Disable(2)	4.5	5.0	5.5	V
I_{OPE}	Output Voltage Enable Current	2	4	10	mA
T_C	Case Temperature	–	25	75	°C

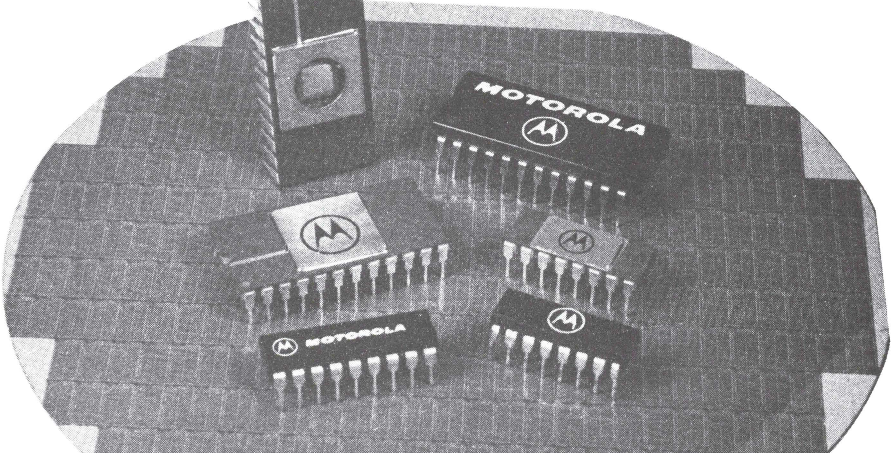
(1) Address and chip select should not be left open for V_{IH}.

(2) Disable condition will be met with output open circuit.

FIGURE 1 – TYPICAL PROGRAMMING WAVEFORMS


$\overline{CS}$
$\leqslant 0$
$\geqslant 0$
V_{PH}
V_{CC}
90%
10%
V_{PL}
t_r
t_p
t_f
t_d
Data-1
t_d
Data-2
V_{OPE}
Data-N
t_d

MECL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MECL MEMORIES
GENERAL INFORMATION

Complete information is available in the MECL Data Book. Contact your sales representative or authorized distributor for information.

TABLE 1 — LIMITS BEYOND WHICH DEVICE LIFE MAY BE IMPAIRED

Characteristic	Symbol	Rating	Unit
Supply Voltage	V_{EE}	−8.0 to 0	V
Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	V
Output Source Current — Continuous Surge	I_{out}	50 100	mA
Junction Temperature — Ceramic Package① Plastic Package	T_J	165 150	°C
Storage Temperature	T_{stg}	−55 to +150	°C

① Maximum T_J may be exceeded (≤ 250°C) for short periods of time (≤ 240 hours) without significant reduction in device life.

TABLE 2 — LIMITS BEYOND WHICH PERFORMANCE MAY BE DEGRADED

Characteristic	Symbol	Rating	Unit
Supply Voltage (V_{CC} = 0)②	V_{EE}	−4.94 to −5.46	V
Output Drive — MCM10100 Series MCM10400 Series MCM10500 Series	—	50 Ω to −2.0 V 50 Ω to −2.0 V 100 Ω to −2.0 V	Ω
Operating Temperature Range③ MCM10100 Series MCM10400 Series MCM10500 Series	T_A	 0 to 75 −55 to +150 −55 to +125	°C

② Functionality only. Data sheet limits are specified for −5.19 to −5.21 V.

③ With airflow ≥ 500 lfpm.

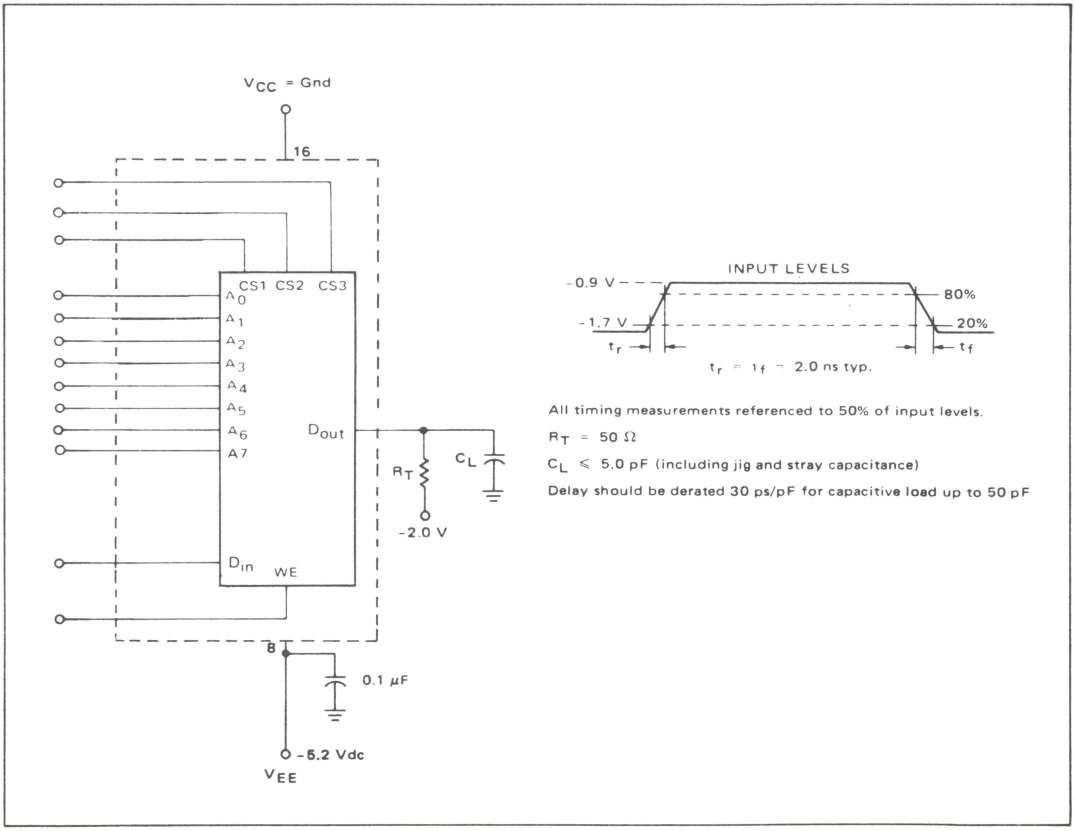
TABLE 3 – DC TEST PARAMETERS

Each MECL 10,000 series device has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 linear feet per minute is maintained. $V_{EE} = -5.2$ V ±0.010 V.

Forcing Function	Parameter	–55°C	0°C	25°C		75°C	125°C
		MCM10500*	MCM10100**	MCM10100**	MCM10500*	MCM10100**	MCM10500*
V_{IHmax} =	V_{OHmax}	–0.880	–0.840	–0.810	–0.780	–0.720	–0.630
	V_{OHmin}	–1.080	–1.000	–0.960	–0.930	–0.900	–0.825
	V_{OHAmin}	–1.100	–1.020	–0.980	–0.950	–0.920	–0.845
V_{IHAmin}		–1.255	–1.145	–1.105	–1.105	–1.045	–1.000
V_{ILAmin}		–1.510	–1.490	–1.475	–1.475	–1.450	–1.400
	V_{OLAmin}	–1.635	–1.645	–1.630	–1.600	–1.605	–1.525
	V_{OLAmax}	–1.655	–1.665	–1.650	–1.620	–1.625	–1.545
V_{ILmin} =	V_{OLmin}	–1.920	–1.870	–1.850	–1.850	–1.830	–1.820
V_{ILmin}	I_{INLmin}	0.5	0.5	0.5	0.5	0.3	0.3

*Driving 100 Ω to –2.0 V.

**Driving 50 Ω to –2.0 V.



$t_r = t_f = 2.0$ ns typ.

All timing measurements referenced to 50% of input levels.

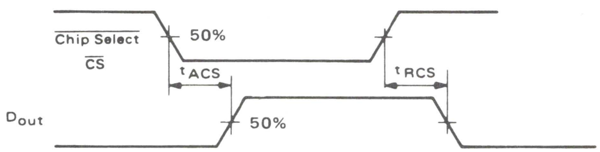
$R_T = 50\ \Omega$

$C_L \leq 5.0$ pF (including jig and stray capacitance)

Delay should be derated 30 ps/pF for capacitive load up to 50 pF

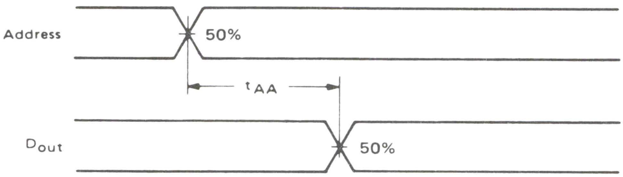
FIGURE 1 – SWITCHING TIME TEST CIRCUIT

FIGURE 2 — CHIP SELECT ACCESS TIME WAVEFORM



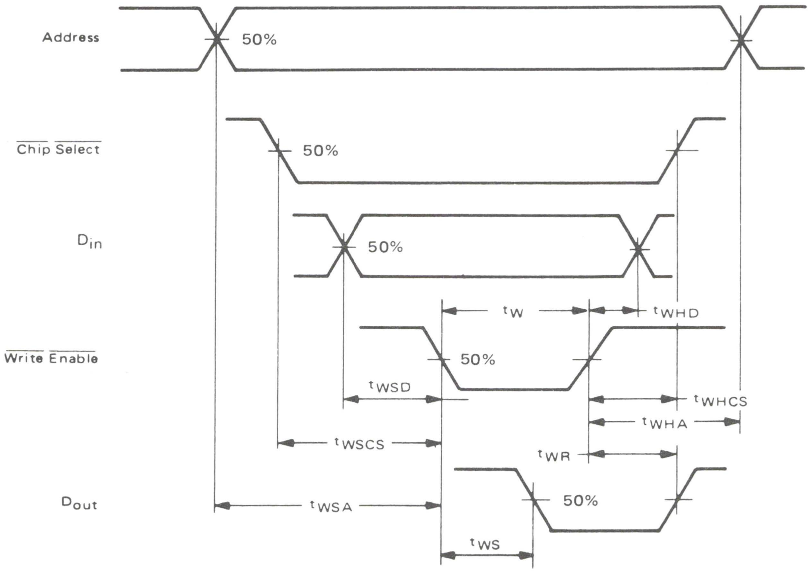
$\overline{\text{Chip Select}}$
$\overline{\text{CS}}$
50%
t_{ACS}
t_{RCS}
D_{out}
50%

FIGURE 3 — ADDRESS ACCESS TIME WAVEFORM

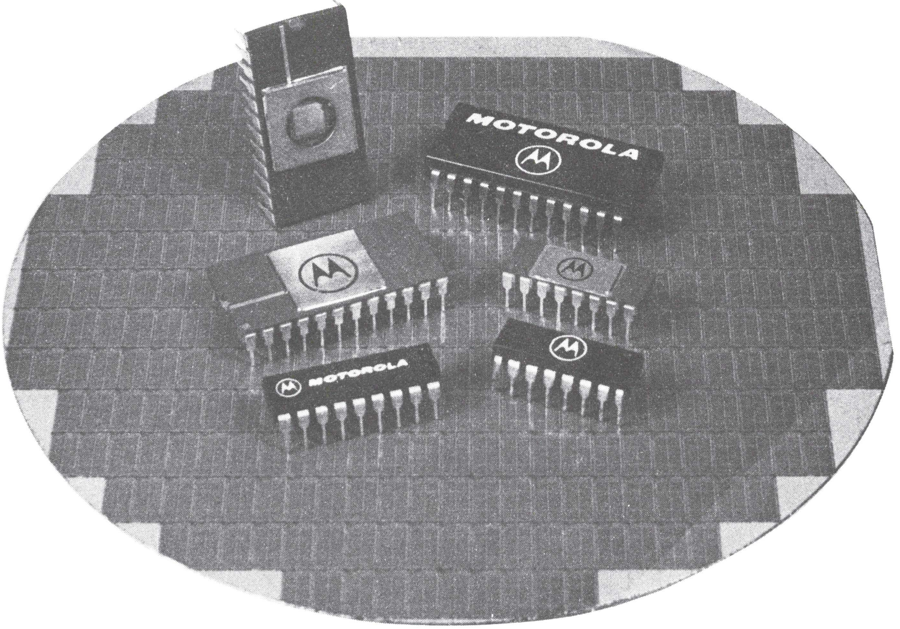


Address
50%
t_{AA}
D_{out}
50%

FIGURE 4 — SETUP AND HOLD WAVEFORMS (WRITE MODE)



Address
50%
$\overline{\text{Chip Select}}$
50%
D_{in}
50%
t_W
t_{WHD}
$\overline{\text{Write Enable}}$
50%
t_{WSD}
t_{WHCS}
t_{WHA}
t_{WSCS}
t_{WR}
D_{out}
50%
t_{WSA}
t_{WS}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MECL RAM

MOTOROLA

MCM10143

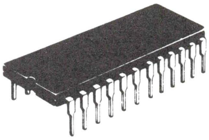
8 X 2 MULTIPORT REGISTER FILE (RAM)

8 x 2 MULTIPORT REGISTER FILE (RAM)

The MCM10143 is an 8 word by 2 bit multiport register file (RAM) capable of reading two locations and writing one location simultaneously. Two sets of eight latches are used for data storage in this LSI circuit.

WRITE

The word to be written is selected by addresses A_0-A_2. Each bit of the word has a separate write enable to allow more flexibility in system design. A write occurs on the positive transition of the clock. Data is enabled by having the write enables at a low level when the clock makes the transition. To inhibit a bit from being written, the bit enable must be at a high level when the clock goes low and not change until the clock goes high. Operation of the clock and the bit enables can be reversed. While the clock is low a positive transition of the bit enable will write that bit into the address selected by A_0-A_2.



L SUFFIX
CERAMIC PACKAGE
CASE 623

READ

When the clock is high any two words may be read out simultaneously, as selected by addresses B_0-B_2 and C_0-C_2, including the word written during the preceding half clock cycle. When the clock goes low the addressed data is stored in the slaves. Level changes on the read address lines have no effect on the output until the clock again goes high. Read out is accomplished at any time by enabling output gates (B_0-B_1), (C_0-C_1).

t_{pd}:

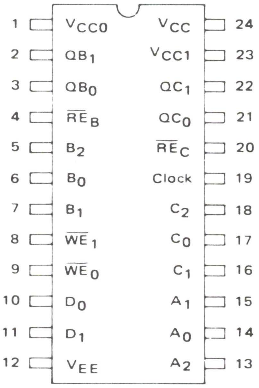
Clock to Data out = 5 ns (typ)
(Read Selected)

Address to Data out = 10 ns (typ)
(Clock High)

$\overline{\text{Read Enable}}$ to Data out = 2.8 ns (typ)
(Clock high, Addresses present)

P_D = 610 mW/pkg (typ no load)

PIN ASSIGNMENT



TRUTH TABLE

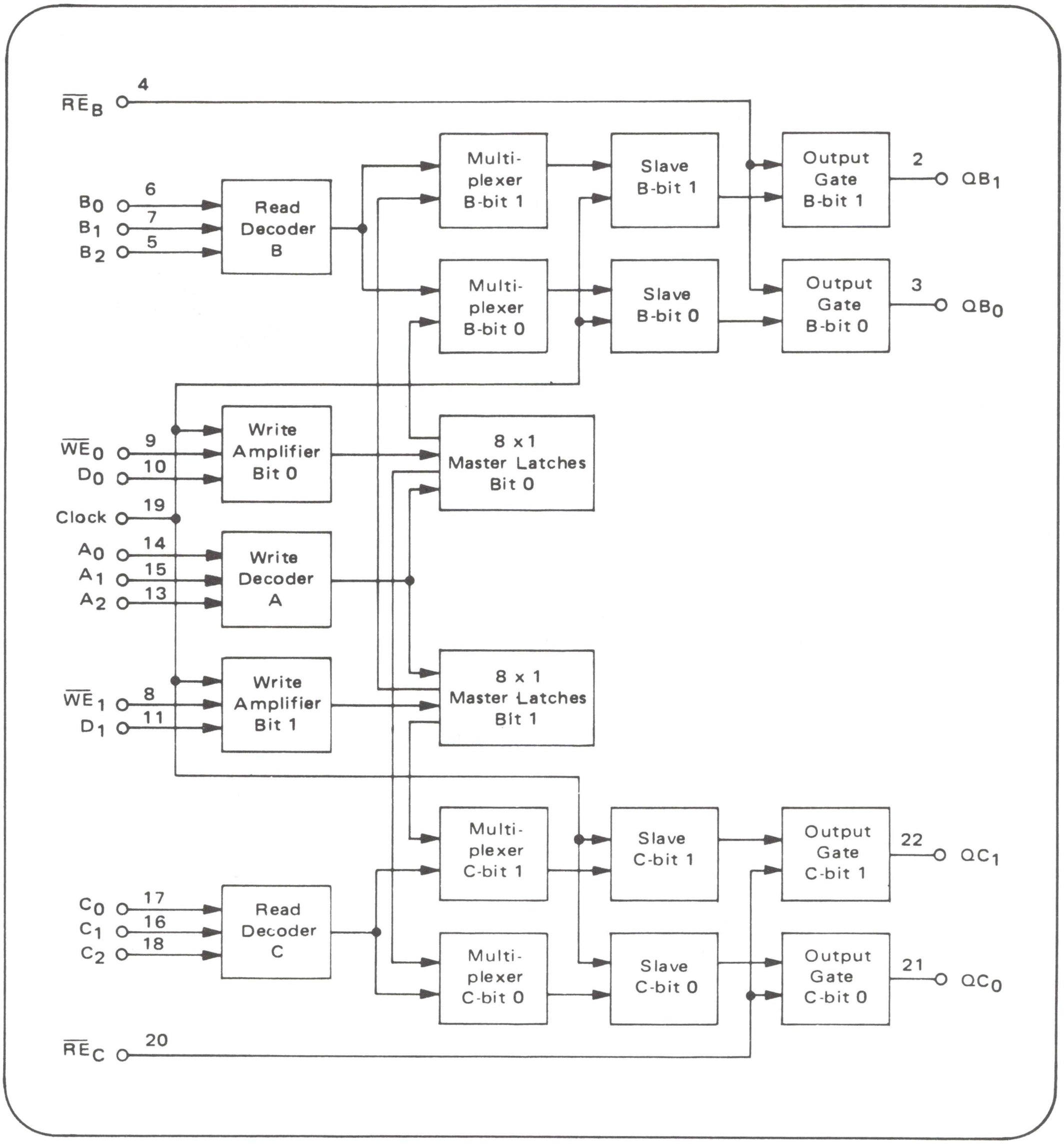
*MODE	INPUT							OUTPUT			
	**Clock	$\overline{WE}_0$	$\overline{WE}_1$	D_0	D_1	$\overline{RE}_B$	$\overline{RE}_C$	QB_0	QB_1	QC_0	QC_1
Write	L→H	L	L	H	H	H	H	L	L	L	L
Read	H	ϕ	ϕ	ϕ	ϕ	L	L	H	H	H	H
Read	H→L	ϕ	ϕ	ϕ	ϕ	L	L	H	H	H	H
Read	L→H→L	H	H	ϕ	ϕ	L	L	H	H	H	H
Write	L→H	L	L	L	H	H	H	L	L	L	L
Read	H	ϕ	ϕ	ϕ	ϕ	L	L	L	H	L	H

**Note: Clock occurs sequentially through Truth Table

*Note: A0-A2, B0-B2, and C0-C2 are all set to same address location throughout Table.

ϕ - Don't Care

BLOCK DIAGRAM

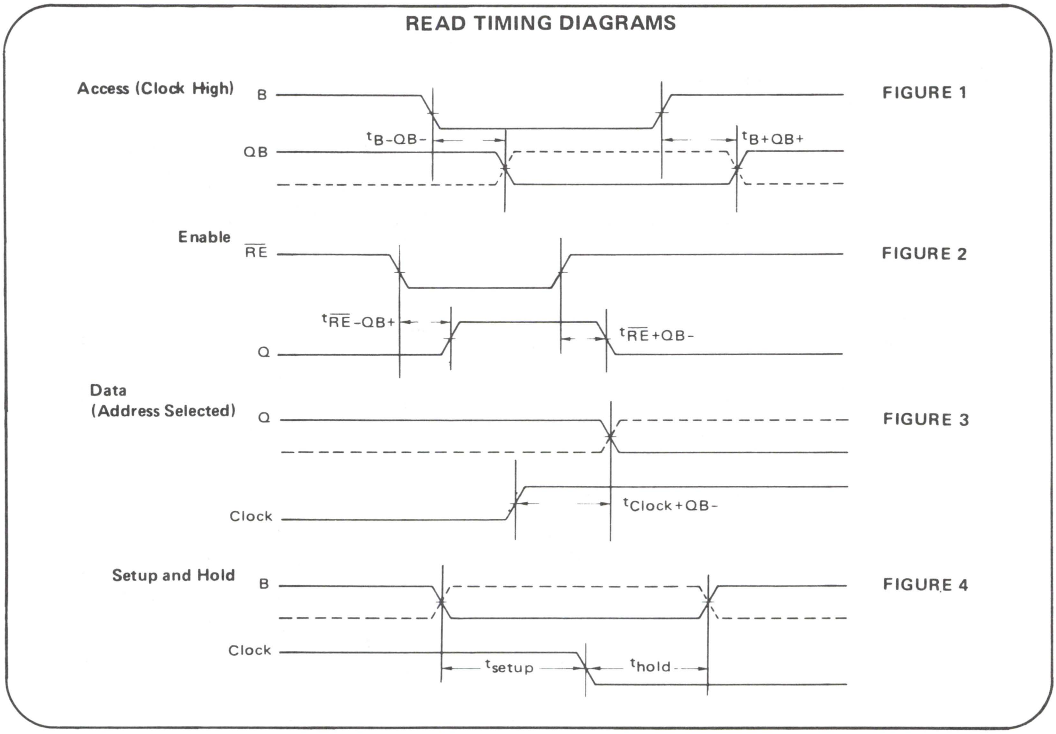

$\overline{RE}_B$ 4
B_0 6
B_1 7
B_2 5
Read Decoder B
Multi-plexer B-bit 1
Multi-plexer B-bit 0
Slave B-bit 1
Slave B-bit 0
Output Gate B-bit 1
Output Gate B-bit 0
2 QB_1
3 QB_0
$\overline{WE}_0$ 9
D_0 10
Write Amplifier Bit 0
8 x 1 Master Latches Bit 0
Clock 19
A_0 14
A_1 15
A_2 13
Write Decoder A
$\overline{WE}_1$ 8
D_1 11
Write Amplifier Bit 1
8 x 1 Master Latches Bit 1
Multi-plexer C-bit 1
Multi-plexer C-bit 0
Slave C-bit 1
Slave C-bit 0
Output Gate C-bit 1
Output Gate C-bit 0
22 QC_1
21 QC_0
C_0 17
C_1 16
C_2 18
Read Decoder C
$\overline{RE}_C$ 20

ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	0°C		+25°C			+75°C		Unit
		Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	–	150	–	118	150	–	150	mAdc
Input Current	I_{inH}								µAdc
Pins 10, 11, 19		–	245	–	–	245	–	245	
All other pins		–	200	–	–	200	–	200	
Switching Times ①									ns
Read Mode									
Address Input	$t_{B\pm QB\pm}$	4.0	15.3	4.5	10	14.5	4.5	15.5	
Read Enable	$t_{\overline{RE}-QB+}$	1.1	5.3	1.2	3.5	5.0	1.2	5.5	
Data	$t_{Clock+QB-}$	1.7	7.3	2.0	5.0	7.0	2.0	7.6	
Setup									
Address	$t_{setup(B-Clock-)}$	–	–	8.5	5.5	–	–	–	
Hold									
Address	$t_{hold(Clock-B+)}$	–	–	−1.5	−4.5	–	–	–	
Write Mode									
Setup									
Write Enable	$t_{setup(\overline{WE}-Clock+)}$	–	–	7.0	4.0	–	–	–	
	$t_{setup(\overline{WE}+Clock-)}$	–	–	1.0	−2.0	–	–	–	
Address	$t_{setup(A-Clock+)}$	–	–	8.0	5.0	–	–	–	
Data	$t_{setup(D-Clock+)}$	–	–	5.0	2.0	–	–	–	
Hold									
Write Enable	$t_{hold(Clock+\overline{WE}+)}$	–	–	5.5	2.5	–	–	–	
	$t_{hold(Clock+\overline{WE}-)}$	–	–	1.0	−2.0	–	–	–	
Address	$t_{hold(Clock+A+)}$	–	–	1.0	−3.0	–	–	–	
Data	$t_{hold(Clock+D+)}$	–	–	1.0	−2.0	–	–	–	
Write Pulse Width	$PW_{\overline{WE}}$	–	–	8.0	5.0	–	–	–	
Rise Time, Fall Time (20% to 80%)	t_r, t_f	1.1	4.2	1.1	2.5	4.0	1.1	4.5	

①AC timing figures do not show all the necessary presetting conditions.

READ TIMING DIAGRAMS


Access (Clock High)
B
QB
t_{B-QB-}
t_{B+QB+}
FIGURE 1
Enable
$\overline{RE}$
Q
$t_{\overline{RE}-QB+}$
$t_{\overline{RE}+QB-}$
FIGURE 2
Data
(Address Selected)
Q
Clock
$t_{Clock+QB-}$
FIGURE 3
Setup and Hold
B
Clock
t_{setup}
t_{hold}
FIGURE 4

WRITE TIMING DIAGRAM

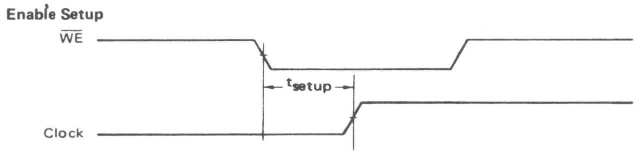

Enable Setup
WE
t_{setup}
Clock

FIGURE 5

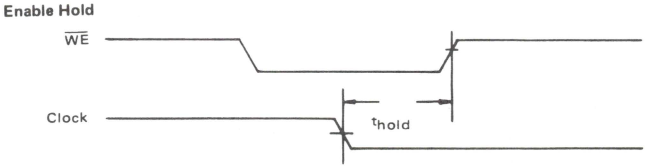

Enable Hold
WE
Clock
t_{hold}

FIGURE 6

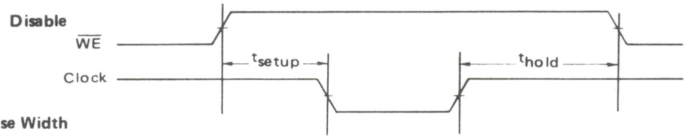

Disable
WE
Clock
t_{setup}
t_{hold}

FIGURE 7

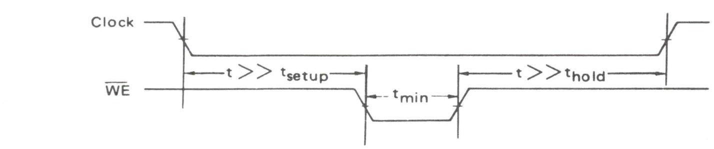

Pulse Width
Clock
WE
t >> t_{setup}
t_{min}
t >> t_{hold}

FIGURE 8

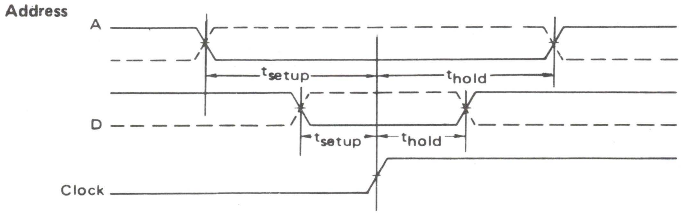

Address
A
t_{setup}
t_{hold}
D
t_{setup}
t_{hold}
Clock

FIGURE 9

MCM10144/MCM10544

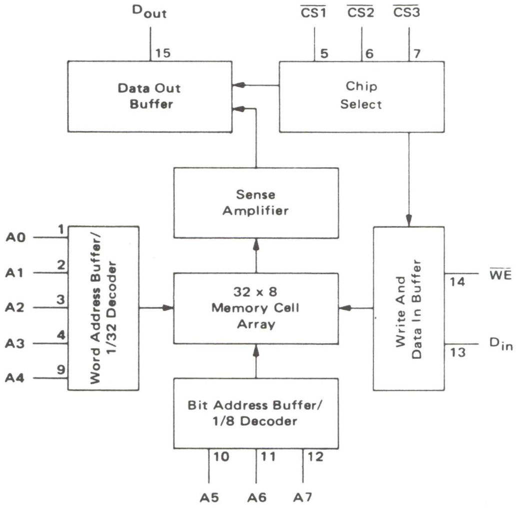
256 X 1-BIT RANDOM ACCESS MEMORY

The MCM10144/10544 is a 256 word X 1-bit RAM. Bit selection is achieved by means of an 8-bit address A0 through A7.

The active-low chip select allows memory expansion up to 2048 words. The fast chip select access time allows memory expansion without affecting system performance.

The operating mode of the RAM ($\overline{CS}$ inputs low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low the chip is in the write mode—the output is low and the data present at D_{in} is stored at the selected address. With $\overline{WE}$ high the chip is in the read mode—the data state at the selected memory location is presented non-inverted at D_{out}.

- Typical Address Access Time = 17 ns
- Typical Chip Select Access Time = 4.0 ns
- 50 kΩ Input Pulldown Resistors on Chip Select
- Power Dissipation (470 mW typ @ 25°C) Decreases with Increasing Temperature
- Pin-for-Pin Replacement for F10410



Dout
CS1
CS2
CS3
15
5
6
7
Data Out Buffer
Chip Select
Sense Amplifier
A0
A1
A2
A3
A4
1
2
3
4
9
Word Address Buffer/ 1/32 Decoder
32 x 8 Memory Cell Array
Write And Data In Buffer
14
WE
13
Din
Bit Address Buffer/ 1/8 Decoder
10
11
12
A5
A6
A7

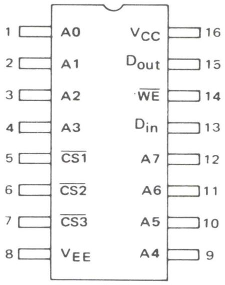
TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$*	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	φ	Q
Disabled	H	φ	φ	L

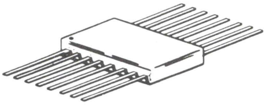
*$\overline{CS} = \overline{CS1} + \overline{CS2} + \overline{CS3}$

φ = Don't Care.

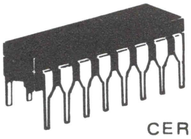
PIN ASSIGNMENT



1
2
3
4
5
6
7
8
A0
A1
A2
A3
CS1
CS2
CS3
VEE
VCC
Dout
WE
Din
A7
A6
A5
A4
16
15
14
13
12
11
10
9



F SUFFIX
CERAMIC PACKAGE
CASE 650



L SUFFIX
CERAMIC PACKAGE
CASE 620

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	−55°C		0°C		+25°C		+75°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_{EE}	—	140	—	135	—	130	—	125	—	125	mAdc
Input Current High	I_{inH}	—	375	—	220	—	220	—	220	—	220	μAdc

-55°C and +125°C test values apply to MC105xx devices only.

SWITCHING CHARACTERISTICS (Note 1)

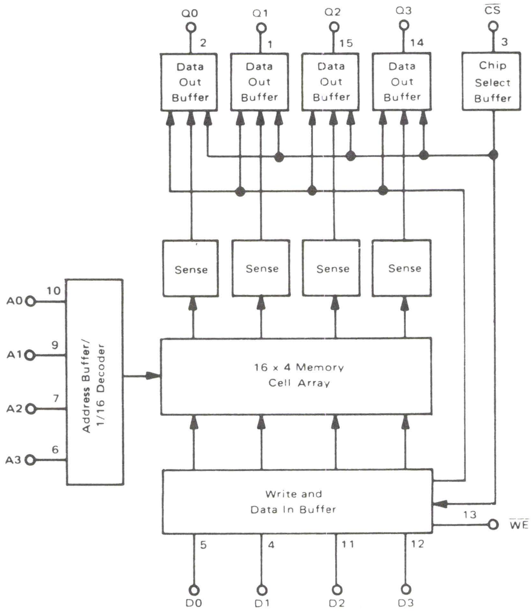
Characteristics	Symbol	MCM10144		MCM10544		Unit	Conditions
		T_A = 0 to +75°C, V_{EE} = −5.2 Vdc ± 5%		T_A = −55 to +125°C, V_{EE} = −5.2 Vdc ± 5%			
		Min	Max	Min	Max		
Read Mode						ns	Measured from 50% of input to 50% of output. See Note 2.
Chip Select Access Time	t_{ACS}	2.0	10	2.0	10		
Chip Select Recovery Time	t_{RCS}	2.0	10	2.0	10		
Address Access Time	t_{AA}	7.0	26	7.0	26		
Write Mode						ns	t_{WSA} = 8.0 ns Measured at 50% of input to 50% of output. t_W = 25 ns.
Write Pulse Width	t_W	25	—	25	—		
Data Setup Time Prior to Write	t_{WSD}	2.0	—	2.0	—		
Data Hold Time After Write	t_{WHD}	2.0	—	2.0	—		
Address Setup Time Prior to Write	t_{WSA}	8.0	—	8.0	—		
Address Hold Time After Write	t_{WHA}	2.0	—	0.0	—		
Chip Select Setup Time Prior to Write	t_{WSCS}	2.0	—	2.0	—		
Chip Select Hold Time After Write	t_{WHCS}	2.0	—	2.0	—		
Write Disable Time	t_{WS}	2.5	10	2.5	10		
Write Recovery Time	t_{WR}	2.5	10	2.5	10		
Rise and Fall Time	t_r, t_f					ns	Measured between 20% and 80% points.
Address to Output		1.5	7.0	1.5	7.0		
$\overline{CS}$ or $\overline{WE}$ to Output		1.5	5.0	1.5	5.0		
Capacitance						pF	Measured with a pulse technique.
Input Capacitance	C_{in}	—	5.0	—	5.0		
Output Capacitance	C_{out}	—	8.0	—	8.0		

NOTES:
1. Test circuit characteristics: $R_T = 50\ \Omega$, MCM10144; $100\ \Omega$, MCM10544. $C_L \leqslant 5.0$ pF (including jig and stray capacitance). Delay should be derated 30 ps/pF for capacitive load up to 50 pF.
2. The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
3. For proper use of MECL Memories in a system environment, consult **MECL System Design** Handbook.

MOTOROLA

MCM10145/MCM10545

16 X 4-BIT REGISTER FILE (RAM)

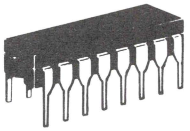

Q0
Q1
Q2
Q3
CS
2
1
15
14
3
Data Out Buffer
Data Out Buffer
Data Out Buffer
Data Out Buffer
Chip Select Buffer
Sense
Sense
Sense
Sense
A0
A1
A2
A3
10
9
7
6
Address Buffer/ 1/16 Decoder
16 x 4 Memory Cell Array
Write and Data In Buffer
13
WE
5
4
11
12
D0
D1
D2
D3

The MCM10145/10545 is a 16 word X 4-bit RAM. Bit selection is achieved by means of a 4-bit address A0 through A3.

The active-low chip select allows memory expansion up to 32 words. The fast chip select access time allows memory expansion without affecting system performance.

The operating mode of the RAM ($\overline{CS}$ input low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low the chip is in the write mode—the output is low and the data present at D_n is stored at the selected address. With $\overline{WE}$ high the chip is in the read mode—the data state at the selected memory location is presented non-inverted at Q_n.

- Typical Address Access Time = 10 ns
- Typical Chip Select Access Time = 4.5 ns
- 50 kΩ Pulldown Resistors on All Inputs
- Power Dissipation (470 mW typ @ 25°C) Decreases with Increasing Temperature



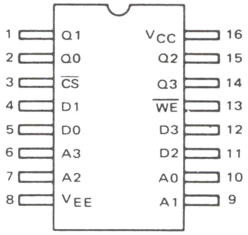
L SUFFIX
CERAMIC PACKAGE
CASE 620

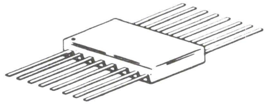
TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$	$\overline{WE}$	D_n	Q_n
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

ϕ = Don't Care.

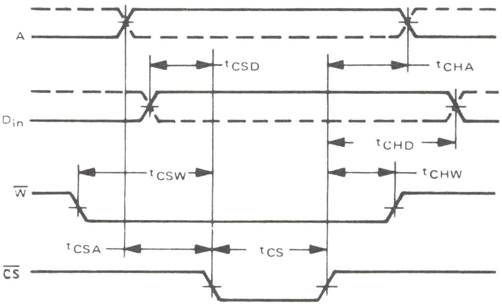
PIN ASSIGNMENT


1 Q1
2 Q0
3 CS
4 D1
5 D0
6 A3
7 A2
8 VEE
16 VCC
15 Q2
14 Q3
13 WE
12 D3
11 D2
10 A0
9 A1



F SUFFIX
CERAMIC PACKAGE
CASE 650

FIGURE 1 – CHIP ENABLE STROBE MODE


A
tCSD
tCHA
Din
tCHD
tCSW
tCHW
W
tCSA
tCS
CS

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	-55°C		0°C		+25°C		+75°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_{EE}	–	135	–	130	–	125	–	120	–	120	mAdc
Input Current High	I_{inH}	–	375	–	220	–	220	–	220	–	220	µAdc

-55°C and +125°C test values apply to MC105xx devices only.

SWITCHING CHARACTERISTICS (Note 1)

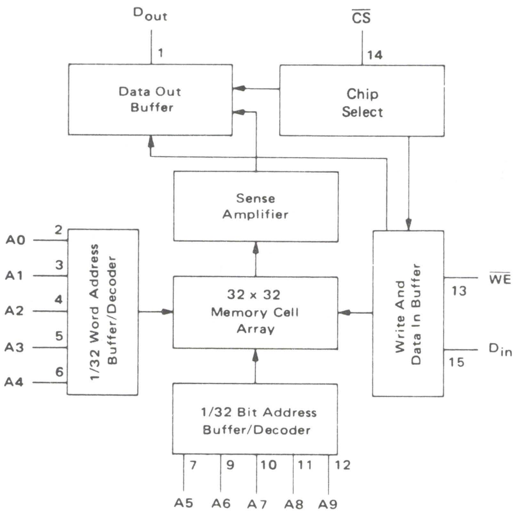
Characteristics	Symbol	MCM10145		MCM10545		Unit	Conditions
		T_A = 0 to +75°C, V_{EE} = -5.2 Vdc ± 5%		T_A = -55 to +125°C, V_{EE} = -5.2 Vdc ± 5%			
		Min	Max	Min	Max		
Read Mode						ns	Measured from 50% of input to 50% of output. See Note 2.
Chip Select Access Time	t_{ACS}	2.0	8.0	2.0	10		
Chip Select Recovery Time	t_{RCS}	2.0	8.0	2.0	10		
Address Access Time	t_{AA}	4.0	15	4.0	18		
Write Mode						ns	t_{WSA} = 5 ns Measured at 50% of input to 50% of output. t_W = 8 ns.
Write Pulse Width	t_W	8.0	–	8.0	–		
Data Setup Time Prior to Write	t_{WSD}	0	–	0	–		
Data Hold Time After Write	t_{WHD}	3.0	–	4.0	–		
Address Setup Time Prior to Write	t_{WSA}	5.0	–	5.0	–		
Address Hold Time After Write	t_{WHA}	1.0	–	3.0	–		
Chip Select Setup Time Prior to Write	t_{WSCS}	0	–	5.0	–		
Chip Select Hold Time After Write	t_{WHCS}	0	–	0	–		
Write Disable Time	t_{WS}	2.0	8.0	2.0	10		
Write Recovery Time	t_{WR}	2.0	8.0	2.0	10		
Chip Enable Strobe Mode						ns	Guaranteed but not tested on standard product. See Figure 1.
Data Setup Prior to Chip Select	t_{CSD}	0	–	–	–		
Write Enable Setup Prior to Chip Select	t_{CSW}	0	–	–	–		
Address Setup Prior to Chip Select	t_{CSA}	0	–	–	–		
Data Hold Time After Chip Select	t_{CHD}	2.0	–	–	–		
Write Enable Hold Time After Chip Select	t_{CHW}	0	–	–	–		
Address Hold Time After Chip Select	t_{CHA}	4.0	–	–	–		
Chip Select Minimum Pulse Width	t_{CS}	18	–	–	–		
Rise and Fall Time	t_r, t_f					ns	Measured between 20% and 80% points.
Address to Output		1.5	7.0	1.5	7.0		
$\overline{CS}$ to Output		1.5	5.0	1.5	5.0		
Capacitance						pF	Measured with a pulse technique.
Input Capacitance	C_{in}	–	6.0	–	6.0		
Output Capacitance	C_{out}	–	8.0	–	8.0		

NOTES:
1. Test circuit characteristics: R_T = 50 Ω, MCM10145; 100 Ω, MCM10545. $C_L \leqslant 5.0$ pF (including jig and Stray Capacitance). Delay should be derated 30 ps/pF for capacitive loads up to 50 pF.
2. The maximum Address Access Time is guaranteed to be the worst-case bit in the memory.
3. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.

MOTOROLA

MCM10146/MCM10546

1024 X 1-BIT RANDOM ACCESS MEMORY


D_{out}
1
$\overline{CS}$
14
Data Out Buffer
Chip Select
Sense Amplifier
A0
A1
A2
A3
A4
2
3
4
5
6
1/32 Word Address Buffer/Decoder
32 x 32 Memory Cell Array
Write And Data In Buffer
13
$\overline{WE}$
D_{in}
15
1/32 Bit Address Buffer/Decoder
7
9
10
11
12
A5
A6
A7
A8
A9

The MCM10146/10546 is a 1024 X 1-bit RAM. Bit selection is achieved by means of a 10-bit address, A0 to A9.

The active-low chip select is provided for memory expansion up to 2048 words.

The operating mode of the RAM ($\overline{CS}$ input low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low, the chip is in the write mode, the output, D_{out}, is low and the data state present at D_{in} is stored at the selected address. With $\overline{WE}$ high, the chip is in the read mode and the data stored at the selected memory location will be presented non-inverted at D_{out}. (See Truth Table.)

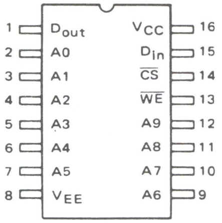
- Pin-for-Pin Compatible with the 10415
- Power Dissipation (520 mW typ @ 25°C) Decreases with Increasing Temperature
- Typical Address Access of 24 ns
- Typical Chip Select Access of 4.0 ns
- 50 kΩ Pulldown Resistor on Chip Select Input

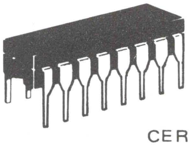
TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

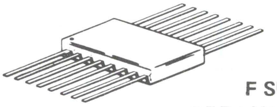
ϕ = Don't Care.

PIN ASSIGNMENT


1
D_{out}
V_{CC}
16
2
A0
D_{in}
15
3
A1
$\overline{CS}$
14
4
A2
$\overline{WE}$
13
5
A3
A9
12
6
A4
A8
11
7
A5
A7
10
8
V_{EE}
A6
9



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650-03

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	−55°C		0°C		+25°C		+75°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_{EE}	–	155	–	150	–	145	–	125	–	125	mAdc
Input Current High	I_{inH}	–	375	–	220	–	220	–	220	–	220	μAdc
Logic "0" Output Voltage	V_{OL}	-1.970	-1.655	-1.920	-1.665	-1.900	-1.650	-1.880	-1.625	-1.870	-1.545	Vdc

NOTE: −55°C and +125°C test values apply to MCM105XX only.

SWITCHING CHARACTERISTICS (Note 1)

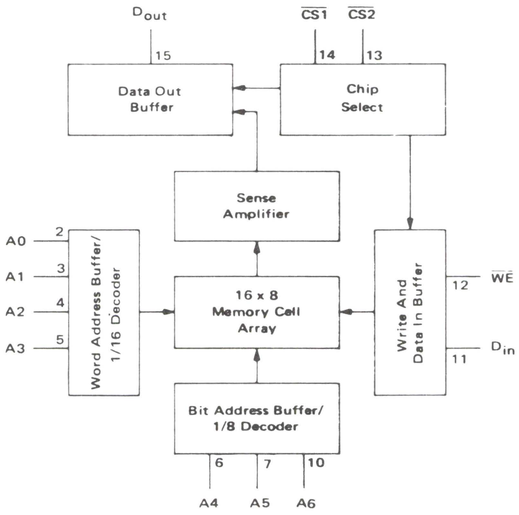
Characteristics	Symbol	MCM10146		MCM10546		Unit	Conditions
		T_A = 0 to +75°C, V_{EE} = −5.2 Vdc ± 5%		T_A = −55 to +125°C, V_{EE} = −5.2 Vdc ± 5%			
		Min	Max	Min	Max		
Read Mode						ns	Measured at 50% of input
Chip Select Access Time	t_{ACS}	2.0	7.0	2.0	8.0		to 50% of output.
Chip Select Recovery Time	t_{RCS}	2.0	7.0	2.0	8.0		See Note 2.
Address Access Time	t_{AA}	8.0	29	8.0	40		
Write Mode						ns	t_{WSA} = 8.0 ns.
Write Pulse Width (To guarantee writing)	t_W	25	–	25	–		Measured at 50% of input to 50% of output.
Data Setup Time Prior to Write	t_{WSD}	5.0	–	5.0	–		t_W = 25 ns
Data Hold Time After Write	t_{WHD}	5.0	–	5.0	–		
Address Setup Time Prior to Write	t_{WSA}	8.0	–	10	–		
Address Hold Time After Write	t_{WHA}	2.0	–	8.0	–		
Chip Select Setup Time Prior to Write	t_{WSCS}	5.0	–	5.0	–		
Chip Select Hold Time After Write	t_{WHCS}	5.0	–	5.0	–		
Write Disable Time	t_{WS}	2.8	7.0	2.8	12		
Write Recovery Time	t_{WR}	2.8	7.0	2.8	12		
Rise and Fall Time	t_r, t_f					ns	Measured between 20% and 80% points.
$\overline{CS}$ or $\overline{WE}$ to Output		1.5	4.0	1.5	4.0		
Address to Output		1.5	8.0	1.5	8.0		
Capacitance						pF	Measured with a pulse technique.
Input Capacitance	C_{in}	–	5.0	–	5.0		
Output Capacitance	C_{out}	–	8.0	–	8.0		

NOTES:
1. Test circuit characteristics: R_T = 50 Ω, MCM10146; 100 Ω, MCM10546. $C_L \leqslant 5.0$ pf including jig and stray capacitance. For Capacitance Loading $\leqslant 50$ pF, delay should be derated by 30 ps/pF.
2. The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
3. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.

MOTOROLA

MCM10147/MCM10547

128 X 1-BIT RANDOM ACCESS MEMORY


D_{out}
15
$\overline{CS1}$
$\overline{CS2}$
14
13
Data Out Buffer
Chip Select
Sense Amplifier
A0
A1
A2
A3
2
3
4
5
Word Address Buffer/ 1/16 Decoder
16 x 8 Memory Cell Array
Write And Data In Buffer
12
$\overline{WE}$
11
D_{in}
Bit Address Buffer/ 1/8 Decoder
6
7
10
A4
A5
A6

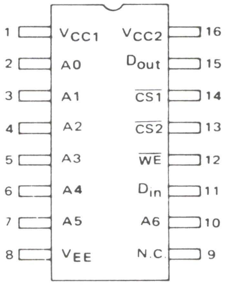
The MCM1047/10547 is a fast 128-word X 1-bit RAM. Bit selection is achieved by means of a 7-bit address, A0 through A6.

The active-low chip selects and fast chip select access time allow easy memory expansion up to 512 words without affecting system performance.

The operating mode ($\overline{CS}$ inputs low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low the chip is in the write mode—the output is low and the data present at D_{in} is stored at the selected address. With $\overline{WE}$ high the chip is in the read mode—the data state at the selected memory location is presented non-inverted at D_{out}.

- Typical Address Access Time of 10 ns
- Typical Chip Select Access Time of 4.0 ns
- 50 kΩ Input Pulldown Resistors on All Inputs
- Power Dissipation (420 mW typ @ 25°C) Decreases with Increasing Temperature
- Similar to F10405

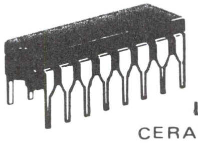
PIN ASSIGNMENT


1 V_{CC1}
2 A0
3 A1
4 A2
5 A3
6 A4
7 A5
8 V_{EE}
16 V_{CC2}
15 D_{out}
14 $\overline{CS1}$
13 $\overline{CS2}$
12 $\overline{WE}$
11 D_{in}
10 A6
9 N.C.

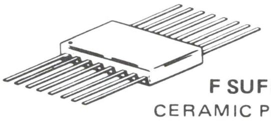
TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$*	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

*$\overline{CS} = \overline{CS1} + \overline{CS2}$ ϕ = Don't Care.



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	-55°C		0°C		+25°C		+75°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_{EE}	—	115	—	105	—	100	—	95	—	95	mAdc
Input Current High	I_{inH}	—	375	—	220	—	220	—	220	—	220	μAdc

-55°C and +125°C test values apply to MC105xx devices only.

SWITCHING CHARACTERISTICS (Note 1)

Characteristics	Symbol	MCM10147		MCM10547		Unit	Conditions
		$T_A = 0$ to $+75^\circ$C, $V_{EE} = -5.2$ Vdc ±5%		$T_A = -55$ to $+125^\circ$C, $V_{EE} = -5.2$ Vdc ±5%			
		Min	Max	Min	Max		
Read Mode						ns	Measured from 50% of input to 50% of output. See Note 2.
Chip Select Access Time	t_{ACS}	2.0	8.0	*	*		
Chip Select Recovery Time	t_{RCS}	2.0	8.0	*	*		
Address Access Time	t_{AA}	5.0	15	*	*		
Write Mode						ns	t_{WSA} = 4.0 ns Measured at 50% of input to 50% of output. t_W = 8.0 ns.
Write Pulse Width	t_W	8.0	—	*	—		
Data Setup Time Prior to Write	t_{WSD}	1.0	—	*	—		
Data Hold Time After Write	t_{WHD}	3.0	—	*	—		
Address Setup Time Prior to Write	t_{WSA}	4.0	—	*	—		
Address Hold Time After Write	t_{WHA}	3.0	—	*	—		
Chip Select Setup Time Prior to Write	t_{WSCS}	1.0	—	*	—		
Chip Select Hold Time After Write	t_{WHCS}	1.0	—	*	—		
Write Disable Time	t_{WS}	2.0	8.0	*	*		
Write Recovery Time	t_{WR}	2.0	8.0	*	*		
Rise and Fall Time	t_r, t_f	1.5	5.0	*	*	ns	Measured between 20% and 80% points.
Capacitance						pF	Measured with a pulse technique.
Input Capacitance	C_{in}	—	5.0	—	*		
Output Capacitance	C_{out}	—	8.0	—	*		

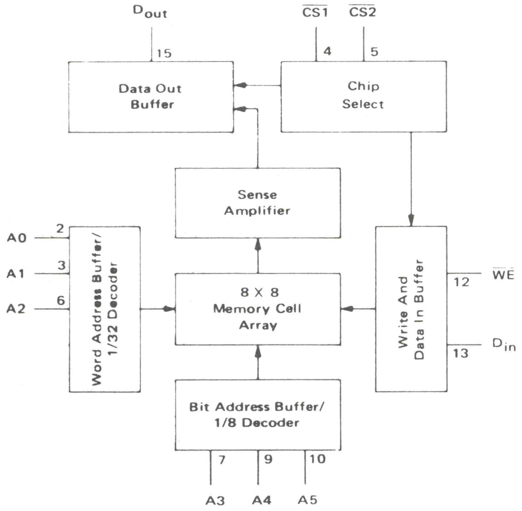
NOTES: 1. Test circuit characteristics: R_T = 50 Ω, MCM10147; 100 Ω, MCM10547.
$C_L \leqslant 5.0$ pF (including jig and stray capacitance).
Delay should be derated 30 ps/pF for capacitive load up to 50 pF.
2. The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
3. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.

*To be determined; contact your Motorola representative for up-to-date information.

MOTOROLA

MCM10148/MCM10548

64 X 1-BIT RANDOM ACCESS MEMORY



D_{out}
15
Data Out Buffer
$\overline{CS1}$
$\overline{CS2}$
4
5
Chip Select
Sense Amplifier
A0
A1
A2
2
3
6
Word Address Buffer/ 1/32 Decoder
8 X 8 Memory Cell Array
Write And Data In Buffer
12
$\overline{WE}$
13
D_{in}
Bit Address Buffer/ 1/8 Decoder
7
9
10
A3
A4
A5

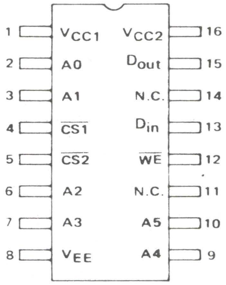
The MCM10148/10548 is a fast 64-word X 1-bit RAM. Bit selection is achieved by means of a 6-bit address, A0 through A5.

The active-low chip selects and fast chip select access time allow easy memory expansion up to 256 words without affecting system performance.

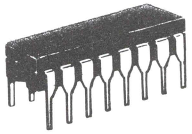
The operating mode ($\overline{CS}$ inputs low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low the chip is in the write mode—the output is low and the data present at D_{in} is stored at the selected address. With $\overline{WE}$ high the chip is in the read mode—the data state at the selected memory location is presented non-inverted at D_{out}.

- Typical Address Access Time of 10 ns
- Typical Chip Select Access Time of 4.0 ns
- 50 kΩ Input Pulldown Resistors on All Inputs
- Power Dissipation (420 mW typ @ 25°C) Decreases with Increasing Temperature

PIN ASSIGNMENT



1 V_{CC1}
2 A0
3 A1
4 $\overline{CS1}$
5 $\overline{CS2}$
6 A2
7 A3
8 V_{EE}
16 V_{CC2}
15 D_{out}
14 N.C.
13 D_{in}
12 $\overline{WE}$
11 N.C.
10 A5
9 A4

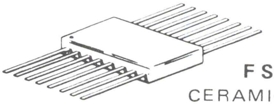


L SUFFIX
CERAMIC PACKAGE
CASE 620

TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$*	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

*$\overline{CS} = \overline{CS1} + \overline{CS2} + \overline{CS3}$ ϕ = Don't Care.



F SUFFIX
CERAMIC PACKAGE
CASE 650

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	-55°C		0°C		+25°C		+75°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_{EE}	–	115	–	105	–	100	–	95	–	95	mAdc
Input Current High	I_{inH}	–	375	–	220	–	220	–	220	–	220	μAdc

-55°C and +125°C test values apply to MC105xx devices only.

SWITCHING CHARACTERISTICS (Note 1)

Characteristics	Symbol	MCM10148 T_A = 0 to +75°C, V_{EE} = −5.2 Vdc ±5%		MCM10548 T_A = −55 to +125°C, V_{EE} = −5.2 Vdc ±5%		Unit	Conditions
		Min	Max	Min	Max		
Read Mode						ns	Measured from 50% of input to 50% of output. See Note 2.
Chip Select Access Time	t_{ACS}	–	7.5	–	*		
Chip Select Recovery Time	t_{RCS}	–	7.5	–	*		
Address Access Time	t_{AA}	–	15	–	*		
Write Mode						ns	t_{WSA} = 5.0 ns Measured at 50% of input to 50% of output. t_W = 8.0 ns.
Write Pulse Width	t_W	8.0	–	*	–		
Data Setup Time Prior to Write	t_{WSD}	3.0	–	*	–		
Data Hold Time After Write	t_{WHD}	2.0	–	*	–		
Address Setup Time Prior to Write	t_{WSA}	5.0	–	*	–		
Address Hold Time After Write	t_{WHA}	3.0	–	*	–		
Chip Select Setup Time Prior to Write	t_{WSCS}	3.0	–	*	–		
Chip Select Hold Time After Write	t_{WHCS}	0	–	*	–		
Write Disable Time	t_{WS}	2.0	7.5	*	*		
Write Recovery Time	t_{WR}	2.0	7.5	*	*		
Rise and Fall Time	t_r, t_f	1.5	5.0	*	*	ns	Measured between 20% and 80% points.
Capacitance						pF	Measured with a pulse technique.
Input Capacitance	C_{in}	–	5.0	–	*		
Output Capacitance	C_{out}	–	8.0	–	*		

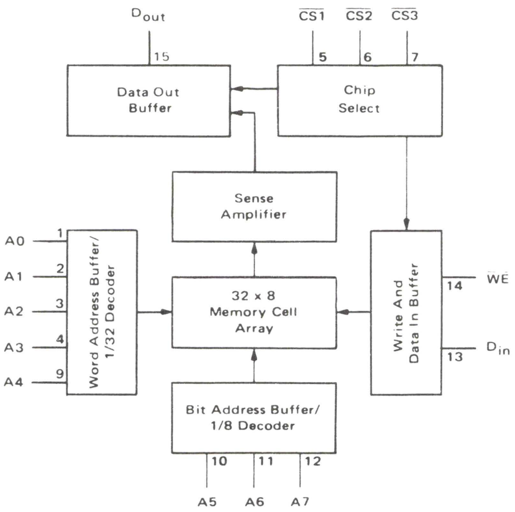
NOTES: 1. Test circuit characteristics: R_T = 50 Ω, MCM10148; 100 Ω, MCM10548.
$C_L \leqslant$ 5.0 pF (including jig and stray capacitance)
Delay should be derated 30 ps/pF for capacitive load up to 50 pF.
2. The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
3. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.

*To be determined; contact your Motorola representative for up-to-date information.

MOTOROLA

MCM10152/MCM10552

256 X 1-BIT RANDOM ACCESS MEMORY



Dout
15
CS1
CS2
CS3
5
6
7
Data Out Buffer
Chip Select
Sense Amplifier
A0
A1
A2
A3
A4
1
2
3
4
9
Word Address Buffer/ 1/32 Decoder
32 x 8 Memory Cell Array
Write And Data In Buffer
14
WE
13
Din
Bit Address Buffer/ 1/8 Decoder
10
11
12
A5
A6
A7

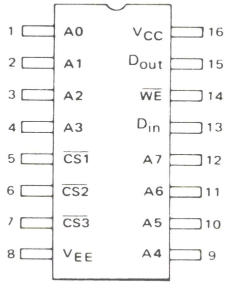
The MCM10152/10552 is a 256-word X 1-bit RAM. Bit selection is achieved by means of an 8-bit address A0 through A7.

The active-low chip select allows memory expansion up to 2048 words. The fast chip select access time allows memory expansion without affecting system performance.

The operating mode of the RAM ($\overline{CS}$ inputs low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low the chip is in the write mode—the output is low and the data present at D_{in} is stored at the selected address. With $\overline{WE}$ high the chip is in the read mode—the data state at the selected memory location is presented non-inverted at D_{out}.

- Typical Address Access Time = 11 ns
- Typical Chip Select Access Time = 4.0 ns
- 50 kΩ Input Pulldown Resistors on All Inputs
- Power Dissipation (570 mW typ @ 25°C) Decreases with Increasing Temperature
- Pin-for-Pin Compatible with F10410/10414

PIN ASSIGNMENT

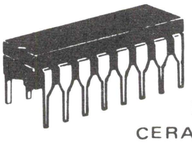


1 A0
2 A1
3 A2
4 A3
5 CS1
6 CS2
7 CS3
8 VEE
16 VCC
15 Dout
14 WE
13 Din
12 A7
11 A6
10 A5
9 A4

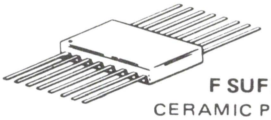
TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$*	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	φ	Q
Disabled	H	φ	φ	L

*$\overline{CS} = \overline{CS1} + \overline{CS2} + \overline{CS3}$ φ = Don't Care.



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	-55°C		0°C		+25°C		+75°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_{EE}	–	140	–	135	–	130	–	125	–	125	mAdc
Input Current High	I_{inH}	–	375	–	220	–	220	–	220	–	220	μAdc

-55°C and +125°C test values apply to MC105xx devices only.

SWITCHING CHARACTERISTICS (Note 1)

Characteristics	Symbol	MCM10152		MCM10552		Unit	Conditions
		T_A = 0 to +75°C, V_{EE} = −5.2 Vdc ±5%		T_A = −55 to +125°C, V_{EE} = −5.2 Vdc ±5%			
		Min	Max	Min	Max		
Read Mode							Measured from 50% of input to 50% of output. See Note 2.
Chip Select Access Time	t_{ACS}	2.0	7.5	*	*		
Chip Select Recovery Time	t_{RCS}	2.0	7.5	*	*		
Address Access Time	t_{AA}	7.0	15	*	*		
Write Mode						ns	t_{WSA} = 5.0 ns Measured at 50% of input to 50% of output. t_W = 10 ns.
Write Pulse Width	t_W	10	–	*	–		
Data Setup Time Prior to Write	t_{WSD}	2.0	–	*	–		
Data Hold Time After Write	t_{WHD}	2.0	–	*	–		
Address Setup Time Prior to Write	t_{WSA}	5.0	–	*	–		
Address Hold Time After Write	t_{WHA}	3.0	–	*	–		
Chip Select Setup Time Prior to Write	t_{WSCS}	2.0	–	*	–		
Chip Select Hold Time After Write	t_{WHCS}	2.0	–	*	–		
Write Disable Time	t_{WS}	2.5	7.5	*	*		
Write Recovery Time	t_{WR}	2.5	7.5	*	*		
Rise and Fall Time	t_r, t_f	1.5	5.0	*	*	ns	Measured between 20% and 80% points.
Capacitance						pF	Measured with a pulse technique.
Input Capacitance	C_{in}	–	5.0	–	*		
Output Capacitance	C_{out}	–	8.0	–	*		

NOTES: 1. Test circuit characteristics: R_T = 50 Ω, MCM10152; 100 Ω, MCM10552.
$C_L \leq 5.0$ pF (including jig and stray capacitance).
Delay should be derated 30 ps/pF for capacitive load up to 50 pF.
2. The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
3. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.

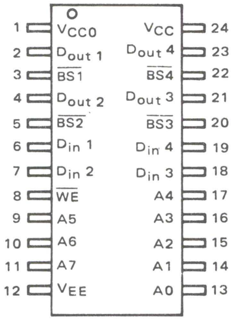
*To be determined; contact your Motorola representative for up-to-date information.

MCM10422

256 X 4-BIT RANDOM ACCESS MEMORY

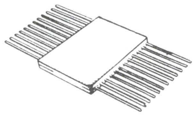
MOTOROLA

PIN ASSIGNMENT

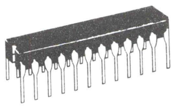

1 V_{CCO}
2 D_{out} 1
3 $\overline{BS1}$
4 D_{out} 2
5 $\overline{BS2}$
6 D_{in} 1
7 D_{in} 2
8 $\overline{WE}$
9 A5
10 A6
11 A7
12 V_{EE}
24 V_{CC}
23 D_{out} 4
22 $\overline{BS4}$
21 D_{out} 3
20 $\overline{BS3}$
19 D_{in} 4
18 D_{in} 3
17 A4
16 A3
15 A2
14 A1
13 A0

PIN DESIGNATION

$\overline{BS1}$ - $\overline{BS4}$		Block Select Inputs
A0 - A7		Address Inputs
D_{in} 1 - D_{in} 4		Data Inputs
D_{out} 1 - D_{out} 4		Data Outputs
$\overline{WE}$ -		Write Enable Input



F SUFFIX
CERAMIC PACKAGE
CASE 652



L SUFFIX
CERAMIC PACKAGE
CASE 748

The MCM10422 is a high speed 1024-bit Read/Write Random Access Memory organized 256 words by 4 bits. Four independent active-low Block Selects permit use in 1024 × 1 and 512 × 2 bit applications. The device has full address decoding on chip, separate data inputs, non-inverting data outputs, and an active-low Write Enable.

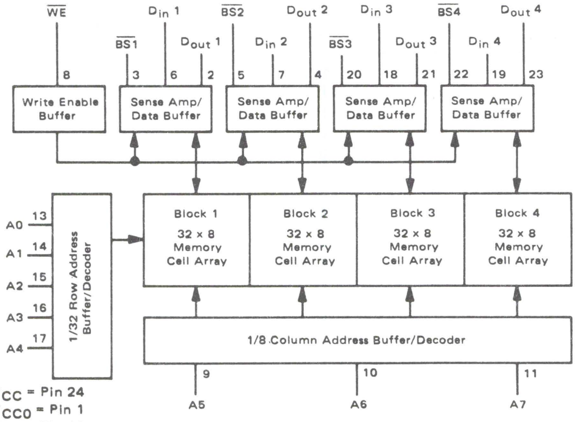
The MCM10422 is designed for high speed scratch pad, control, cache, and buffer storage applications. The device is available in a space-saving 24-pin CERDIP, or in the standard 24-pin flatpack (12 pins on each side).

- Typical Address Access of 12 ns
- Typical Power Dissipation of 850 mW
- Power Dissipation Decreases with Increasing Temperature
- Fully Compatible with MECL 10,000
- Operating Temperature Range 0°C to 75°C
- Organized 256 Words by 4 Bits
- Four Independent Block Selects
- Emitter-Follower Outputs Permits Full Wire-OR'ing

TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{BS}_n$	$\overline{WE}$	D_{in} n	D_{out} n
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Block Disabled	H	ϕ	ϕ	L

ϕ Don't Care NOTE: Blocks Enable Independently


$\overline{WE}$
8
Write Enable Buffer
$\overline{BS1}$
3
D_{in} 1
6
D_{out} 1
2
Sense Amp/ Data Buffer
$\overline{BS2}$
5
D_{in} 2
7
D_{out} 2
4
Sense Amp/ Data Buffer
$\overline{BS3}$
20
D_{in} 3
18
D_{out} 3
21
Sense Amp/ Data Buffer
$\overline{BS4}$
22
D_{in} 4
19
D_{out} 4
23
Sense Amp/ Data Buffer
Block 1 32 x 8 Memory Cell Array
Block 2 32 x 8 Memory Cell Array
Block 3 32 x 8 Memory Cell Array
Block 4 32 x 8 Memory Cell Array
A0 13
A1 14
A2 15
A3 16
A4 17
1/32 Row Address Buffer/Decoder
1/8 Column Address Buffer/Decoder
9 A5
10 A6
11 A7

V_{CC} = Pin 24
V_{CCO} = Pin 1
V_{EE} = Pin 12

FUNCTIONAL DESCRIPTION:

This device is a 256 x 4-bit RAM. Word selection is achieved by means of an 8-bit address, A0-A7.

The operating mode of each block ($\overline{BS}_n$ input low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low, the block is in the write mode, the output D_{out} n is low and the data state present at D_{in} n is stored at the selected address in block n. With $\overline{WE}$ high, the block is in the read mode and the data stored at the selected memory location will be presented non-inverted at D_{out} n.

The independent, active-low Block Selects and the wire-OR capability of the emitter follower outputs permit use as a 1024 x 1 or 512 x 2-bit RAM. For example, for use as a 1024 x 1-bit RAM tie all D_{in} inputs together to form a single D_{in}, wire-OR the D_{out} lines together to form a single D_{out} line, and drive the Block Selects with a 1-of-4 low decoder.

Package	θ_{JA} (Junction to Ambient) Blown	Still	θ_{JC} (Junction to Case)
L Suffix	35°C/W	55°C/W	15°C/W
F Suffix	35°C/W	52°C/W	10°C/W

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (V_{CC} = 0)	V_{EE}	-8 to 0	Vdc
Base Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	Vdc
Output Source Current – Continuous – Surge	I_O	< 50 < 100	mAdc
Junction Operating Temperature	T_J	< 165	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

Test Temperature	DC TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
0°C	-0.840	-1.870	-1.145	-1.490	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+75°C	-0.720	-1.830	-1.045	-1.450	-5.2

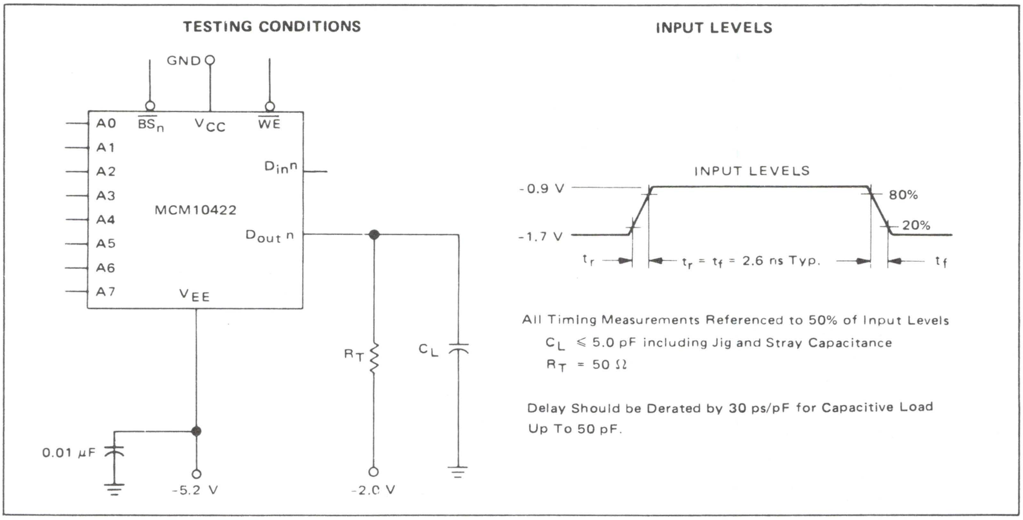
ELECTRICAL CHARACTERISTICS

Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

DC Characteristics	Symbol	MCM10422 Test Limits 0°C Min	Max	+25°C Min	Max	+75°C Min	Max	Unit	Conditions
Power Supply Drain Current	I_{EE}	—	200	—	195	—	185	mAdc	Typ I_{EE} @ 25°C = 160 mA All outputs and inputs open. Measure pin 12.
Input Current High	$I_{in}H$	—	220	—	220	—	220	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IH(max)}$
Input Current Low (Block Selects)	$I_{in}L$	0.5	—	0.5	—	0.3	—	μAdc	Test one input at a time, all other inputs are open.
Input Current Low*	$I_{in}L$	-50	—	-50	—	-50	—	μAdc	$V_{in} = V_{IL(min)}$
Logic "1" Output Voltage	V_{OH}	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	Load 50 Ω to -2.0 V
Logic "0" Output Voltage	V_{OL}	-1.870	-1.665	-1.850	-1.650	-1.830	-1.625	Vdc	
Logic "1" Threshold Voltage	V_{OHA}	-1.020	—	-0.980	—	-0.920	—	Vdc	Threshold testing is performed and guaranteed on one input at a time. $V_{in} = V_{IHA}$ or V_{ILA}. Load 50 Ω to -2.0 V.
Logic "0" Threshold Voltage	V_{OLA}	—	-1.645	—	-1.630	—	-1.605	Vdc	

*Minimum limit equals the maximum negative current the driving circuitry will be required to sink.

FIGURE 1 – SWITCHING TEST CIRCUIT AND WAVEFORMS


TESTING CONDITIONS
GND
A0
A1
A2
A3
A4
A5
A6
A7
$\overline{BS}_n$
V_{CC}
$\overline{WE}$
$D_{in}n$
MCM10422
$D_{out}n$
V_{EE}
R_T
C_L
0.01 μF
-5.2 V
-2.0 V
INPUT LEVELS
INPUT LEVELS
-0.9 V
-1.7 V
80%
20%
t_r
$t_r = t_f = 2.6$ ns Typ.
t_f

All Timing Measurements Referenced to 50% of Input Levels
$C_L \leqslant 5.0$ pF including Jig and Stray Capacitance
$R_T = 50\ \Omega$

Delay Should be Derated by 30 ps/pF for Capacitive Load Up To 50 pF.

Guaranteed with $V_{EE} = -5.2$ Vdc ± 5.0%, $T_A = 0°C$ to 75°C (see Note 1). Output Load see Figure 1.

Characteristic	Symbol	MCM10422 Test Limits		Unit	Conditions
		Min	Max		
Read Mode					See Figures 2 and 3.
Block Select Access Time	t_{ABS}	–	6.5	ns	Measured at 50% of input to 50% of output.
Block Select Recovery Time	t_{RBS}	–	6.0	ns	See Note 1.
Address Access Time	t_{AA}	–	15.0	ns	
Write Mode					See Figure 4.
Write Pulse Width (To guarantee writing)	t_W	15.0	–	ns	$t_{WSA} = 2.0$ ns. Measured at 50% of input to 50% of output.
Data Setup Time Prior to Write	t_{WSD}	1.0	–	ns	
Data Hold Time After Write	t_{WHD}	5.0	–	ns	
Address Setup Time Prior to Write	t_{WSA}	2.0	–	ns	$t_W = 15.0$ ns
Address Hold Time After Write	t_{WHA}	11.0	–	ns	
Block Select Setup Time Prior to Write	t_{WSBS}	0.0	–	ns	
Block Select Hold Time After Write	t_{WHBS}	0.0	–	ns	
Write Disable Time	t_{WS}	–	5.0	ns	
Write Recovery Time	t_{WR}	–	11.0	ns	
Rise and Fall Time					Measured between 20% and 80% points.
Output Rise and Fall Time	t_r, t_f	1.5	4.0	ns	
Capacitance					Measured with a pulse technique.
Input Lead Capacitance	C_{in}	–	8.0	pF	
Output Lead Capacitance	C_{out}	–	8.0	pF	

Notes:
(1) The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
(2) For proper use of MECL Memories in a system environment, consult: "MECL System Design Handbook."

FIGURE 2 – BLOCK SELECT ACCESS TIME

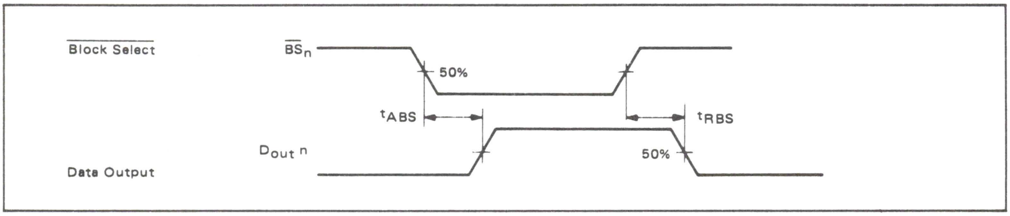

Block Select
$\overline{BS}_n$
50%
t_{ABS}
t_{RBS}
D_{out} n
50%
Data Output

FIGURE 3 – ADDRESS ACCESS TIME

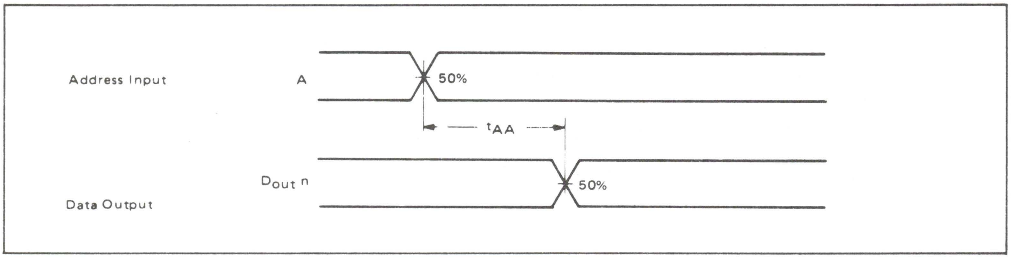
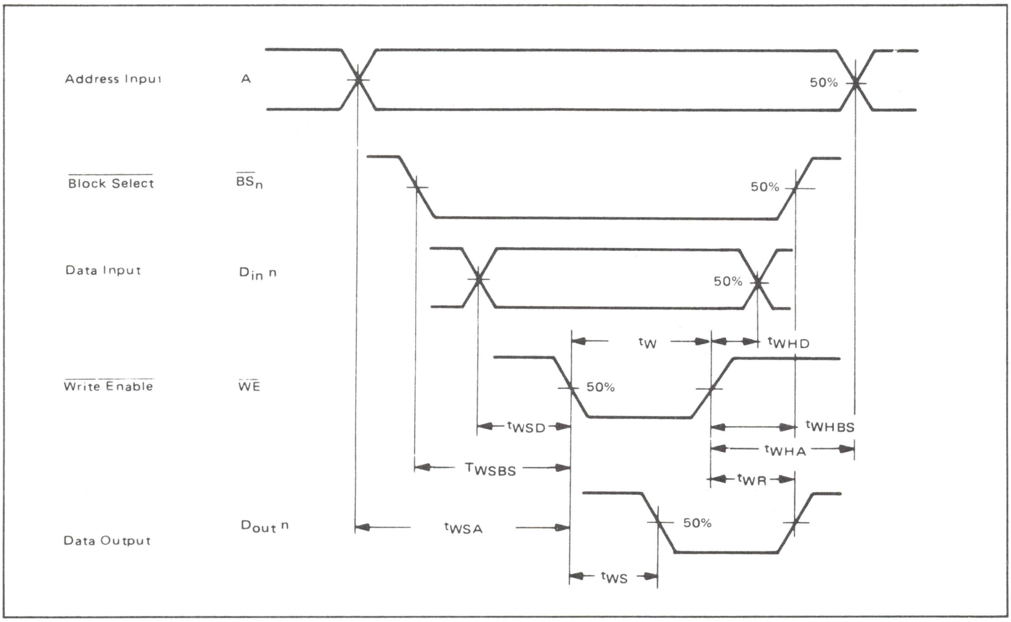

Address Input
A
50%
t_{AA}
D_{out} n
50%
Data Output

FIGURE 4 – WRITE STROBE MODE

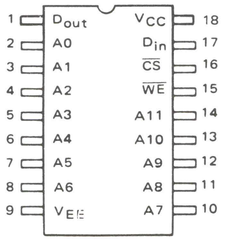

Address Input
A
50%
Block Select
$\overline{BS}_n$
50%
Data Input
D_{in} n
50%
t_W
t_{WHD}
Write Enable
$\overline{WE}$
50%
t_{WSD}
t_{WHBS}
t_{WHA}
T_{WSBS}
t_{WR}
D_{out} n
50%
Data Output
t_{WSA}
t_{WS}

MCM10470

4096 X 1-BIT
RANDOM ACCESS MEMORY

MOTOROLA

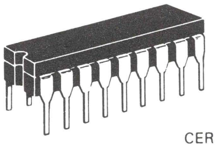
PIN ASSIGNMENT



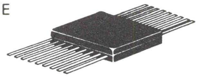
1 Dout
2 A0
3 A1
4 A2
5 A3
6 A4
7 A5
8 A6
9 VEE
18 VCC
17 Din
16 CS
15 WE
14 A11
13 A10
12 A9
11 A8
10 A7

Pin Description

$\overline{CS}$	Chip Select
A0-A11	Address Inputs
$\overline{WE}$	Write Enable
D_{in}	Data Input
D_{out}	Data Output



L SUFFIX
CERAMIC PACKAGE
CASE 726



F SUFFIX
CERAMIC PACKAGE
CASE 747

The MCM10470 is a 4096 bit Read/Write Random Access Memory organized 4096 words by 1 bit. Data is selected or stored by means of a 12-bit address (A0 through A11) decoded on the chip. The chip is designed with a separate data in line, a non-inverting data output, and an active-low chip select.

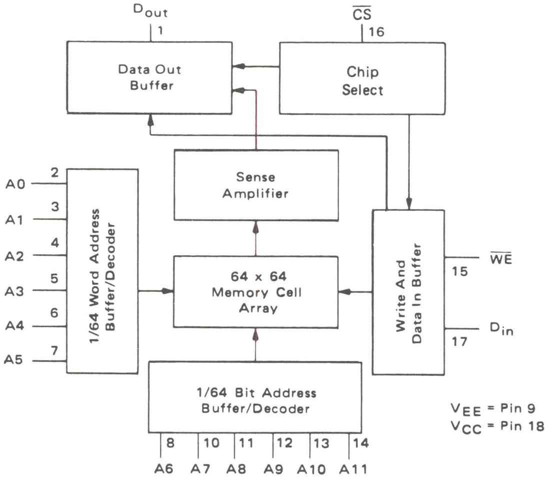
This device is designed for use in high-speed scratch pad, control, cache and buffer storage applications.

- Fully Compatible with MECL 10,000
- Pin-for-Pin Compatible with the Industry's Standard 10470
- Temperature Range of 0° to 75°C
- Emitter-Follower Output Permits Full Wire-ORing
- Power Dissipation Decreases with Increasing Temperature
- Typical Address Access of 25 ns
- Typical Chip Select Access of 10 ns

TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

ϕ = Don't Care.



Dout
1
CS
16
Data Out Buffer
Chip Select
Sense Amplifier
A0 2
A1 3
A2 4
A3 5
A4 6
A5 7
1/64 Word Address Buffer/Decoder
64 x 64 Memory Cell Array
Write And Data In Buffer
WE 15
Din 17
1/64 Bit Address Buffer/Decoder
8 10 11 12 13 14
A6 A7 A8 A9 A10 A11
VEE = Pin 9
VCC = Pin 18

FUNCTIONAL DESCRIPTION:

This device is a 4096 x 1-bit RAM. Bit selection is achieved by means of a 12-bit address, A0 to A11.

The active-low chip select is provided for memory expansion.

The operating mode of the RAM ($\overline{CS}$ input low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low, the chip is in the write mode, the output, D_{out}, is low and the data state present at D_{in} is stored at the selected address. With $\overline{WE}$ high, the chip is in the read mode and the data stored at the selected memory location will be presented non-inverted at D_{out}. (See Truth Table)

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (V_{CC} = 0)	V_{EE}	-7.0 to 0	Vdc
Base Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	Vdc
Output Source Current – Continuous – Surge	I_O	< 50 < 100	mAdc
Junction Operating Temperature	T_J	< 165	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

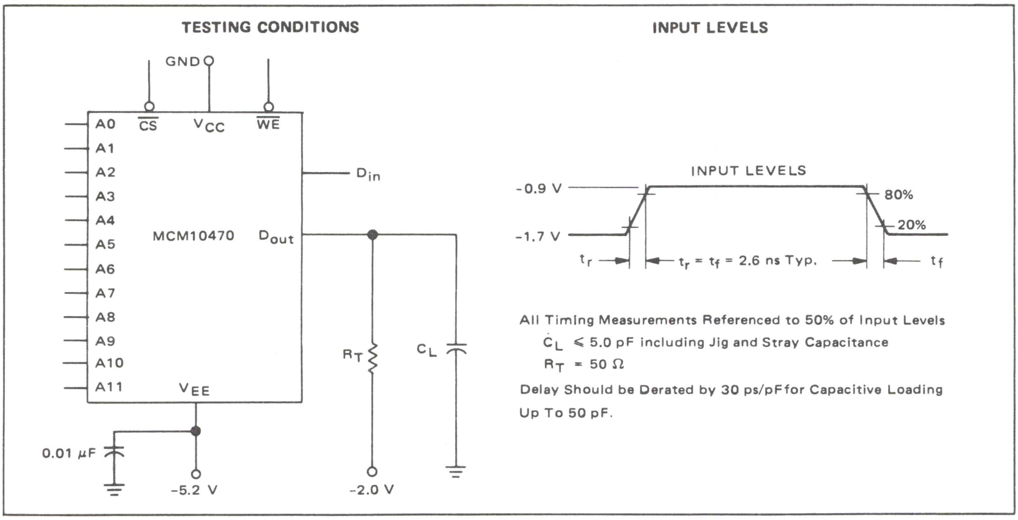
ELECTRICAL CHARACTERISTICS

Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

	DC TEST VOLTAGE VALUES (Volts)				
Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
0°C	-0.840	-1.870	-1.145	-1.490	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+75°C	-0.720	-1.830	-1.045	-1.450	-5.2

		MCM10470 Test Limits							
		0°C		+25°C		+75°C			
DC Characteristics	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Conditions**
Power Supply Drain Current	I_{EE}	–	200	–	195	–	185	mAdc	Typ I_{EE} @ 25°C = 160 mA. All outputs and inputs open. Measure pin 9.
Input Current High	I_{inH}	–	220	–	220	–	220	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IH(max)}$.
Input Current Low Chip Select	I_{inL}	0.5	–	0.5	–	0.3	–	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IL(min)}$.
Input Current Low*	I_{inL}	-50	–	-50	–	-50	–	μAdc	
Logic "1" Output Voltage	V_{OH}	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	Load 50 Ω to -2.0 V
Logic "0" Output Voltage	V_{OL}	-1.870	-1.665	-1.850	-1.650	-1.830	-1.625	Vdc	
Logic "1" Threshold Voltage	V_{OHA}	-1.020	–	-0.980	–	-0.920	–	Vdc	Threshold testing is performed and guaranteed on one input at a time. $V_{in} = V_{IHA}$ or V_{ILA}. Load 50 Ω to -2.0 V.
Logic "0" Threshold Voltage	V_{OLA}	–	-1.645	–	-1.630	–	-1.605	Vdc	

FIGURE 1 – SWITCHING TEST CIRCUIT AND WAVEFORMS


TESTING CONDITIONS
INPUT LEVELS
GND
$\overline{CS}$
V_{CC}
$\overline{WE}$
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
MCM10470
D_{in}
D_{out}
V_{EE}
R_T
C_L
0.01 µF
-5.2 V
-2.0 V
INPUT LEVELS
-0.9 V
-1.7 V
80%
20%
t_r
$t_r = t_f = 2.6$ ns Typ.
t_f

All Timing Measurements Referenced to 50% of Input Levels

$C_L \leqslant 5.0$ pF including Jig and Stray Capacitance

$R_T = 50\ \Omega$

Delay Should be Derated by 30 ps/pF for Capacitive Loading Up To 50 pF.

Guaranteed with $V_{EE} = -5.2$ Vdc ± 5.0%, $T_A = 0^{\circ}C$ to $75^{\circ}C$ (see Note 1). Output Load see Figure 1.

Characteristic	Symbol	MCM10470 Test Limits		Unit	Conditions
		Min	Max		
Read Mode					See Figures 2 and 3.
Chip Select Access Time	t_{ACS}	–	15	ns	Measured at 50% of input to 50% of output.
Chip Select Recovery Time	t_{RCS}	–	15	ns	
Address Access Time	t_{AA}	–	35	ns	
Write Mode					See Figure 4.
Write Pulse Width (To guarantee writing)	t_W	25	–	ns	$t_{WSA} = 8.0$ ns. Measured at 50% of input to 50% of output.
Data Setup Time Prior to Write	t_{WSD}	5.0	–	ns	
Data Hold Time After Write	t_{WHD}	5.0	–	ns	
Address Setup Time Prior to Write	t_{WSA}	10	–	ns	$t_W = 25$ ns
Address Hold Time After Write	t_{WHA}	5.0	–	ns	
Chip Select Setup Time Prior to Write	t_{WSCS}	5.0	–	ns	
Chip Select Hold Time After Write	t_{WHCS}	5.0	–	ns	
Write Disable Time	t_{WS}	–	15	ns	
Write Recovery Time	t_{WR}	–	20	ns	
Rise and Fall Time					Measured between 20% and 80% points.
Output Rise and Fall Time	t_r, t_f	–	4.0	ns	
Capacitance		Typ			Measured with a pulse technique.
Input Lead Capacitance	C_{in}	4.0		pF	
Output Lead Capacitance	C_{out}	7.0		pF	

Notes:

(1) The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.

(2) For proper use of MECL Memories in a system environment, consult: "MECL System Design Handbook."

FIGURE 2 – CHIP SELECT ACCESS TIME

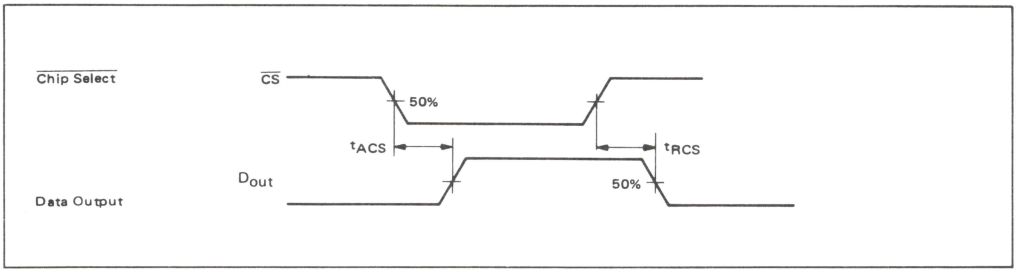

Chip Select
CS
50%
tACS
tRCS
Dout
50%
Data Output

FIGURE 3 – ADDRESS ACCESS TIME

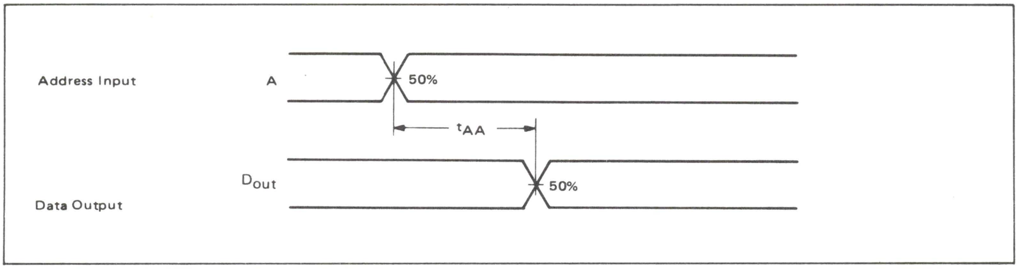
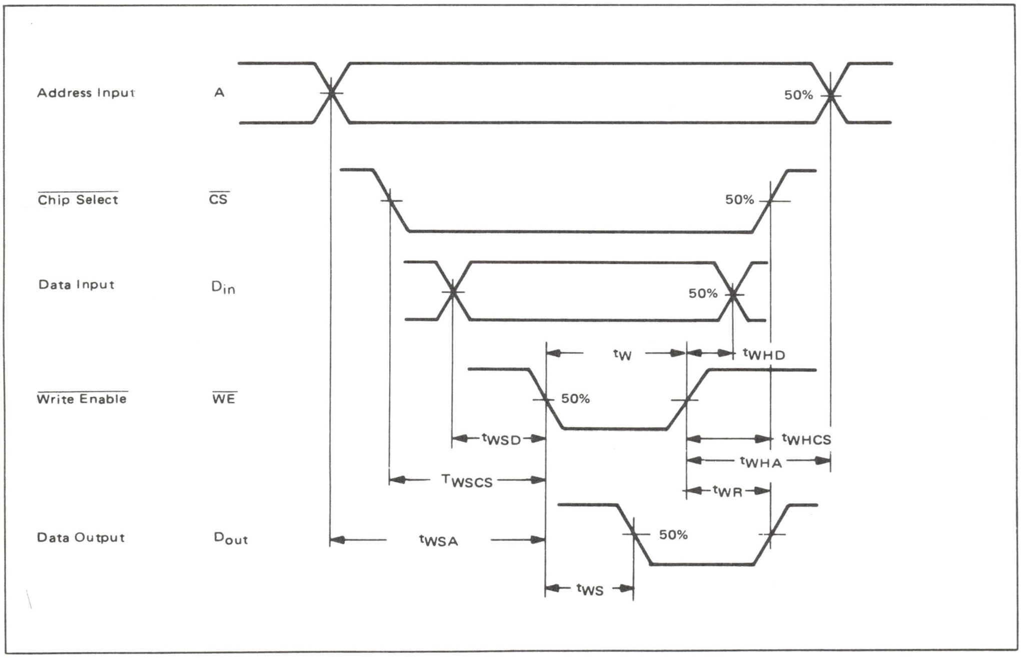
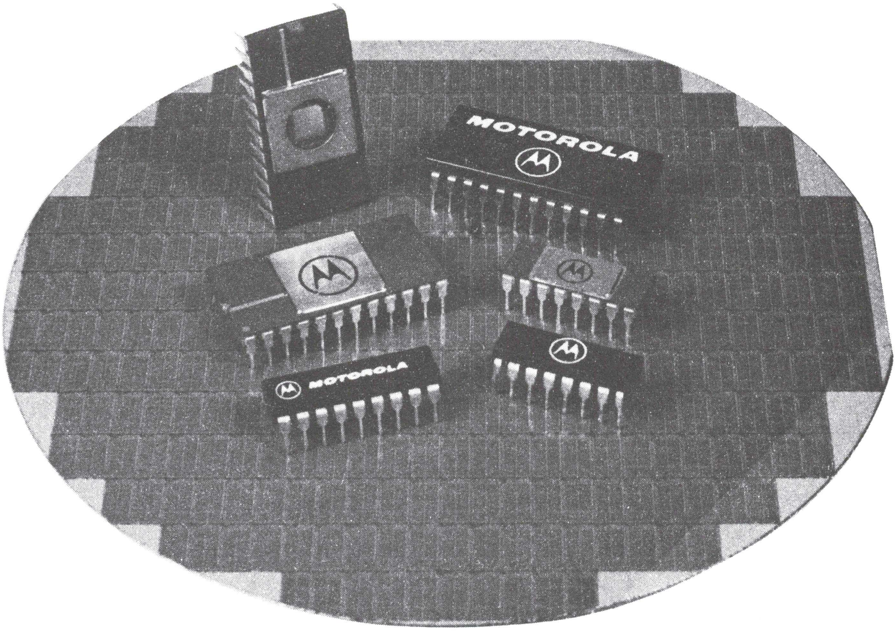

Address Input
A
50%
tAA
Dout
50%
Data Output

FIGURE 4 – WRITE STROBE MODE


Address Input
A
50%
Chip Select
CS
50%
Data Input
Din
50%
tW
tWHD
Write Enable
WE
50%
tWSD
tWHCS
tWHA
TWSCS
tWR
Data Output
Dout
tWSA
50%
tWS

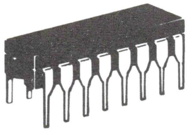

MOTOROLA
MOTOROLA

MECL PROM

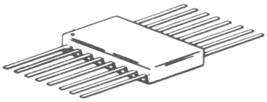
MOTOROLA

MCM10139/MCM10539

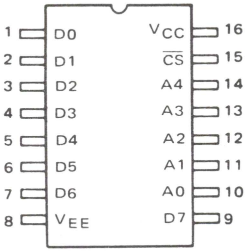
32 x 8-BIT PROGRAMMABLE READ-ONLY MEMORY



L SUFFIX
CERAMIC PACKAGE
CASE 620



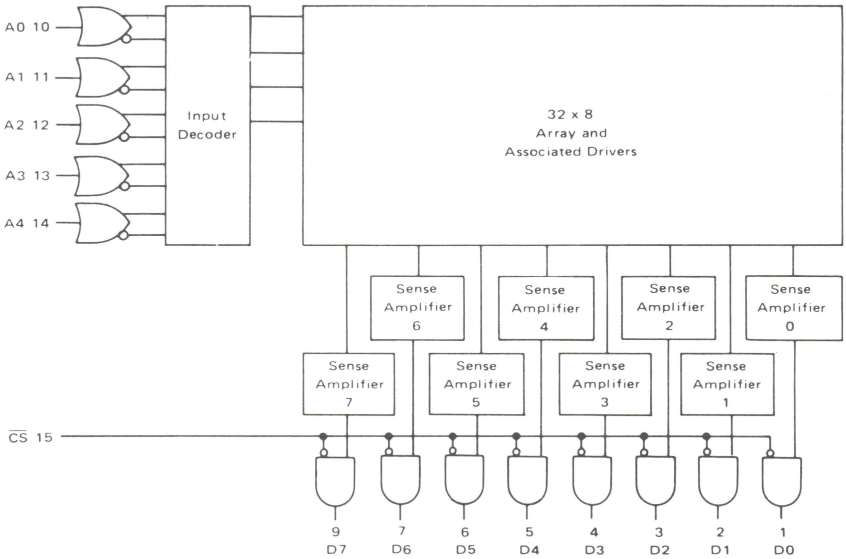
F SUFFIX
CERAMIC PACKAGE
CASE 650


1 D0
2 D1
3 D2
4 D3
5 D4
6 D5
7 D6
8 VEE
16 VCC
15 CS
14 A4
13 A3
12 A2
11 A1
10 A0
9 D7

The MCM10139/10539 is a 256-bit field programmable read only memory (PROM). Prior to programming, all stored bits are at logic 0 (low) levels. The logic state of each bit can then be changed by on-chip programming circuitry. The memory has a single negative logic chip enable. When the chip is disabled ($\overline{CS}$ = high), all outputs are forced to a logic 0 (low).

- Typical Address Access Time = 15 ns
- Typical Chip Select Access Time = 10 ns
- 50 kΩ Input Pulldown Resistors on all inputs
- Power Dissipation (520 mW typ @ 25°C) Decreases with Increasing Temperature

BLOCK DIAGRAM


A0 10
A1 11
A2 12
A3 13
A4 14
Input Decoder
32 x 8 Array and Associated Drivers
Sense Amplifier 6
Sense Amplifier 4
Sense Amplifier 2
Sense Amplifier 0
Sense Amplifier 7
Sense Amplifier 5
Sense Amplifier 3
Sense Amplifier 1
CS 15
9 D7
7 D6
6 D5
5 D4
4 D3
3 D2
2 D1
1 D0

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	-55°C		-0°C		+25°C		+75°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_{EE}	—	160	—	150	—	145	—	140	—	160	mAdc
Input Current High	I_{inH}	—	450	—	265	—	265	—	265	—	265	μAdc
Logic "0" Output Voltage	V_{OL}											Vdc
MCM10139		—	—	-2.010	-1.665	-1.990	-1.650	-1.970	-1.625	—	—	
MCM10539		-2.060	-1.655	—	—	-1.990	-1.620	—	—	-1.960	-1.545	

SWITCHING CHARACTERISTICS (Note 1)

Characteristic	Symbol	MCM10139 (V_{EE} = −5.2 Vdc ±5%; T_A = 0°C to +75°C)	MCM10539 (V_{EE} = −5.2 Vdc ± 5 %; T_A = −55°C to +125°C)	Conditions
Chip Select Access Time	t_{ACS}	15 ns Max	*	Measured from 50% of input to 50% of output. See Note 2
Chip Select Recovery Time	t_{RCS}	15 ns Max	*	
Address Access Time	t_{AA}	20 ns Max	*	
Rise and Fall Time	t_r, t_f	3.0 ns Typ	*	Measured between 20% and 80% points.
Input Capacitance	C_{in}	5.0 pF Max	*	Measured with a pulse technique.
Output Capacitance	C_{out}	8.0 pF Max	*	

NOTES:
1. Test circuit characteristics: R_T = 50 Ω, MCM10139; 100 Ω, MCM10539. $C_L \leqslant 5.0$ pF including jig and stray capacitance. For Capacitance Loading $\leqslant$50 pF, delay should be derated by 30 ps/pF.
2. The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
3. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.

*To be determined; contact your Motorola representative for up-to-date information.

FIGURE 1 — MANUAL PROGRAMMING CIRCUIT

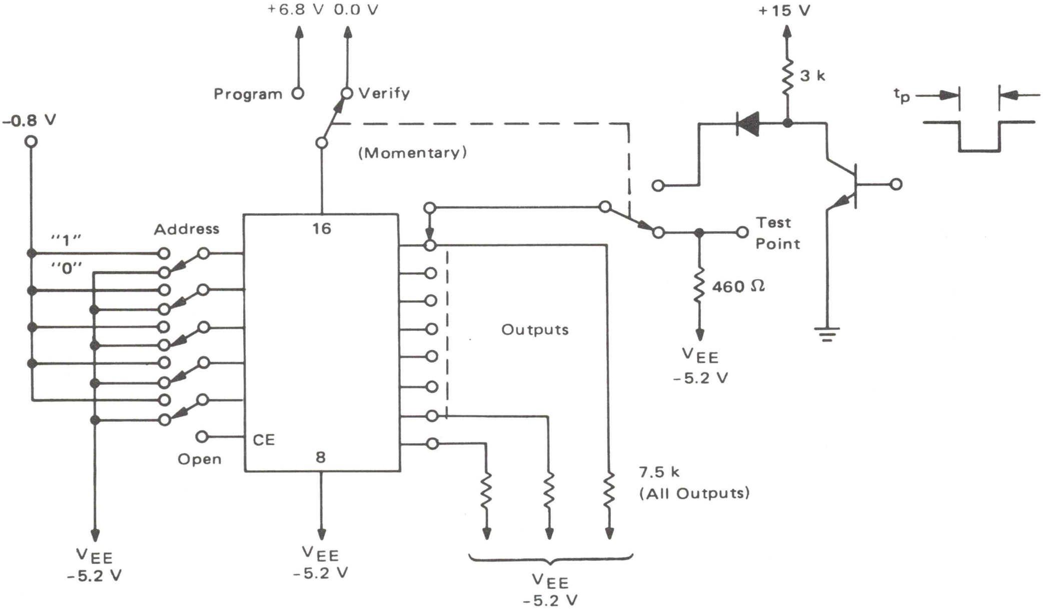
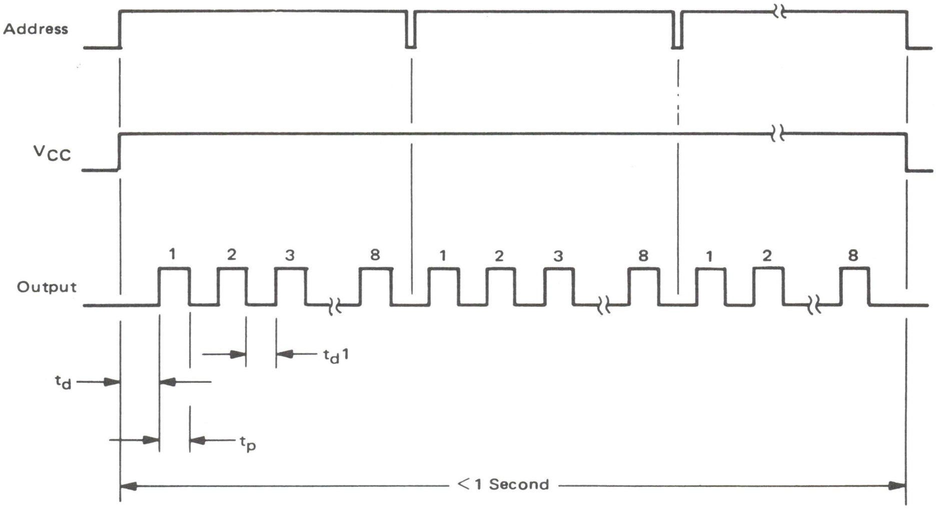

+6.8 V
0.0 V
Program
Verify
(Momentary)
-0.8 V
"1"
"0"
Address
16
CE
Open
8
Outputs
Test Point
460 Ω
+15 V
3 k
tp
7.5 k (All Outputs)
VEE -5.2 V
VEE -5.2 V
VEE -5.2 V
VEE -5.2 V

FIGURE 2 — AUTOMATIC PROGRAMMING CIRCUIT


Address
VCC
Output
1
2
3
8
1
2
3
8
1
2
8
td
td1
tp
< 1 Second

RECOMMENDED PROGRAMMING PROCEDURE*

The MCM10139 is shipped with all bits at logical "0" (low). To write logical "1s", proceed as follows.

MANUAL (See Figure 1)

Step 1 Connect V_{EE} (Pin 8) to -5.2 V and V_{CC} (Pin 16) to 0.0 V. Address the word to be programmed by applying -1.2 to -0.6 volts for a logic "1" and -5.2 to -4.2 volts for a logic "0" to the appropriate address inputs.

Step 2 Raise V_{CC} (Pin 16) to +6.8 volts.

Step 3 After V_{CC} has stabilized at +6.8 volts (including any ringing which may be present on the V_{CC} line), apply a current pulse of 2.5 mA to the output pin corresponding to the bit to be programmed to a logic "1".

Step 4 Return V_{CC} to 0.0 Volts.

CAUTION

To prevent excessive chip temperature rise, V_{CC} should not be allowed to remain at +6.8 volts for more than 1 second.

Step 5 Verify that the selected bit has programmed by connecting a 460 Ω resistor to -5.2 volts and measuring the voltage at the output pin. If a logic "1" is not detected at the output, the procedure should be repeated once. During verification V_{IH} should be -1.0 to -0.6 volts.

Step 6 If verification is positive, proceed to the next bit to be programmed.

AUTOMATIC (See Figure 2)

Step 1 Connect V_{EE} (Pin 8) to -5.2 volts and V_{CC} (Pin 16) to 0.0 volts. Apply the proper address data and raise V_{CC} (Pin 16) to +6.8 volts.

Step 2 After a minimum delay of 100 µs and a maximum delay of 1.0 ms, apply a 2.5 mA current pulse to the first bit to be programmed (0.1 ⩽ PW ⩽ 1 ms).

Step 3 Repeat Step 2 for each bit of the selected word specified as a logic "1". (Program only one bit at a time. The delay between output programming pulses should be equal to or less than 1.0 ms.)

Step 4 After all the desired bits of the selected word have been programmed, change address data and repeat Steps 2 and 3.

NOTE: If all the maximum times listed above are maintained, the entire memory will program in less than 1 second. Therefore, it would be permissible for V_{CC} to remain at +6.8 volts during the entire programming time.

Step 5 After stepping through all address words, return V_{CC} to 0.0 volts and verify that each bit has programmed. If one or more bits have not programmed, repeat the entire procedure once. During verification V_{IH} should be -1.0 to -0.6 volts.

*NOTE: For devices that program incorrectly—return serialized units with individual truth tables. Noncompliance voids warranty.

PROGRAMMING SPECIFICATIONS

Characteristic	Symbol	Limits			Units	Conditions
		Min	Typ	Max		
Power Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	Vdc	
To Program	V_{CCP}	+6.04	+6.8	+7.56	Vdc	
To Verify	V_{CCV}	0	0	0	Vdc	
Programming Supply Current	I_{CCP}	–	200	600	mA	V_{CC} = +6.8 Vdc
Address Voltage						
Logical "1"	V_{IH} Program	-1.2	–	-0.6	Vdc	
	V_{IH} Verify	-1.0	–	-0.6	Vdc	
Logical "0"	V_{IL}	-5.2	–	-4.2	Vdc	
Maximum Time at V_{CC} = V_{CCP}	–	–	–	1.0	sec	
Output Programming Current	I_{OP}	2.0	2.5	3.0	mAdc	
Output Program Pulse Width	t_p	0.5	–	1.0	ms	
Output Pulse Rise Time	–	–	–	10	µs	
Programming Pulse Delay (1)						
Following V_{CC} change	t_d	0.1	–	1.0	ms	
Between Output Pulses	t_d1	0.01	–	1.0	ms	

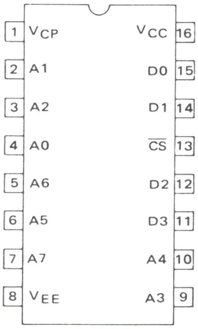
NOTE 1. Maximum is specified to minimize the amount of time V_{CC} is at +6.8 volts.

MOTOROLA

MCM10149/MCM10549

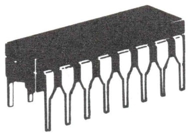
256 X 4-BIT PROGRAMMABLE READ-ONLY MEMORY

PIN ASSIGNMENT

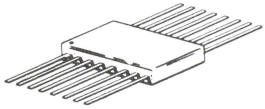

1 VCP
2 A1
3 A2
4 A0
5 A6
6 A5
7 A7
8 VEE
VCC 16
D0 15
D1 14
CS 13
D2 12
D3 11
A4 10
A3 9

The MCM10149/10549 is a 256-word X 4-bit field programmable read only memory (PROM). Prior to programming, all stored bits are at logic 1 (high) levels. The logic state of each bit can then be changed by on-chip programming circuitry. The memory has a single negative logic chip enable. When the chip is disabled ($\overline{CS}$ = high), all outputs are forced to a logic 0 (low).

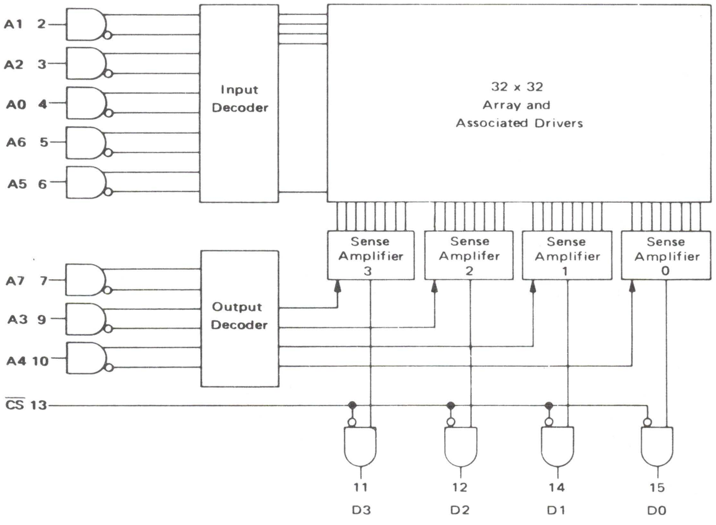
- Typical Address Access Time of 20 ns
- Typical Chip Select Access Time of 8.0 ns
- 50 kΩ Input Pulldown Resistors on All Inputs
- Power Dissipation (540 mW typ @ 25°C) Decreases with Increasing Temperature



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650


A1 2
A2 3
A0 4
A6 5
A5 6
Input Decoder
32 x 32 Array and Associated Drivers
Sense Amplifier 3
Sense Amplifer 2
Sense Amplifier 1
Sense Amplifier 0
A7 7
A3 9
A4 10
Output Decoder
CS 13
11 D3
12 D2
14 D1
15 D0

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	-55°C		0°C		+25°C		+75°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_{EE}	–	140	–	135	–	130	–	125	–	125	mAdc
Input Current High	I_{inH}	–	450	–	265	–	265	–	265	–	265	μAdc

-55°C and +125°C test values apply to MC105xx devices only.

SWITCHING CHARACTERISTICS (Note 1)

Characteristics	Symbol	MCM10149		MCM10549		Unit	Conditions
		T_A = 0 to +75°C, V_{EE} = −5.2 Vdc ±5%		T_A = −55 to +125°C, V_{EE} = −5.2 Vdc ±5%			
		Min	Max	Min	Max		
Read Mode						ns	Measured from 50% of input to 50% of output. See Note 1.
Chip Select Access Time	t_{ACS}	2.0	10	*	*		
Chip Select Recovery Time	t_{RCS}	2.0	10	*	*		
Address Access Time	t_{AA}	7.0	25	*	*		
Rise and Fall Time	t_r, t_f	1.5	7.0	*	*	ns	Measured between 20% and 80% points.
Capacitance						pF	Measured with a pulse technique.
Input Capacitance	C_{in}	–	5.0	–	5.0		
Output Capacitance	C_{out}	–	8.0	–	8.0		

NOTES: 1. Test circuit characteristics: R_T = 50 Ω, MCM10149; 100 Ω, MCM10549.
$C_L \leqslant 5.0$ pF (including jig and stray capacitance)
Delay should be derated 30 ps/pF for capacitive load up to 50 pF
2. The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
3. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.
4. $V_{CP} = V_{CC}$ = Gnd for normal operation.

*To be determined; contact your Motorola representative for up-to-date information.

PROGRAMMING THE MCM10149 †

During programming of the MCM10149, input pins 7, 9, and 10 are addressed with standard MECL 10K logic levels. However, during programming input pins 2, 3, 4, 5, and 6 are addressed with $0 \text{ V} \leqslant V_{IH} \leqslant +0.25$ V and $V_{EE} \leqslant V_{IL} \leqslant -3.0$ V. It should be stressed that this deviation from standard input levels is required only during the programming mode. During normal operation, standard MECL 10,000 input levels must be used.

With these requirements met, and with $V_{CP} = V_{CC} = 0$ V and $V_{EE} = -5.2$ V ± 5%, the address is set up. After a minimum of 100 ns delay, V_{CP} (pin 1) is ramped up to +12 V ± 0.5 V (total voltage V_{CP} to V_{EE} is now 17.2 V, +12 V − [−5.2 V]). The rise time of this V_{CP} voltage pulse should be in the 1–10 μs range, while its pulse width (t_{w1}) should be greater than 100 μs but less than 1 ms. The V_{CP} supply current at +12 V will be approximately 525 mA while current drain from V_{CC} will be approximately 175 mA. A current limit should therefore be set on both of these supplies. The current limit on the V_{CP} supply should be set at 700 mA while the V_{CC} supply should be limited to 250 mA. It should be noted that the V_{EE} supply must be capable of sinking the combined current of the V_{CC} and V_{CP} supplies while maintaining a voltage of −5.2 V ± 5%.

Coincident with, or at some delay after the V_{CP} pulse has reached its 100% level, the desired bit to be fused can be selected. This is done by taking the corresonding output pin to a voltage of +2.85 V ± 5%. It is to be noted that only one bit is to be fused at a time. The other three unselected outputs should remain terminated through their 50 ohm load resistor (100 ohm for MCM10549) to −2.0 V. Current into the selected output is 5 mA maximum.

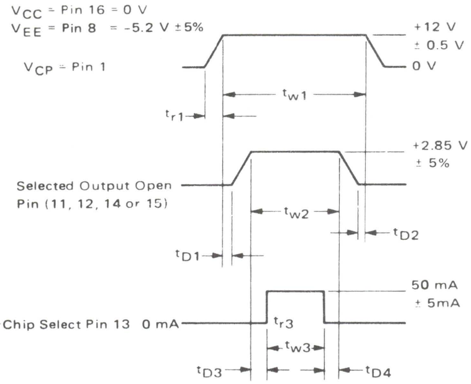
After the bit select pulse has been applied to the appropriate output, the fusing current is sourced out of the chip select pin 13. The 0% to 100% rise time of this current pulse should be 250 ns max. Its pulse width should be greater than 100 μs. Pulse magnitude is 50 mA ±5.0 mA. The voltage clamp on this current source is to be −6.0 V.

After the fusing current source has returned 0 mA, the bit select pulse is returned to it initial level, i.e., the output is returned through its load to −2.0 V. Thereafter, V_{CP} is returned to 0 V. Strobing of the outputs to determine success in programming should occur no sooner than 100 ns after V_{CP} has returned to 0 V. The remaining bits are programmed in a similar fashion.

† NOTE: For devices that program incorrectly, return serialized units with individual truth tables. Non compliance voids warranty.

PROGRAMMING SPECIFICATIONS

The following timing diagrams and fusing information represent programming specifications for the MCM10149.


V_{CC} = Pin 16 = 0 V
V_{EE} = Pin 8 = −5.2 V ±5%
V_{CP} = Pin 1
+12 V
± 0.5 V
0 V
t_{w1}
t_{r1}
+2.85 V
± 5%
Selected Output Open
Pin (11, 12, 14 or 15)
t_{w2}
t_{D2}
t_{D1}
50 mA
± 5mA
Chip Select Pin 13 0 mA
t_{r3}
t_{w3}
t_{D3}
t_{D4}

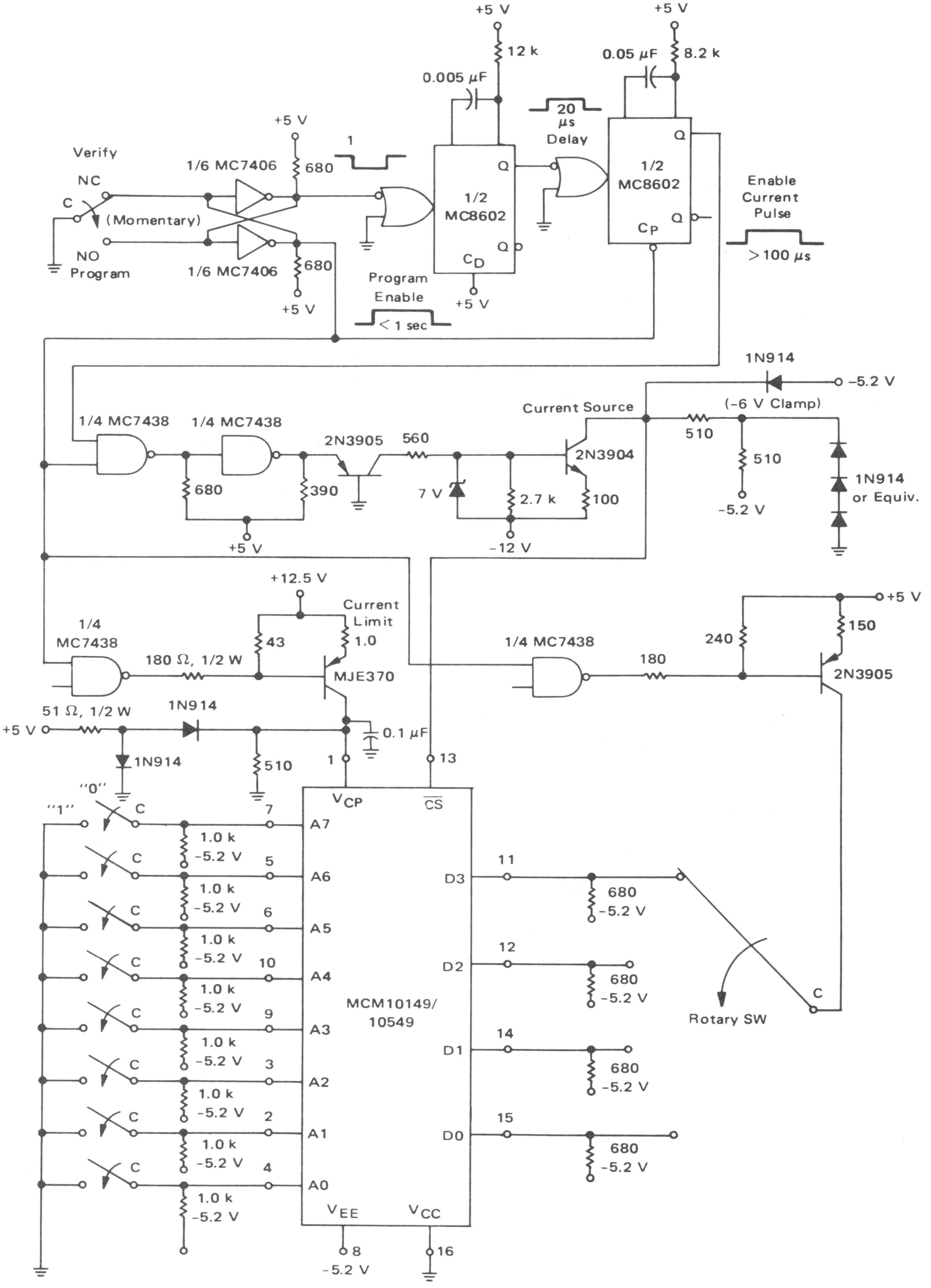
The timing diagram is shown for programming one bit. Note that only one bit is blown at a time. All addressing must be done 100 ns prior to the beginning of the V_{CP} pulse, i.e., V_{CP} = 0 V. Likewise, strobing of the outputs to determine success in programming should occur no sooner than 100 ns after V_{CP} returns to 0 V.

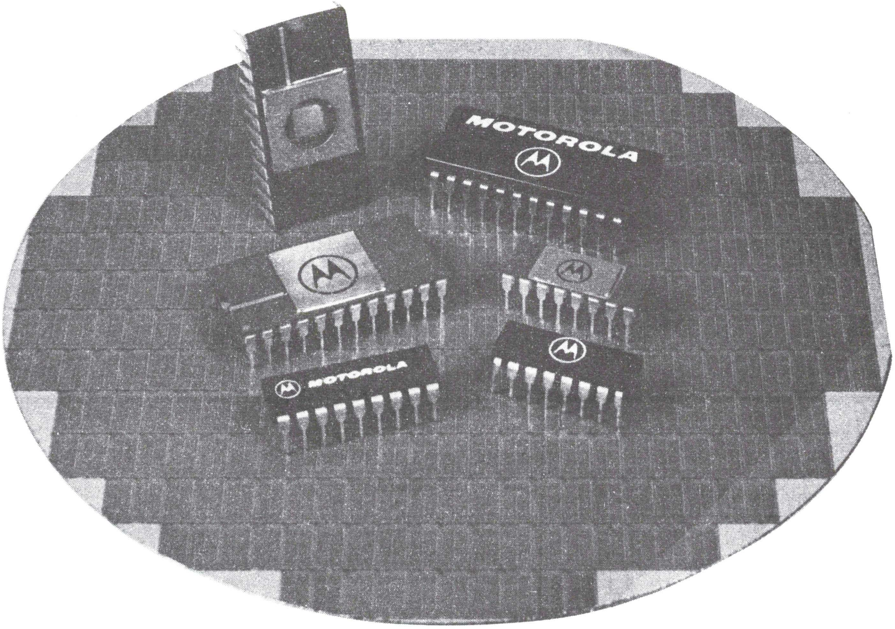
Note that the fusing current is defined as a positive current out of the chip select, pin 13. A programming duty cycle of ⩽ 15% is to be observed.

Definitions and values of timing symbols are as follows.

Symbol	Definition	Value
t_{r1}	Rise Time, Programming Voltage	⩾ 1 μs
t_{w1}	Pulse Width, Programming Voltage	⩾ 100 μs < 1 ms
t_{D1}	Delay Time, Programming Voltage Pulse to Bit Select Pulse	⩾ 0
t_{w2}	Pulse Width, Bit Select	⩾ 100 μs
t_{D2}	Delay Time, Bit Select Pulse to Programming Voltage Pulse	⩾ 0
t_{D3}	Delay Time, Bit Select Pulse to Programming Current Pulse	⩾ 1 μs
t_{r3}	Rise Time, Programming Current Pulse	250 ns max
t_{w3}	Pulse Width, Programming Current Pulse	⩾ 100 μs
t_{D4}	Delay Time, Programming Current Pulse to Bit Select Pulse	⩾ 1 μs

MANUAL PROGRAMMING CIRCUIT


+5 V
12 k
0.005 μF
+5 V
0.05 μF
8.2 k
20 μs Delay
Q
1/2 MC8602
Q
Cp
Enable Current Pulse
> 100 μs
+5 V
680
1
Verify
NC
C
(Momentary)
NO
Program
1/6 MC7406
1/6 MC7406
680
+5 V
1/2 MC8602
Q
Q
CD
+5 V
Program Enable
< 1 sec
1N914
–5.2 V
(–6 V Clamp)
Current Source
510
510
–5.2 V
1N914 or Equiv.
1/4 MC7438
1/4 MC7438
2N3905
560
2N3904
680
390
+5 V
7 V
2.7 k
100
–12 V
+12.5 V
Current Limit
1.0
43
1/4 MC7438
180 Ω, 1/2 W
MJE370
+5 V
150
240
1/4 MC7438
180
2N3905
51 Ω, 1/2 W
+5 V
1N914
1N914
510
0.1 μF
1
13
"0"
"1"
C
1.0 k
–5.2 V
7
5
6
10
9
3
2
4
VCP
CS
A7
A6
A5
A4
A3
A2
A1
A0
D3
D2
D1
D0
11
12
14
15
680
–5.2 V
MCM10149/ 10549
Rotary SW
C
VEE
VCC
8
–5.2 V
16


MOTOROLA
MOTOROLA

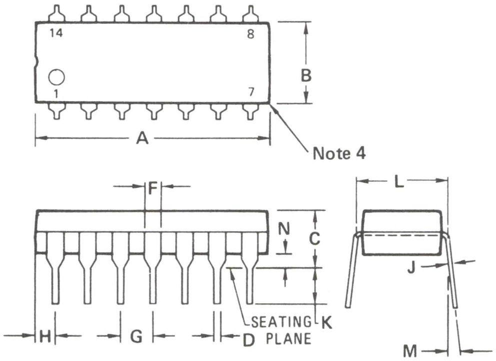
Mechanical Data

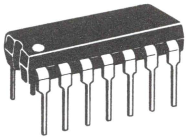
MECHANICAL DATA

The packaging availability for each device is indicated on the individual data sheets. Dimensions for the packages are given in this section.

14-PIN PACKAGES

PLASTIC PACKAGE
CASE 646





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	19.56	0.715	0.770
B	6.10	6.60	0.240	0.260
C	4.06	5.08	0.160	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0^{0}	10^{0}	0^{0}	10^{0}
N	0.51	1.02	0.020	0.040

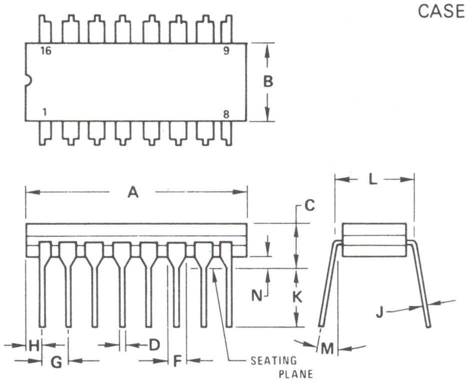
CASE 646-05

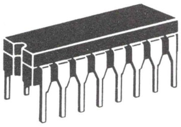
NOTES:

1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

16-PIN PACKAGES

FRIT-SEAL CERAMIC PACKAGE
CASE 620





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.10	7.49	0.240	0.295
C	–	5.08	–	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.32	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	–	15^{0}	–	15^{0}
N	0.51	1.02	0.020	0.040

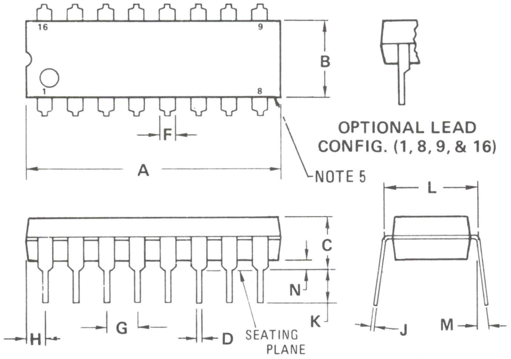
CASE 620-08

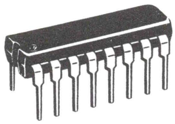
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. PACKAGE INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT.
3. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIM "A" AND "B" DO NOT INCLUDE GLASS RUN-OUT.
5. DIM "F" MAY NARROW TO 0.76 mm (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

MECHANICAL DATA (Continued)

16-PIN PACKAGES (Continued)

PLASTIC PACKAGE
CASE 648





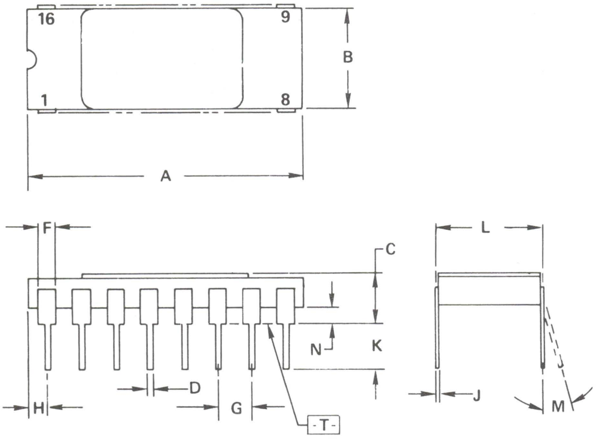
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.80	21.34	0.740	0.840
B	6.10	6.60	0.240	0.260
C	4.06	5.08	0.160	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.38	2.41	0.015	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

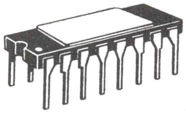
CASE 648-05

NOTES:

1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS 1, 8, 9, and 16).
5. ROUNDED CORNERS OPTIONAL.

CERAMIC PACKAGE
CASE 690





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.07	20.57	0.790	0.810
B	7.11	7.62	0.280	0.300
C	2.67	4.19	0.105	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.52	0.030	0.060
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	3.18	5.08	0.125	0.200
L	7.62 BSC		0.300 BSC	
M	–	10°	–	10°
N	0.38	1.52	0.015	0.060

CASE 690-13

NOTES:

1. -A- AND -B- ARE DATUMS.
2. -T- IS SEATING PLANE
3. POSITIONAL TOLERANCE FOR LEADS (D).

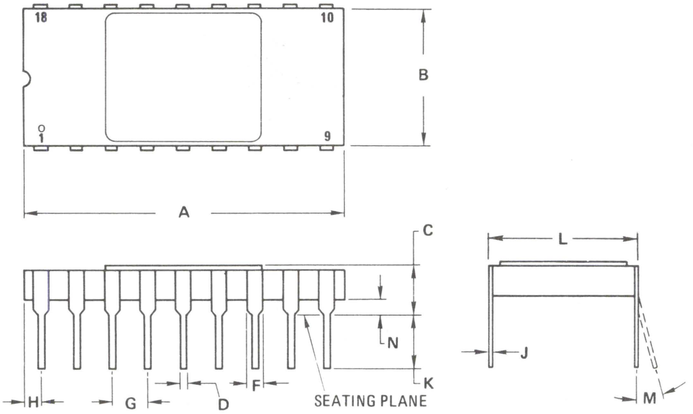
   ⌖ Ø 0.25 (0.010)Ⓜ T AⓂ BⓂ

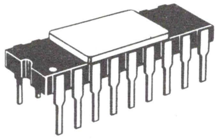
4. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.
6. 690-11 AND 690-12 OBSOLETE. NEW STANDARD 690-13.

MECHANICAL DATA (Continued)

18-PIN PACKAGES

CERAMIC PACKAGE
CASE 680





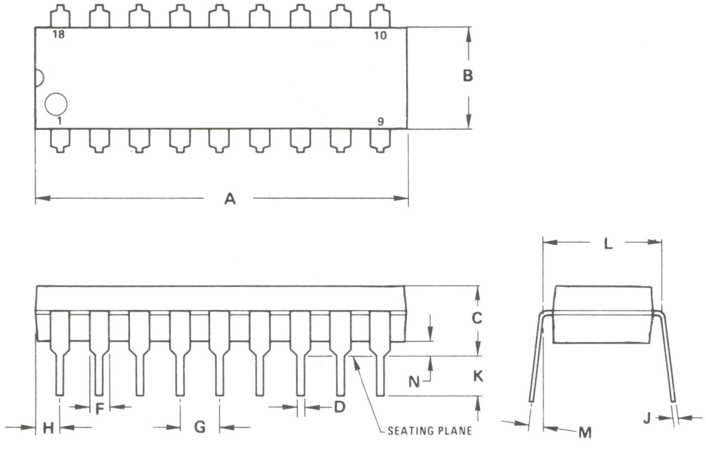
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.48	23.24	0.885	0.915
B	7.16	7.75	0.282	0.305
C	3.18	4.27	0.125	0.168
D	0.38	0.58	0.015	0.023
F	0.76	1.52	0.030	0.060
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.68	4.44	0.105	0.175
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.38	1.40	0.015	0.055

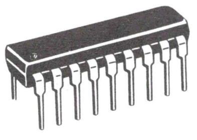
CASE 680-06

NOTES:

1. LEADS WITHIN 0.13 mm (0.005) RAD OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

PLASTIC PACKAGE
CASE 707





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

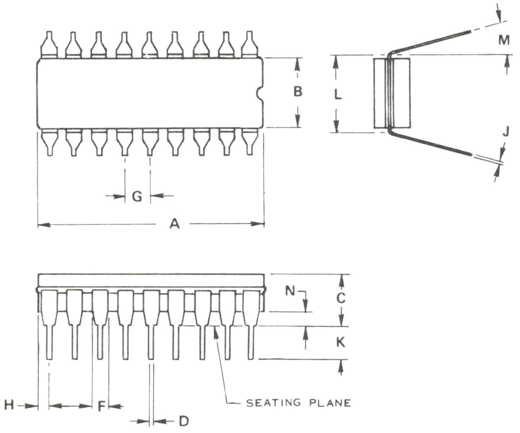
CASE 707-02

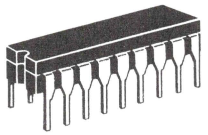
NOTES:

1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

18-PIN PACKAGES (Continued)

FRIT-SEAL CERAMIC PACKAGE
CASE 726



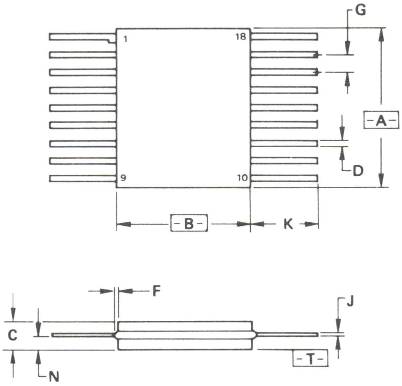


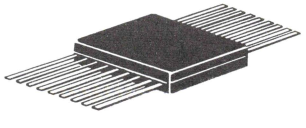
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.35	23.11	0.880	0.910
B	6.10	7.49	0.240	0.295
C	–	5.08	–	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.32	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

CASE 726-04

NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA. AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM "A" & "B" INCLUDES MENISCUS.

CERAMIC PACKAGE
CASE 747





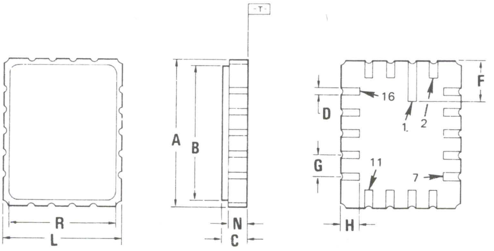
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	11.43	–	0.450
B	9.14	9.91	0.360	0.390
C	1.52	2.03	0.060	0.080
D	0.41	0.46	0.016	0.018
F	–	0.25	–	0.010
G	1.27 BSC		0.050 BSC	
J	0.10	0.15	0.004	0.006
K	–	7.75	–	0.305
N	–	0.89	–	0.035

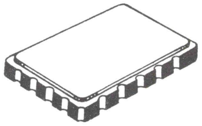
CASE 747-01

NOTES:
1. -A-, -B-, AND -T- ARE DATUMS.
2. -T- IS SEATING PLANE.
3. LEADS POSITIONAL TOLERANCE.
   ⌖ 0.13 (0.005) Ⓜ | T | A Ⓜ | B Ⓜ
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

18-PIN PACKAGES (Continued)

CERAMIC CHIP CARRIER PACKAGE
CASE 752



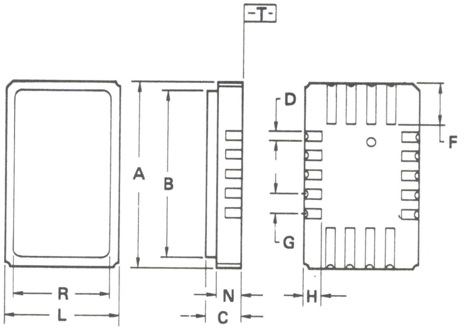


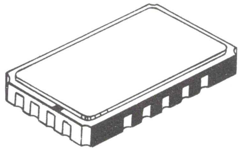
NOTES:
1. DIMENSIONS A AND L ARE DATUMS.
2. -T- IS GAUGE PLANE.
3. POSITIONAL TOLERANCE FOR TERMINALS (D): 18 PLACES
   ⌖ | 0.25 (0.010) Ⓜ | T | AⓈ | LⓈ
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.64	9.27	0.340	0.365
B	7.62	8.89	0.300	0.350
C	1.27	2.03	0.050	0.080
D	0.25	0.89	0.010	0.035
F	2.41	2.67	0.095	0.105
G	1.27 BSC		0.050 BSC	
H	1.02	1.52	0.040	0.060
L	6.98	7.62	0.275	0.0300
N	1.27	1.78	0.050	0.070
R	6.48	7.11	0.255	0.280

CASE 752-02

CERAMIC CHIP CARRIER PACKAGE
CASE 752A





NOTES:
1. DIMENSIONS A AND L ARE DATUMS.
2. -T- IS GUAGE PLANE.
3. POSITIONAL TOLERANCE FOR TERMINALS (D): 18 PLACES
   ⌖ | 0.25 (0.010) Ⓜ | T | AⓈ | LⓈ
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

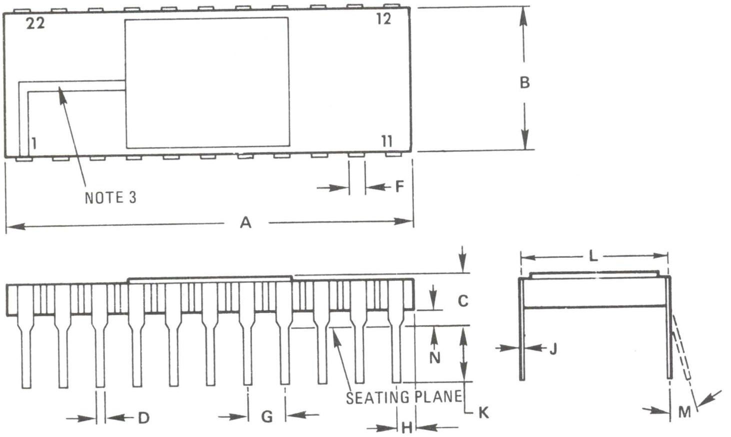
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	11.81	12.45	0.465	0.490
B	11.18	11.68	0.440	0.460
C	1.27	2.03	0.050	0.080
D	0.25	0.89	0.010	0.035
F	2.41	3.05	0.095	0.120
G	1.27 BSC		0.050 BSC	
H	0.89	1.52	0.035	0.060
L	7.11	7.75	0.280	0.305
N	1.27	1.78	0.050	0.070
R	6.35	6.86	0.250	0.270

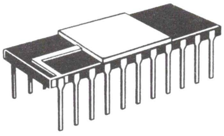
CASE 752A-01

MECHANICAL DATA (Continued)

22-PIN PACKAGES

CERAMIC PACKAGE
CASE 677





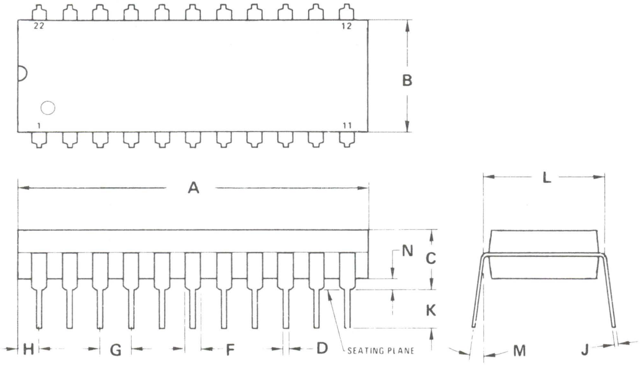
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	27.15	27.71	1.069	1.091
B	9.65	10.29	0.380	0.405
C	2.67	4.11	0.105	0.162
D	0.38	0.58	0.015	0.023
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.51	1.52	0.020	0.060
J	0.20	0.30	0.008	0.012
K	3.18	5.08	0.125	0.200
L	9.91	10.41	0.390	0.410
M	–	10°	–	10°
N	0.64	1.27	0.025	0.050

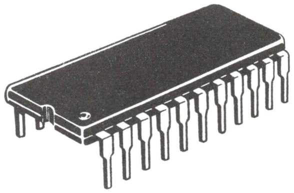
CASE 677-06

NOTES:

1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. EXPOSED CONTACT TO LEAD 1, OPTIONAL.

PLASTIC PACKAGE
CASE 708





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	27.56	28.32	1.085	1.115
B	8.64	9.14	0.340	0.360
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	10.16 BSC		0.400 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

CASE 708-04

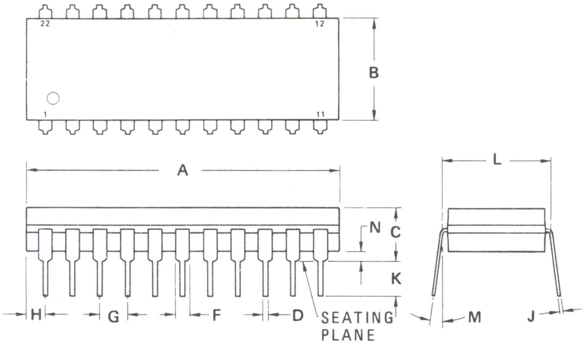
NOTES:

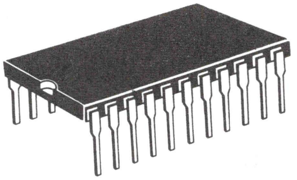
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

MECHANICAL DATA (Continued)

22-PIN PACKAGES (Continued)

FRIT-SEAL CERAMIC PACKAGE
CASE 736





NOTES:

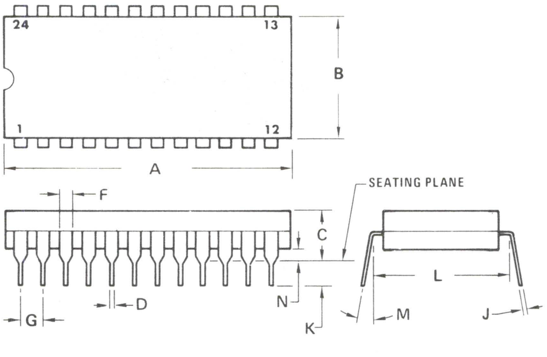
1. LEADS TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION (DIM "D").
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

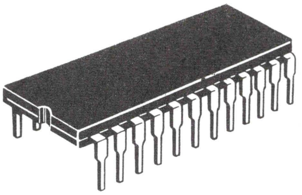
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	26.80	27.81	1.055	1.095
B	9.14	9.91	0.360	0.390
C	3.81	5.46	0.150	0.215
D	0.38	0.53	0.015	0.021
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.27	0.020	0.050
J	0.20	0.30	0.008	0.012
K	3.18	4.32	0.125	0.170
L	9.91	10.41	0.390	0.410
M	–	15°	–	15°
N	0.25	0.89	0.010	0.035

CASE 736-03

24-PIN PACKAGES

FRIT-SEAL CERAMIC PACKAGE
CASE 623





NOTES:

1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL).

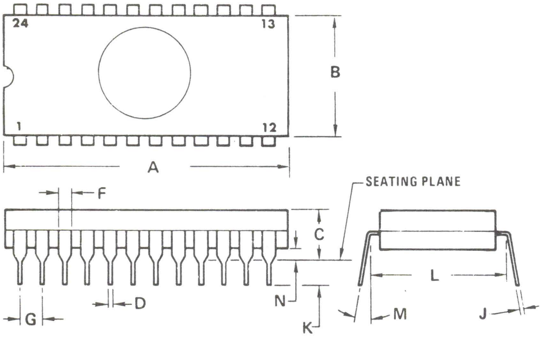
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	31.24	32.77	1.230	1.290
B	12.70	15.49	0.500	0.610
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

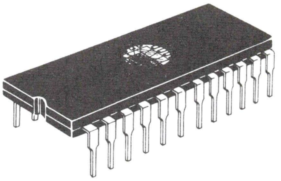
CASE 623-05

MECHANICAL DATA (Continued)

24-PIN PACKAGES (Continued)

FRIT-SEAL CERAMIC PACKAGE
CASE 623A



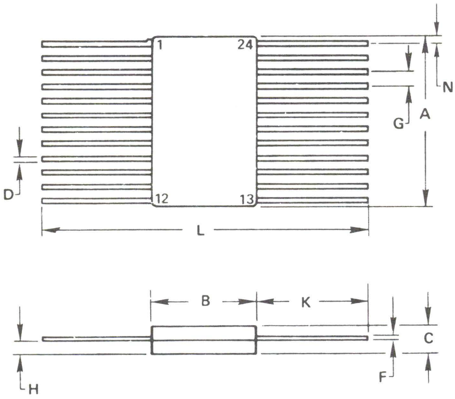


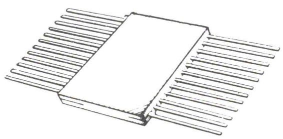
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.24	32.77	1.230	1.290
B	12.70	15.49	0.500	0.610
C	4.06	5.84	0.160	0.230
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

CASE 623A-03

NOTES:
1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL).

CERAMIC PACKAGE
CASE 652





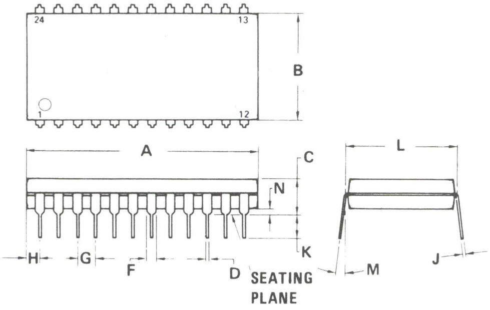
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.99	15.49	0.590	0.610
B	9.27	9.91	0.365	0.390
C	1.27	2.03	0.050	0.080
D	0.38	0.48	0.015	0.019
F	0.08	0.15	0.003	0.006
G	1.27 BSC		0.050 BSC	
H	0.69	1.02	0.027	0.040
K	6.35	9.40	0.250	0.370
L	21.97	–	0.865	–
N	0.25	0.63	0.010	0.025

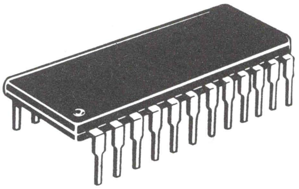
CASE 652-02

NOTES:
1. LEADS WITHIN 0.25 mm (0.010) TOTAL OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

24-PIN PACKAGES (Continued)

PLASTIC PACKAGE
CASE 709





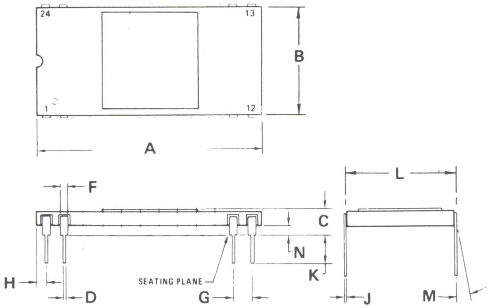
NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

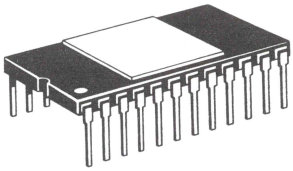
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.37	32.13	1.235	1.265
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.78	2.03	0.070	0.080
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

CASE 709-02

CERAMIC PACKAGE
CASE 716

See Case 716-07 for EPROM package.





NOTE:
1. LEADS TRUE POSITIONED WITHIN 0.25mm (0.010) DIA (AT SEATING PLANE) AT MAXIMUM MATERIAL CONDITION.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

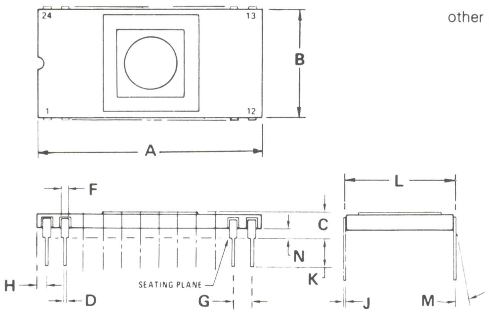
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	27.64	30.99	1.088	1.220
B	14.73	15.34	0.580	0.604
C	2.67	4.32	0.105	0.170
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	2.54	4.57	0.100	0.180
L	14.99	15.49	0.590	0.610
M	–	10°	–	10°
N	1.02	1.52	0.040	0.060

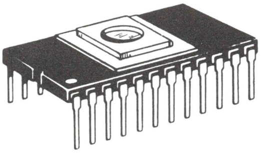
CASE 716-06

24-PIN PACKAGES (Continued)

CERAMIC PACKAGE
CASE 716

EPROM package only –
See Case 716-06 for
other packages.



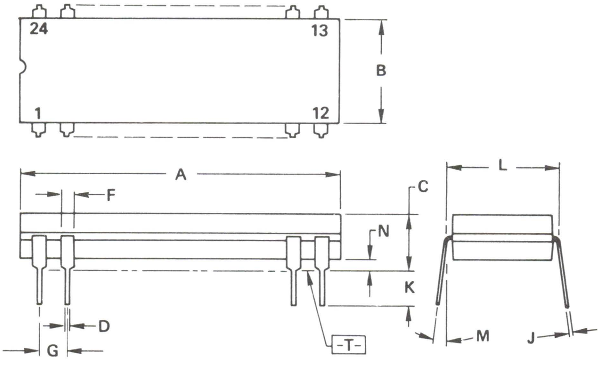


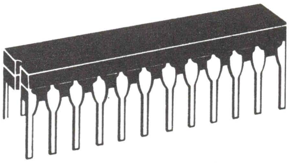
NOTE:
1. LEADS TRUE POSITIONED WITHIN 0.25mm (0.010) DIA (AT SEATING PLANE) AT MAXIMUM MATERIAL CONDITION.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	27.64	30.99	1.088	1.220
B	14.94	15.34	0.588	0.604
C	3.18	5.08	0.125	0.200
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	2.54	4.19	0.100	0.165
L	14.99	15.49	0.590	0.610
M	–	10°	–	10°
N	1.02	1.52	0.040	0.060

CASE 716-07

PLASTIC PACKAGE
CASE 748





	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	29.21	31.75	1.150	1.250
B	9.40	10.16	0.370	0.400
C	–	5.72	–	0.225
D	0.38	0.56	0.015	0.022
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	2.54	4.32	0.100	0.170
L	10.16 BSC		0.400 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

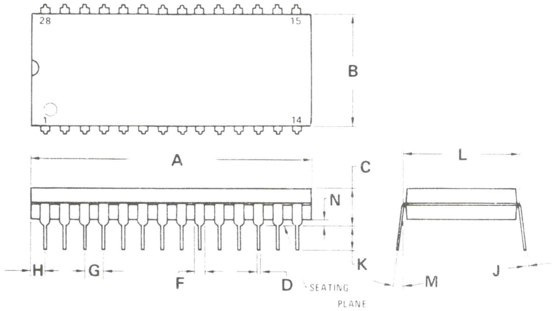
CASE 748-01

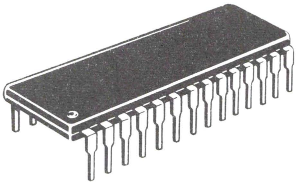
NOTES:
1. DIMENSIONS -A- AND -B- ARE DATUM.
2. POSITIONAL TOLERANCES FOR LEADS:
   ϕ | Ø 0.25 (0.010) Ⓜ | T | A Ⓜ | B Ⓜ
3. -T- IS SEATING PLANE.
4. DIMENSIONS A AND B INCLUDE MENISCUS.
5. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

MECHANICAL DATA (Continued)

28-PIN PACKAGES

PLASTIC PACKAGE
CASE 710





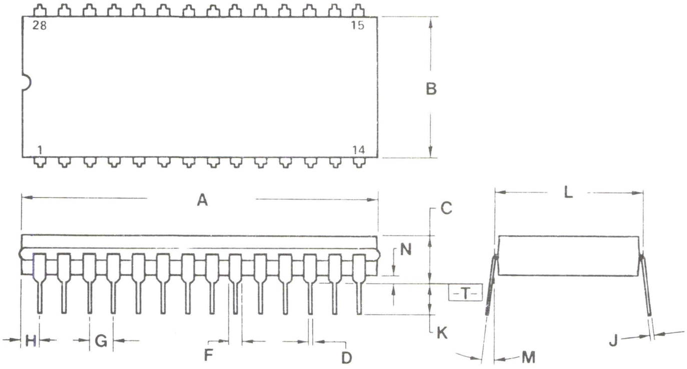
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	36.45	37.21	1.435	1.465
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

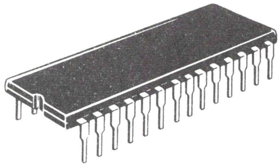
CASE 710-02

NOTES:

1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

FRIT-SEAL CERAMIC PACKAGE
CASE 733





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	36.45	37.85	1.435	1.490
B	12.70	15.37	0.500	0.605
C	4.06	5.84	0.160	0.230
D	0.38	0.56	0.015	0.022
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	5°	15°	5°	15°
N	0.51	1.27	0.020	0.050

CASE 733-03

NOTES:

1. DIM -A- IS DATUM.
2. POSITIONAL TOL FOR LEADS:
   ⌖ | Ø 0.25 (0.010) Ⓜ | T | A Ⓜ
3. -T- IS SEATING PLANE.
4. DIM A AND B INCLUDES MENISCUS.
5. DIM -L- TO CENTER OF LEADS WHEN FORMED PARALLEL.
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

TTL RAM	TTL RAM
TTL PROM	TTL PROM
MECL	MECL Memory General Information
MECL RAM	MECL RAM
MECL PROM	MECL PROM
Mechanical	Mechanical Data
Selector	Selector Guides
DRAM	MOS Dynamic RAM
SRAM	MOS Static RAM
EPROM	MOS EPROM
EEPROM	MOS EEPROM
ROM	MOS ROM

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